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Signed ..Chan...Pak....Kwong.......

Dedicated to my parents

Chan Sek Woon, Lam Yuen Kwai

and to my wife

Ha Thoai Ha

THE DESIGN OF ACTIVE RESISTORS AND TRANSCONDUCTORS IN A CMOS TECHNOLOGY

Pak Kwong CHAN

School of Electronic, Communication and Electrical Eng.,

University of Plymouth, Plymouth, Devon PL4 8AA, England.

In collaboration with the GEC Plessey Semiconductors, Plymouth.

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Abstract

This thesis surveys linearisation techniques for implementing monolithic MOS active resistors and transconductors, and investigates the design of linear tunable resistors and transconductors. Improving linearity and tunability in the presence of non-ideal factors such as bulk modulation, mobility-degradation effects and mismatch of transistors is a principal objective. A family of new non-saturation-mode resistors and two novel saturation-mode transconductors are developed. Where possible, approximate analytical expressions are derived to explain the principles of operation. Performance comparisons of the new structures are made with other well-known circuits and their relative advantages and disadvantages evaluated.

Experimental and simulation results are presented which validate the proposed linearisation techniques. It is shown that the proposed family of resistors offers improved linearity whilst the transconductors combine extended tunability with low distortion. Continuous-time filter examples are given to demonstrate the potential of these circuits for application in analogue signal-processing tasks.

Contents

1 Introduction **1**

1.1 Monolithic MOS Circuits 1

1.2 Overview of MOS Resistors 5

1.2.1 Linearisation Methods 5

1.2.2 Discussion of Published Resistor Circuits 10

1.3 Overview of MOS Transconductors 15

1.3.1 Linearisation Methods 15

1.3.2 Discussion of Published Transconductor Circuits 19

2 Fully Integrated MOS Resistors **36**

2.1 MOS Resistor Synthesis Elements 37

2.2 MOS Resistors with Unscaled-Gate Compensation 38

2.3 MOS Resistors with Dual Gate-Bulk Compensation 43

2.4 MOS Resistors with Scaled-Gate Compensation 50

2.5 Second-Order Effects 54

2.6 Applications of MOS Resistors 56

2.6.1 A Tow-Thomas Second-Order Lowpass Filter 57

2.6.2 Fourth-Order Sallen-Key Lowpass Filter 59

3 Performance Comparison of MOS Resistor Circuits **82**

3.1 Simulation Results 82

3.1.1 Unscaled-Gate Compensation Resistors 82

3.1.2 Dual Gate-Bulk and Scaled-Gate Compensation Resistors 85

3.1.3 MOS Filter Examples 92

3.2 Experimental Results 95

3.2.1 Layout Techniques 95

3.2.2 Unscaled-Gate Compensation Resistors and Filter Example 96

4 Fully Integrated MOS Transconductors **123**

4.1 Long-Tail Differential Pair (LTP) 123

4.2 Compensated Common-Source Pair (CCSP) 127

4.3 Cross-Coupled Pair (CCP) 130

4.4 Anti-Phase Common-Source Pair (ACSP) 131

4.5 Offset-Biased Cross-Coupled Pair (OBCCP) 133

4.6 Second-Order Effects 136

4.7 Transconductor-C Filter Example 137

5 Performance Comparison of MOS Transconductor Circuits **148**

5.1 Simulation Results 148

5.1.1 Linearisation of LTP 148

5.1.2 Linearised Transconductors 151

5.1.3 MOS Transconductor-C Filter Example 157
5.2 Experimental Results 158
5.2.1 Layout Techniques 158
5.2.2 LTP and ACSP Transconductors 159

6 Conclusions 181
6.1 Discussion of Results 181
6.2 Recommendations of Future Work 183

Bibliography 184

A List of Symbols 196

B CMOS Parameters for Plessey $2\mu m$ P-well Process 199

C CMOS Parameters for Plessey $1\mu m$ Twin Well Process 201

D Simplified Level-2 Non-Saturation-Mode Drain-Current Equations 203

E Simplified Level-3 Saturation-Mode Drain-Current Equations 207

F Dual Gate-Bulk Compensation Technique for Single-Transistor Resistor 210

G Analysis of Parallel-Form Resistor Based on Simplified Level-2 Non-Saturation Drain-Current Equation 213

H Analysis of Series-Pair Resistors Based on Simplified Level-2 Non-Saturation Drain-Current Equation 216

I Analysis of Series-Parallel Resistors Based on Simplified Level-2 Non-Saturation Drain-Current Equation 220

J Analytical Expressions of Dual Gate-Bulk Compensation Resistors Based on Simplified Level-3 Non-Saturation Drain-Current Equation 223

K Analysis of the Long-Tail Differential Pair 226

L Analysis of the Anti-Phase Common-Source Pair 229

M Analysis of the Cross-Coupled Pair 232

N Analysis of the Offset-Biased Cross-Coupled Pair 235

O Microphotograph of a Complete Chip 238

P Published Papers 239

List of Figures

1.1 MOS resistor and transconductor symbol 25
1.2 Notation for NMOS resistor/transconductor elements 25
1.3 Typical output characteristics for an NMOS transistor 26
1.4 Normal and lateral electric field 26
1.5 Resistor linearisation schemes 27
1.6 Dual gate-bulk compensation PFR 28
1.7 Shunt-feedback grounded resistor (SFGR) 28
1.8 Body-driven grounded resistor (BDGR) 29
1.9 Depletion-mode parallel-form resistor structure 29
1.10 Alternative parallel-form resistor structure 30
1.11 DPR-based balanced integrator 30
1.12 Four-transistor DPR 31
1.13 Transconductor linearisation schemes 32
1.14 Balanced source-degenerated transconductor 33
1.15 Multiple differential-pair-based linearisation schemes 34
1.16 Current-source-based OBDP transconductor 35
1.17 OBDP transconductor based on Negative Impedance Convertor 35

2.1 Fundamental CMOS resistor building blocks 62
2.2 P-channel source follower 62
2.3 Schematic of unscaled-gate compensation parallel-form resistor 63
2.4 Schematic of unscaled-gate compensation series-pair resistors 64
2.5 Schematic of unscaled-gate compensation series-parallel quad resistors . 65
2.6 Dual gate-bulk compensation TCR-I and TCR-II 66
2.7 N-channel source follower 66
2.8 N-channel differential-pair-based level-shifting buffer 67
2.9 Schematic of dual gate-bulk compensation parallel-form resistor 67
2.10 Schematic of dual gate-bulk compensation series-pair resistors 68
2.11 Schematic of dual gate-bulk compensation series-parallel quad resistors . 69
2.12 Circuit diagram of scaled signal generator 70
2.13 Schematic of scaled-gate compensation grounded resistor 71
2.14 Schematic of scaled-gate compensation floating resistor 71
2.15 Circuit diagram of the Tow-Thomas second-order filter 72
2.16 Normalised Tow-Thomas second-order filter 73
2.17 RC Tow-Thomas second-order filter at normalised values (Q=0.86) . . . 74
2.18 GVCR-based Tow-Thomas second-order filter, according to Fig. 2.17 . . 75
2.19 Simplified GVCR-based Tow-Thomas second-order filter 76
2.20 Second-order Sallen-Key lowpass filter 77
2.21 Fourth-order lowpass Butterworth 78
2.22 Fourth-order SPQR-based Sallen-Key lowpass filter 79
2.23 Modified VanPeteghem-Rice unity-gain buffer 80

2.24 Simplified fourth-order Sallen-Key lowpass filter 81

3.1 Control voltage tuning of static characteristics for unscaled-gate compensation PFR 101
3.2 Control voltage tuning of static characteristics for unscaled-gate compensation SPR-III 102
3.3 Control voltage tuning of static characteristics for unscaled-gate compensation SPQR-I 103
3.4 THD of unscaled-gate compensation PFR, SPR-III and SPQR-I with different resistance values at $0.5V_{pp}$, $\theta = 0.15V^{-1}$ 104
3.5 Static characteristic of PFR, SPR-III and SPQR-I for nominal resistance ($185.2K\Omega$) 104
3.6 THD of unscaled-gate compensation PFR, SPR-III and SPQR-I against signal level at nominal resistance ($185.2K\Omega$) for $\theta = 0.15V^{-1}$ 105
3.7 THD of unscaled-gate compensation PFR, SPR-III and SPQR-I with different resistance values at $0.5V_{pp}$, $\theta = 0.4V^{-1}$ 105
3.8 THD of unscaled-gate compensation PFR, SPR-III and SPQR-I against signal level at nominal resistance ($185.2K\Omega$) for $\theta = 0.4V^{-1}$ 106
3.9 Bandwidth of unscaled-gate compensation resistors at nominal resistance ($185.2K\Omega$) 106
3.10 Control voltage tuning of static characteristics for dual gate-bulk compensation PFR 107
3.11 Control voltage tuning of static characteristics for dual gate-bulk compensation SPR-I 108
3.12 Control voltage tuning of static characteristics for dual gate-bulk compensation SPR-III 109
3.13 Control voltage tuning of static characteristics for dual gate-bulk compensation SPQR-I 110
3.14 Control voltage tuning of static characteristics for dual gate-bulk compensation SPQR-II 111
3.15 Control voltage tuning of static characteristics for dual gate-bulk compensation SPQR-III 112
3.16 Control voltage tuning of static characteristics for scaled-gate compensation GVCR 113
3.17 THD of dual gate-bulk and scaled-gate compensation resistors with different resistance values at $0.5V_{pp}$, $\theta = 0.15V^{-1}$ and $\pm 5V$ supply 114
3.18 Static characteristics of dual gate-bulk and scaled-gate compensation resistors for nominal resistance ($120K\Omega$) 114
3.19 THD of dual gate-bulk and scaled-gate compensation resistors against input signal for nominal resistance ($120K\Omega$) 115
3.20 THD of dual gate-bulk and scaled-gate compensation resistor with different resistance values at $0.5V_{pp}$ for $\pm 2\%$ mismatches 115
3.21 Bandwidth of dual gate-bulk and scaled-gate compensation resistors at nominal resistance ($120K\Omega$) 116
3.22 Tuning of lowpass cut-off frequency in the GVCR-based filter 116
3.23 Comparison of simulated and ideal frequency characteristic at nominal $4.7KHz$ cut-off frequency 117
3.24 THD with variation of input signal at different frequencies (1/3 of cut-off frequencies) for GVCR-based filter 117
3.25 Comparison of simulated and ideal frequency characteristic at nominal $37KHz$ cut-off frequency for SPQR-based filter 118

3.26 Tuning of lowpass cut-off frequency in the SPQR-based filter 118
3.27 THD with variation of input signal at different frequencies (1/3 of cut-off frequencies) for SPQR-based filter 119
3.28 A microphotograh of unscaled-gate compensation CMOS resistors . . . 119
3.29 Experimental set-up for measuring total harmonic distortion of test resistor 120
3.30 Experimental THD comparison of PFR, SPR-III and SPQR-I with variation of resistance values at $0.5V_{pp}$ 120
3.31 Experimental comparison of static characteristics for PFR, SPR-III and SPQR-I at the nominal resistance of $37K\Omega$ 121
3.32 Experimental THD comparion of PFR, SPR-III and SPQR-I against input signal at the nominal resistance of $37K\Omega$ 121
3.33 Experimental family static characteristics of the SPQR-I 122
3.34 Experimental plot of THD with variation of input signal at different frequencies (1/3 of cut-off frequencies) for second-order Sallen-Key lowpass based on the SPQR-I 122

4.1 The differential-pair transconductor with constant-current biasing . . . 139
4.2 The differential pair under equivalent voltage-source excitation 139
4.3 Compensated common-source pair transconductor 140
4.4 Cross-coupled pair scheme 141
4.5 Cross-coupled pair transconductor 142
4.6 Proposed anti-phase common-source pair scheme 143
4.7 Anti-phase common-source pair transconductor 144
4.8 Proposed offset-biased cross-coupled pair scheme 145
4.9 Implementation of offset-biased cross-coupled pair transconductor 146
4.10 Second-order transconductor-C lowpass filter 147

5.1 Variation of quiescent gate overdrive and transconduction coefficients (normalised with respect to their $\theta = 0$ values) with mobility factor . . . 165
5.2 Third-harmonic distortion versus input bias current at 1KHz with a $1V_{pp}$ input signal and a $10\mu m/30\mu m$ aspect ratio 165
5.3 Transconductor structure 166
5.4 Control voltage tuning of static characteristic for LTP transconductor . 167
5.5 Control voltage tuning of static characteristic for CCSP transconductor 168
5.6 Control voltage tuning of static characteristic for CCP transconductor . 169
5.7 Control voltage tuning of static characteristic for ACSP transconductor 170
5.8 Control voltage tuning of static characteristic for OBCCP transconductor 171
5.9 THD of OTAs with different transconductance values at $1V_{pp}$ and $\pm 5V$ supplies 172
5.10 THD of OTAs with different transconductance values at $2.5V_{pp}$ and $\pm 5V$ supplies 172
5.11 Static Characteristics of the OTAs ($26\mu A/V$) 173
5.12 Comparison of OTAs with THD against input signal at nominal $26\mu A/V$ 173
5.13 Predicted third-harmonic distortion against bias current for LTP, CCP and ACSP at $1V_{pp}$ input signal 174
5.14 THD comparison of OTAs with variation of transconductance at $1V_{pp}$, 2% mismatches 174
5.15 THD comparison of OTAs with variation of transconductance at $2.5Vpp$, 2% mismatches and $\pm 5V$ supplies 175
5.16 Tuning of lowpass cut-off frequency in the ACSP-based filter 175

5.17 Comparsion of simulated and ideal frequency characteristic at nominal $4.7KHz$ cut-off frequency for ACSP-based filter 176
5.18 THD with variation of input signal at different frequencies (1/3 of cut-off frequencies) for ACSP-based filter 176
5.19 A microphotograph of the LTP and ACSP transconductors 177
5.20 Experimental set-up for measuring the total harmonic distortion of the LTP and ACSP 177
5.21 Experimental THD comparison of LTP and ACSP with variation of transconductance value 178
5.22 Experimental family static characteristics of the ACSP 178
5.23 Expermental comparison of static characteristics for the LTP and ACSP at the nominal $72\mu A/V$ 179
5.24 Experimental THD comparison of the LTP and ACSP against input signal at the nominal $72\mu A/V$ 179
5.25 Experimental Comparison of THD predicted by the standard equation [47] and the new equation 180

A.1 A NMOS Transistor with Terminal Voltages and Current 196

F.1 Dual Gate-Bulk Compensation Single Transistor 211

List of Tables

3.1 Performance comparison of unscaled-gate compensation resistors with $\theta = 0.15V^{-1}$ at nominal resistance ($185.2K\Omega$) 99

3.2 THD comparison of unscaled-gate compensation resistors with $\theta = 0.4V^{-1}$ at nominal resistance ($185.2K\Omega$) 99

3.3 Performance comparison of dual gate-bulk and scaled-gate compensation resistors with $\theta = 0.15V^{-1}$ and $\pm 5V$ supply voltage at norminal resistance ($120K\Omega$) 100

5.1 Device aspect ratios for the simulated transconductors 162

5.2 Performance comparison of OTAs at nominal transconductance $26\mu A/V$ 163

5.3 Device aspect ratios for the experimental LTP and ACSP transconductors 164

Chapter 1

Introduction

1.1 Monolithic MOS Circuits

CMOS processes were originally developed [1] as a means of fabricating digital logic circuitry and basically restrict the designer to using enhancement-mode MOS transistors. The processes typically offer good quality but low-valued capacitors and high-tolerance temperature-sensitive resistors.

A fundamental problem associated with the design of monolithic passive resistors in a CMOS technology is the inability to implement high-value linear resistors in an acceptable area of silicon wafer. Although resistors can be fabricated [2] as strips of polycrystalline silicon, the resistance density is low (20→200 ohms/square) and no adjustments are possible. Many solutions to this problem have been proposed [3]→[35] based on using the MOS transistor as a voltage-controllable two-terminal resistor or as a component in an electrically adjustable transconductor. Fig. 1.1 shows the basic symbols for these two active elements. A major problem with both approaches is that of harmonic distortion. In order to illustrate the fundamental cause of nonlinearity, the drain current is considered

as flowing through the n-channel MOSFET of Fig. 1.2. Typical $v \sim i$ characteristic curves are shown in Fig. 1.3. The transfer characteristic can be divided into two operating regions: nonsaturation and saturation. In the non-saturation region, the drain current (Appendix D) is given [36]→[38] by

$$\begin{aligned} I_d &= 2K\{[v_g - V_{FB} - \phi_B - \frac{(v_d + v_s)}{2}](v_d - v_s) \\ &\quad - \frac{2}{3}\gamma[(v_d - v_b + \phi_B)^{\frac{3}{2}} - (v_s - v_b + \phi_B)^{\frac{3}{2}}]\} \end{aligned} \tag{1.1}$$

where V_{FB} is the flat-band voltage, ϕ_B is the surface potential, γ is the bulk parameter. All the potentials v_g, v_b, v_d and vs are measured with respect to an external reference potential. The so-called [37] transconductance factor K is given as

$$K = \frac{\mu C_{ox} W}{2L} \tag{1.2}$$

where μ is the effective mobility, C_{ox} is the thin oxide capacitance per unit area, W is the channel width and L is the the channel length. By expanding the $\frac{3}{2}$ power terms, the drain current can be approximated [5],[37] as

$$I_d = 2K[(v_g - V_t^\star)(v_d - v_s) - \frac{m'}{2}(v_d^2 - v_s^2) + \frac{\gamma}{24(\phi_B - v_b)^{\frac{3}{2}}}(v_d^3 - v_s^3)] \tag{1.3}$$

where

$$V_t^\star = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - v_b} \tag{1.4}$$

and

$$m' = 1 + \frac{\gamma}{2\sqrt{\phi_B - v_b}} \tag{1.5}$$

Alternatively, a third-order approximation to drain current can be written (Appendix D) [38] as

$$I_d = 2K[(v_{gs} - V_t)v_{ds} - \frac{m}{2}v_{ds}^2 + \frac{\gamma}{24(\phi_B + v_{sb})^{\frac{3}{2}}}v_{ds}^3] \tag{1.6}$$

where

$$V_t = V_{FB} + \phi_B + \gamma\sqrt{\phi_B + v_{sb}} \tag{1.7}$$

and

$$m = 1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb}}} \tag{1.8}$$

Eqn (1.6) reveals that an MOS transistor can be used as a two-terminal resistor if v_{gs} is maintained constant or as a transconducting two-port network using v_{gs} as the control potential. It will be appreciated that, when used as a resistor, the quadratic and cubic terms in v_{ds} degrade the linearity. It can be noted that the cubic nonlinearity is usually smaller than the quadratic term.

When the MOS transistor is operated in the saturation region, the drain current can be approximately written as

$$I_d = K(v_{gs} - V_t)^2(1 + \lambda v_{ds}) \tag{1.9}$$

where the channel-length modulation factor λ models the finite output conductance. It will be appreciated that although resistor and transconductor behaviour can be implemented in this region, the saturated MOS transistor is typically employed as a transconductor. However, since I_d varies with the square of v_{gs}, linearisation techniques are necessary.

Additional non-ideal effects further complicate the linearisation process. For example, variation of process parameters such as γ and V_{FB} shift the value of threshold voltage V_t (see Eqn (1.7)). When the source-to-bulk voltage varies, V_t is modulated and subsequently, the resistance value. With respect to the transconductance parameter K, it is not unusual [39] to find a spread of around of 10 to 20 percent arising from variations in process and geometry parameters. However, the key factor affecting the transconductance parameter K is that μ, the carrier mobility, is a function of the terminal voltages. To explain this phenomenon, Fig.

1.4 shows the electric field in the cross-section of a MOS transistor. The carrier mobility varies with both the vertical and lateral electric fields in the channel and in general, high field strengths reduce the carrier mobility and thereby the drain current for a given set of bias potentials. The vertical electric field E_Y depends on $(v_{gs} - V_t)$, the oxide thickness and additionally on v_{sb} and the bulk doping. The lateral field E_X depends on the channel length and the applied drain-to-source voltage. For most practical cases, the effect of the vertical field on mobility is dominant and especially so for long channel transistors. Although accurate equations for μ are available [40], an approximate expression based only on the vertical field mobility reduction is usually sufficient to predict the mobility degradation effect. The expression typically adopted is

$$\mu = \frac{\mu_o}{1 + \theta(v_{gs} - V_t)} \tag{1.10}$$

The mobility degradation effect together with variation in V_t, which as noted, is a function of v_{sb}, produces significant additional harmonic distortion. This thesis provides a detailed account of these problems and of possible solutions for both non-saturation resistors and saturation transconductors.

Another major problem for active resistors and transconductors is that the signal-handling capability is affected by the tuning process. The tunability is closely related to the architecture of the active resistors/transconductors and signal levels employed and can be a crucial factor. An objective of this work is to consider possible solutions for achieving highly tunable circuits.

Finally, other issues such as ease of design and silicon area are also considered in the design of active resistors and transconductors. This can be important not merely in terms of reducing the design burden but the utilization of silicon area often reflects the complexity of circuits. Although simple circuits usually occupy

small silicon area, they typically involve a design trade-off between performance and ease of design. The circuits proposed in this thesis, whenever possible, aim at combining ease of design with high levels of performance and efficient utilization of silicon area.

1.2 Overview of MOS Resistors

1.2.1 Linearisation Methods

Although active devices occupy less chip area than passive elements, their use increases nonlinearity, reduces signal swing and requires the provision of biasing circuits as previously noted. There are two competing approaches to active resistor design. The first [3]→[31] is based on operating transistors in the non-saturation region, and the second [32]→[35] utilizes transistors operating in saturation. In either case, the goal is to design an active resistor that has good linearity, has a large signal-handling capability, is simple to implement and can be tuned over a wide range. An ability to operate in single-ended mode is also desirable because of the additional silicon area associated with balanced operational amplifiers.

With reference to Eqn (1.3), the major contribution to the drain current distortion is the dependence on $(v_d^2 - v_s^2)$. The quadratic term can be split into two parts only; one of which is γ-dependent. The γ-dependent term is contributed by the modulation of the source with respect to the bulk. Suppression of this so-called bulk effect would significantly reduce the total distortion. Several linearisation schemes have been suggested [3]→[35]. Some schemes [3]→[8] attempt to eliminate nonlinearities in the current of either single or multiple devices. Other schemes [9]→[35] attempt to cancel nonlinearities by summing or subtracting cur-

rents in matched devices. Fig. 1.5 summarises the basic schemes based on transistors operating in non-saturation. Although both Eqns (1.3) and (1.6) are useful for simulation purposes, it will be convenient at this point to neglect the cubic terms (which are typically smaller than the quadratic term by an order of magnitude or more). The simplified expressions are

$$I_d = 2K[(v_g - V_t^\star)(v_d - v_s) - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - v_b}})(v_d^2 - v_s^2)] \tag{1.11}$$

and

$$I_d = 2K[(v_{gs} - V_t)v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb}}})v_{ds}^2] \tag{1.12}$$

where $V_t^\star$ and V_t are defined as Eqns (1.4) and (1.7), respectively. It is further assumed that mobility is constant.

1.2.1.1 Single-Transistor Resistor (STR)

The common approach [8] for single transistor linearisation is the unscaled-gate compensation. This involves applying an unscaled signal common-mode component combined with a bias control voltage V_C to the Single Transistor Resistor (STR) as shown in scheme (a), the drain current in equation (1.11) becomes

$$I_d = 2K[(V_C - V_T)v_{ds} - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \tag{1.13}$$

where

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V_B} \tag{1.14}$$

It will be seen that although the main quadratic term has been eliminated the remaining gamma-related quadratic term will restrict the linearity of the STR. There are two principle ways to cancel this gamma-related quadratic component. The first approach is scaled-gate compensation [5] where a scaled common-mode

control signal equal to

$$v_g = V_C + (1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(\frac{v_d + v_s}{2}) \quad (1.15)$$

is applied to the gate. Substituting this equation back into (1.11), the drain current

$$I_d = 2K(V_C - V_T)v_{ds} \quad (1.16)$$

is a linear function of v_{ds}.

The second approach is dual gate-bulk compensation [8]. This involves simultaneously modulating the gate and bulk nodes by common-mode signals given as $v_g = V_C + (\frac{v_d+v_s}{2})$ and $v_b = V_B + (\frac{v_d+v_s}{2})$, where V_C and V_B are dc levels. The algebra for this approach is given in Appendix F where it is shown that design resistance becomes: $[2K(V_C - V_T)]^{-1}$. However, these approaches are difficult to implement in integrated circuit applications because of the need to generate the common-mode signal.

1.2.1.2 Parallel-Form Resistor (PFR)

Scheme (b) shows the circuit configuration for the Parallel-Form Resistor (PFR) [9]. Linearisation is achieved by coupling unscaled terminal voltages to the individual gates of the transistor pair. Using Eqn (1.11), the drain currents in M1 and M2 are given by

$$I_1 = 2K[(V_C + v_d - V_T)v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(v_d^2 - v_s^2)] \quad (1.17)$$

and

$$I_2 = 2K[(V_C + v_s - V_T)v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(v_d^2 - v_s^2)] \quad (1.18)$$

Adding the two current gives

$$I = 4K[(V_C - V_T)v_{ds} - \frac{\gamma}{4\sqrt{\phi_B - v_B}}(v_d^2 - v_s^2)] \quad (1.19)$$

It can be seen that the main quadratic term is cancelled but linearity is again degraded by the gamma-related term. The influence of this component, however, can be reduced by dual gate-bulk compensation [8] and β-scaling compensation [10],[14]. Dual gate-bulk compensation involves modulating both the gate and bulk with the same unscaled control signal. β-scaling compensation involves the intentional adjustment of the aspect ratios of the transistor pairs.

In the β-scaling scheme, assume the transistor transconductance to be K_1 for M1 and K_2 for M2. By Eqn (1.11), the drain currents are

$$I_1 = 2K_1[(V_C + m_k v_d - V_T)v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(v_d^2 - v_s^2) \tag{1.20}$$

and

$$I_2 = 2K_2[(V_C + m_k v_s - V_T)v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(v_d^2 - v_s^2) \tag{1.21}$$

The summation of these drain currents gives

$$\begin{aligned} I &= (2K_1 + 2K_2)(V_C - V_T)v_{ds} + (2K_1 v_d + 2K_2 v_s)v_{ds} \\ &\quad - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(2K_1 + 2K_2)(v_d^2 - v_s^2) \end{aligned} \tag{1.22}$$

There is no set of K_1 and K_2 which will eliminate the quadratic term in the general case. However, for the special condition $v_s = 0$ and $v_d = V_{in}$, Eqn (1.26) is then reduced to the form

$$I = (2K_1 + 2K_2)(V_C - V_T)V_{in} + [2K_1 - (1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(K_1 + K_2)]V_{in}^2 \tag{1.23}$$

from which it can be seen that the quadratic term is completely suppressed when

$$\frac{2K_1}{K_1 + K_2} = 1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}} \tag{1.24}$$

and the resistance value becomes $[2(K_1 + K_2)(V_C - V_T)]^{-1}$. Thus, this β-scaling technique is only valid for grounded applications.

1.2.1.3 Series-Pair Resistor (SPR)

Scheme (c) shows how linearisation can be obtained by feeding back the mid-point potential to the common gate for a series-connected transistor pair, which is referred to as the Series-Pair Resistor (SPR) [16]. An analysis using Eqns (1.6)→(1.8) gives

$$I = K[(V_C - V_T)v_{ds} - \frac{(1+\delta)}{8(V_C - V_T)}v_{ds}^3 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \qquad (1.25)$$

where $\delta = \frac{\gamma}{2\sqrt{\phi_B - V_B}}$. In this compound transistor structure, the quadratic terms in v_{ds} are eliminated but a series of odd ordered distortion terms are generated which combine with the residual gamma-related quadratic term. This quadratic component can be eliminated using the dual gate-bulk compensation technique noted earlier. This is achieved by driving the bulks together with the gates with the offset mid-point potential.

1.2.1.4 Differential-Pair Resistor (DPR)

The final scheme (d), the Differential Pair Resistor (DPR) [19], shows a pair of transistor driven by balanced signals. Noting that both right-hand terminals share the same potential V_x, the drain currents are

$$I_1 = 2K\{(V_C - V_T)(V_{in} - V_x) - (1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})[V_{in}^2 - V_x^2]\} \qquad (1.26)$$

and

$$I_2 = 2K\{(V_C - V_T)(-V_{in} - V_x) - (1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})[(-V_{in})^2 - V_x^2]\} \qquad (1.27)$$

The difference of the two current gives

$$I = 4K(V_C - V_T)V_{in} \qquad (1.28)$$

Thus the current is independent on V_x and moreover is free of bulk effect. In practice, odd-order terms not included in this simplified analysis will be present.

1.2.2 Discussion of Published Resistor Circuits

Linearisation techniques based on a single device are of much interest since they avoid the problems associated with mismatches in transistor pairs and the additional silicon requirement of balanced networks. The Shunt-Feedback Grounded Resistor (SFGR) [3] was the earliest attempt at linearising a single MOS transistor by generating a common-mode voltage via a resistor-based feedback network. The structure is shown in Fig. 1.7. The linearisation technique is a special case of the unscaled-gate compensation technique for the STR in scheme (a). Unfortunately, as already seen, the gamma-related quadratic component degrades the linearity and furthermore, high-quality passive integrated resistors are not available. Although its variant [4] improves the distortion performance, the technique demands both the operational amplifiers and passive resistors. Banu and Tsividis proposed [8] the unscaled common-mode gate compensation and dual common-mode gate-bulk compensation for a CMOS floating transistor as discussed in the STR scheme. A variant is the Body-Driven Grounded Resistor (BDGR) [6]. Fig. 1.8 shows the schematic structure. The basic principle is to inject the bulk terminal with an appropriate input signal such that the generated distortion cancelling term would match to either the even or odd order distortion, depending on the choice of scaled value of the input signal. Let the scale factor for the input voltage be β, the bulk voltage is $v_b = \beta V_{in} + V_B$. Using Eqn (1.11), the drain current can be approximated as

$$I_d \approx 2K[(V_C - V_T)V_{in} - \frac{\gamma\beta}{2\sqrt{\phi_B - V_B}}V_{in}^2 - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})V_{in}^2] \qquad (1.29)$$

By choosing the scale factor as

$$\beta = -\frac{1}{2}(1 + \frac{2\sqrt{\phi_B - V_B}}{\gamma}) \qquad (1.30)$$

the quadratic term is cancelled. The theory works equally well for the extension to the cubic term but the analysis is more complex. The major difference between this body-driven technique and the scaled-gate-compensated technique [5] is that a phase reversed signal voltage is required. In addition, the magnitude of bulk driven signal is higher than that of the gate compensation signal. Importantly however, the previous techniques [5],[6] lack any practical means of generating the compensation signals in integrated form. Even though compensation circuits can be synthesised using traditional operational amplifiers and passive resistors, it is not a cost-effective approach for integrated applications.

The parallel-form resistor PFR [8]→[15] takes two principle forms. The first [8]→[10],[15] is based on a transistor pair operating in the triode region. The second [11]→[14] relies on one transistor operating in the triode region and the other transistor in saturation. A triode PFR type based on scheme (b) has been proposed [8],[9]. As previously noted, linearisation is obtained when the gate potentials are coupled with appropriate control and terminal signals. Implementation is easily achieved via the use of opposite-transistor-type buffers as the coupling circuits. As an alternative to the use of enhancement-mode transistor pair, depletion-mode devices has been employed [10] in the resistor structure shown in Fig. 1.9. The depletion-mode structure is simpler than the enhancement counterpart because depletion transistors conduct when the input signal is zero and avoid the need for biasing circuitry. The price paid for this is an increase in sensitivity since additional process steps are required to fabricate the depletion transistors. Moon et al. [11] suggested a PFR form as depicted in Fig. 1.10. By Eqns (1.11) and (1.4), the non-saturation current flowing via M1 is

$$I_1 = 2K[(V_C - V_{TO})V_{in} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B}})V_{in}^2] \tag{1.31}$$

where

$$V_{TO} = V_{FB} + \phi_B + \gamma\sqrt{\phi_B} \tag{1.32}$$

Ignoring the channel-length modulation effect, the saturated drain current (Eqn 1.9 and 1.7) in M2 can be approximated as

$$I_2 = K(V_{in} + V_R - V_{TO})^2 \tag{1.33}$$

where V_R is the dc bias source for M2. Addition of the two currents yields

$$I = 2K[(V_C + V_R - V_{TO})V_{in} + \frac{1}{2}K(V_R + V_{TO})^2 - \frac{\gamma}{4\sqrt{\phi_B}}V_{in}^2] \tag{1.34}$$

It can be seen that complete cancellation of the nonlinearity is not achieved in this resistor because of the bulk modulation in M1. Since the bulk terminal of M1 is shorted to ground and the source-to-bulk voltage in M2 is zero, this lowers the threshold voltage of the transistors and raises the gamma-related quadratic components compared with other PFR schemes. But the major problems are the generation of an offset (dc) component in the current and the fact that operation is restricted to one quadrant due to the bulk connection arrangement of M1 and M2. Although the structure can be extended to two quadrants using the opposite-transistor-type circuit [12], elimination of the offset requires matched p-channel and n-channel transistors. Wang [13] offered a solution to the offset problem but again, the resistor operates only in one quadrant.

However, the fundamental problems associated with this group of parallel form resistors are the quadratic gamma-related distortion component, mobility degradation and resistance dependence on threshold process parameters. Among these problems, the gamma-dependent quadratic component due to bulk modulation in schemes [9]→[12] is the dominant distortion source. As a consequence, these circuits are only suitable for applications with high supply voltages and low gamma

processes. Techniques involving dual gate-bulk compensation [8] and β-scaling [13]→[15] compensation could reduce this gamma-dependent distortion. Even though these improved schemes suppress the unwanted gamma-related quadratic term, the mobility degradation effect which causes the error in the cancellation of nonlinearity, is ignored by all the PFR schemes. The resistance dependence on V_T remains unsolved.

The series structures of Fig. 1.5(c) are attractive active resistors owing to their simplicity in terms of silicon efficiency when compared to the PFR. VanPeteghem and Rice [16],[17] made an important contribution with the CMOS series-pair resistor (SPR) using the dual gate-bulk compensation technique. The distortion due to the gamma-related quadratic term is eliminated. Unlike the buffers in the PFR scheme [8],[9] which use opposite transistor types, the buffer proposed by VanPeteghem and Rice eliminates the need to match p-channel and n-channel transistors. As a result, the resistance is independent of V_T (as indicated in Eqn (H.18)) and less sensitive to process variations. Chapter 2 further explores this technique which was also adopted in a depletion-mode version [18] based upon Silicon-on-Sapphire (SOS) technology. SOS CMOS processes have several potential advantages over the traditional CMOS technologies. These include higher density, lower parasitic capacitance and a radiation-hard property. Unlike the PFR schemes, series structures reduce the mobility degradation effect because the gate-source voltages are lower for the same terminal signal conditions. Unfortunately, the scheme in [16] and [17] generates a bias-dependent cubic distortion whereas that in [18] generates a non-bias-dependent cubic term. In applications where a wide tuning range is needed, the low-bias condition imposes the problem of linearity on the circuit [16],[17].

One of the earliest MOS resistors was the DPR arrangement [20]→[22] as shown in Fig. 1.11. The balanced operation virtually eliminates all even-order distortion and the remaining odd distortion is relatively small. The resistance does, however, depend upon $4K(V_C - V_T)$ and variation of process parameters can produce the changes in K and V_T. The resulting changes in resistance must then be corrected. It may be noted that balanced architectures are silicon inefficient and require the operational amplifiers to have good common-mode rejection characteristics.

The DPR has a four-transistor form [24],[25] as illustrated in Fig. 1.12. In this structure, the resistance value is actually independent on V_T and is given as $[4K(V_A - V_C)]^{-1}$. Furthermore, the circuit is claimed to cancel distortion of any order at the expense of higher thermal noise and mismatch sensitivity. Unfortunately, the four-transistor-based DPR suffers from the problem that the linearity of the resistor is reduced by the mobility degradation effect because of the difference in gate control signals applied to the MOS transistor pairs. This technique also demands a relatively high silicon area and good common-mode rejection ratio.

Czarnul [26],[27] suggested a modification to convert a single input into balanced form for the DPR but such a scheme would be expensive needing an operational amplifier for each resistor. Other modifications [23],[28] together with various synthesis techniques [29],[30] have adopted four-transistor DPR techniques for single-ended applications but distortion performance is degraded due to mobility-related nonlinearities.

The discussion so far has related to nonsaturation-mode resistors. Saturation-mode active resistors have received much attention since they usually offer low

supply operation, good linearity and are free of the bulk effect. An early example [32] uses a current-differencing technique which employs current mirrors to copy and subtract the currents on a group of four transistors in the saturation region. This method was then repeated for the non-saturation counterpart [31]. Wang proposed a non-tunable transresistor [33] and a balanced resistor structure [34]. The resistor suggested by Steyaert et al. [35] suffers from the problem that the resistance value, which makes use of channel-length modulation effect, is highly process sensitive because the channel-length modulation factor is a function of many process parameters and of the specified channel length in particular.

1.3 Overview of MOS Transconductors

1.3.1 Linearisation Methods

In active filter applications where small chip area and high-frequency characteristics are considered important, the use of 'OTA-C' techniques, as an alternative to operational amplifier based circuits, are particularly promising [41]→[43]. These 'OTA-C' techniques use operational transconductance amplifiers together with capacitors as the principal filter elements. Given the importance of CMOS technology to commercial integrated-circuit manufacture, many CMOS-based techniques [47]→[84] have been proposed. Operational transconductance amplifiers or transconductors can be classified according to the mode of operation as either saturation-mode or nonsaturation-mode. Practical transconductors should possess low distortion, wide tunability, large input-signal range, low power consumption, good frequency response, a single-ended driven property and where possible have a simple structure.

A major objective in transconductor design is to modify the normal square-law behaviour of the transistor as described in Eqns (1.9) and (1.6), respectively. Some saturated-mode transconductors make uses of negative feedback [47],[49]→[54],[59] but the majority [55],[56],[60]-[74] are linearised by taking the difference of square-law currents. An alternative linearisation technique exploits the cancellation of nonlinearity in a non-saturated transistor-based transconductor [75]→[78] Fig. 1.13 summarises the basic linearisation schemes. Schemes (a)→(d) are based on transistors operating in the saturation region and scheme (e) is based on non-saturation transistor. The linearisation techniques will be illustrated by means of the simplified square-law [47] equation

$$I_d = K(v_{gs} - V_t)^2 \tag{1.35}$$

where $K = \mu C_{ox} W/2L$, assuming that the mobility carrier μ is constant, and channel-length modulation is negligible. It may be noted that since the source and bulk terminals are typically shorted to each other, bulk effect is normally absent and the threshold voltages are not signal dependent.

1.3.1.1 Source-Degeneration Pair (SDP)

A common linearisation technique involves applying negative feedback in the form of source-degenerated elements in a differential pair. The portion of input signal that appears across the input transistors of the differential pair is thereby reduced, with improvement to linearity and the differential input swing. The so-called [49] Source-Degenerated Pair (SDP) is shown in scheme (a). Using the simplified square-law of Eqn (1.39), it can be shown that

$$V_{in} = v_1 - v_2 = v_{gs1} + I_1 R - v_{gs2} - I_2 R \tag{1.36}$$

where

$$v_{gs1} = \sqrt{\frac{I_1}{K}} + V_{TO} \tag{1.37}$$

and

$$v_{gs2} = \sqrt{\frac{I_2}{K}} + V_{TO} \tag{1.38}$$

On account of the constant current relationship, $2I = I_1 + I_2$, the output current is obtained as

$$I_o = I_1 - I_2 = 2i = 2\sqrt{KI}V_{in}(1 - \frac{2iR}{V_{in}})\sqrt{1 - \frac{KV_{in}^2}{4I}(1 - \frac{2iR}{V_{in}})^2} \tag{1.39}$$

If it is assumed that the voltage drop across R is mainly contributed by the first-order signal current component $\sqrt{KI}V_{in}$, the output difference current can be approximated as

$$I_o \approx GV_{in}(1 - GR)\sqrt{1 - \frac{KV_{in}^2}{4I}(1 - GR)^2} \tag{1.40}$$

where $GR < 1$ and

$$G = 2\sqrt{KI} \tag{1.41}$$

and the transconductance is

$$G_m = \frac{dI_o}{dV_{in}} = G(1 - GR)[\sqrt{1 - \frac{KV_{in}^2}{4I}(1 - GR)^2} - \frac{\frac{KV_{in}^2}{4I}(1 - GR)^2}{\sqrt{1 - \frac{KV_{in}^2}{4I}(1 - GR)^2}}] \tag{1.42}$$

The terms in V_{in} cause significant distortion under large-signal conditions. The element R can be passive or active. It can be seen that, using high resistance value of R as negative feedback, the transconductance is reduced in exchange for an improved linearity. For the special case when R = 0, the current takes the well-known [47] form

$$I_o = GV_{in}\sqrt{1 - \frac{KV_{in}^2}{4I}} \tag{1.43}$$

and the transfer function becomes

$$G_m = G[\sqrt{1-\frac{KV_{in}^2}{4I}} - \frac{\frac{KV_{in}^2}{4I}}{\sqrt{1-\frac{KV_{in}^2}{4I}}}] \quad (1.44)$$

1.3.1.2 Compensated Common-Source Pair (CCSP)

An LTP can be linearised by making the tail current a function of the input signal. Scheme (b) shows the schematic diagram for the Compensated Common-Source Pair (CCSP) [60]. By choosing the tail current as

$$I_t = I + \frac{KV_{in}^2}{4}, \quad (1.45)$$

the transconductance G becomes $2\sqrt{KI}$. The advantage of this technique is that linearity is improved without a reduction in transconductance.

1.3.1.3 Cross-Coupled Pair (CCP)

In scheme (c), when the transistor pair is configured as a Cross-Coupled Pair (CCP) [65] as denoted in Fig. 1.13, subtraction of their drain currents cancels the nonlinear terms. The drain currents in M1 and M2 are given by

$$I_1 = K(v_1 - v_2 - V_Q - V_{TO})^2 \quad (1.46)$$

and

$$I_2 = K(v_2 - v_1 - V_Q - V_{TO})^2 \quad (1.47)$$

where V_Q is the dc bias and is defined as

$$V_Q = \sqrt{\frac{I}{K}} + V_{TO} \quad (1.48)$$

Subtracting I_2 from I_1 gives

$$I_o = 4\sqrt{KI}V_{in} \quad (1.49)$$

The transfer function in principle is perfectly linear and a high ac transconductance is easily obtained.

1.3.1.4 Mono-Offset-Biased Pair (MOBP)

The Mono-Offset-Biased Pair (MOBP) [71] as shown in scheme (d) also yields a linear current. The current difference gives

$$I_o = 2KV_BV_{in} - 2KV_B(\frac{V_B}{2} + V_{TO} + V_{SS}) \tag{1.50}$$

It can be noted that a dc offset component is generated in this scheme. Linearisation techniques which adopt this method are complicated by the need to eliminate the offset component.

1.3.1.5 Grounded-Source Transconductor Element (GSTE)

Scheme (e) employs a grounded non-saturated transistor as a transconductive element [75]. Using Eqns (1.6) and (1.7), the drain current for the Grounded-Source Transconductive Element (GSTE) is obtained as

$$I_{ds} = 2K[V_{in}V_K + (V_C - V_{TO})V_K - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B}})V_K^2 + \frac{\gamma}{24\phi_B^{\frac{3}{2}}}V_K^3] \tag{1.51}$$

This scheme also generates a dc offset but the transconductance is controllable via V_K. This is in contrast to previous schemes in which the bias current I is used to control the transconductance. One further requirement of this technique is that the controlling direct voltage source must have a sourcing/sinking capability. This requires the voltage source to have a low internal resistance. The saturation and non-saturation based techniques described above constitute the operating principles for most published transconductor circuits.

1.3.2 Discussion of Published Transconductor Circuits

The first generation of fully integrated 'OTA-C' analogue filters were implementated using bipolar-JFET [44] or bipolar [45],[46] technologies, in which each resis-

tor R was replaced by the well-known Long-Tail Pair (LTP) operational transconductance amplifier. One of the most important feature of the LTP is its applicability to high-frequency design [80]. Unfortunately, as has been shown, its inherently nonlinear characteristics restrict the input swing to a small range. The input characteristic of an LTP can be improved using the source-degeneration techniques [44],[49] of Fig. 1.13(a). In order to implement a single LTP source-degenerated circuit, Tan [44] and Peterson et al. [49] made use of an active transistor element at the expense of reducing the common-mode range of the LTP. The observed reduction of common-mode range is due to the voltage drop across the active resistor. Transconductors with alternative source-degenerated architectures [50]→[53] have been employed, but exhibit linear $v \sim i$ conversion only if balanced inputs are available. Fig. 1.14 shows a balanced source-degenerated transconductor. In addition to these circuits, linearisation schemes based on multiple LTP's such as the series-connected LTP [47] and regeneration structures [47],[55],[56] have emerged as alternative techniques for extending the linearity. Fig. 1.15 shows some multiple-LTP based schemes. The fundamental series-connected LTP achieves linearisation without employing source-degeneration elements. As shown in Fig. 1.15(a), the voltage v_c generated at the mid point, of the series-connected LTP [47] is a common-mode signal. Thus, only one half of the input signal is applied to the individual LTP's. Using Eqn (1.46), the output current becomes

$$I_o = I_1 - I_2 = \sqrt{KI} V_{in} \sqrt{1 - \frac{K V_{in}^2}{16I}} \qquad (1.52)$$

The transconductance is reduced to half of that for the standard LTP but the nonlinearity is reduced by a factor of four. Fig. 1.15(b) shows the schematic for a regeneration-based transconductor [55]. The input signal drives a p-channel differential pair to produce the ac currents. When these currents flow through

another series-connected LTP, two scaled voltages are generated:

$$V_x = V_C + \sqrt{\frac{K_3}{K_5}} V_{in} \quad (1.53)$$

and

$$V_y = V_C - \sqrt{\frac{K_3}{K_5}} V_{in}, \quad (1.54)$$

where K_3 and K_5 are the transconductances of the p-channel LTP transistor and n-channel series LTP transistor, respectively. Under the assumption that $K_1 = K_2 = K$, the difference of the currents I_1 and I_2 becomes

$$I_o = 4K(V_C - V_{TO}) \sqrt{\frac{K_3}{K_5}} V_{in} \quad (1.55)$$

The price paid for this improved linearity is a reduced input signal swing and reduced tunability because the stacked structure requires higher supply voltages to maintain the transistors operating in the saturation region.

The interesting proposition has been advanced [58] that the devices in an LTP can be linearised using small-dimension devices under high gate-overdrive conditions. For a saturated small-dimension device, with mobility dependence on both normal and tangential fields, the drain current is given in Appendix E by

$$I_d = \frac{K_{oc}}{[1 + (\theta + \alpha)(V_{gs} - V_t)]} (V_{gs} - V_t)^2 (1 + \frac{\Delta L}{L}) \quad (1.56)$$

where the symbols are defined in the Appendices A and E. It should be mentioned that the change of channel length ΔL is a function of v_{ds}. This is an alternative representation of the channel-length modulation effect. If the channel length L and gate oxide thickness t_{ox} are decreased, θ and α are increased. If $(V_{gs} - V_t)$ is made large, then the product of $(\theta + \alpha)(V_{gs} - V_t)$ is greater than 1. Under such a condition, the drain current is approximated as

$$I_d \approx \frac{K_c}{(\theta + \alpha)} (V_{gs} - V_t)(1 + \frac{\Delta L}{L}) \quad (1.57)$$

The square-law behaviour of drain current is thus transformed into a linear function. As the devices are designed with small dimensions, problems such as channel-length modulation, device mismatches and hot electron effect etc. degrade the distortion performance. An alternative LTP-based circuit has been proposed [59] which is based on the traditional feedback technique for operational amplifers. However, although the circuit exhibits excellent linearity, it is not tunable.

Nedungadi et al. [60],[61] developed a Compensated Common-Source Pair (CCSP) transconductor based on the LTP linearised in the current domain. Fig. 1.11(b) illustrates their basic technique in schematic form. This structure implements the required tail-current function by injecting the long-tail pair with a compensating current which is proportional to the square of the input signal. Bult et al. [62] employed the same technique on their transconductor design but the stacked structure limits the signal-handling capability and tunability.

The introduction of the Cross-Coupled Pair (CCP) by Viswanathan [65] represents an important linearisation technique for single-ended applications. An implementation of Fig. 1.13(c) can be obtained by means of two shunt-feedback buffers for cross-coupling signals to the sources of the transistor pair. Many authors [66]→[68] have adopted similar strategies but with differing implementations. The CCP enjoys the advantage of a high transconductance gain but the signal-handling capability of the transconductor is restricted because of the saturation requirement of both the current source/sink and transistor pair.

Wang [70]→[72] has recently proposed an Offset-Biased Double Pair (OBDP) based on the MOBP technique as described in Fig. 1.13. The proposed transconductor is shown schematically in Fig. 1.16.

If v_{gs1} and v_{gs2} are the gate-to-source voltages of M1 and M2, then $v_{gs3} = v_{gs1} -$

V_B and $v_{gs4} = v_{gs2} - V_B$. Applying the square-law characteristics to transistors M1 to M4, the output currents are

$$I_1 = I_{d1} + I_{d4} = K(v_{gs1} - V_{TO})^2 + K(v_{gs2} - V_B - V_{TO})^2 \quad (1.58)$$

and

$$I_2 = I_{d2} + I_{d3} = K(v_{gs2} - V_{TO})^2 + K(v_{gs1} - V_B - V_{TO})^2 \quad (1.59)$$

The differential output current is

$$I_o = I_1 - I_2 = 2KV_BV_{in} \quad (1.60)$$

Since the sum $I_1 + I_2 = 2I$, the branch currents are

$$I_1 = I + KV_BV_{in} \quad (1.61)$$

and

$$I_2 = I - KV_BV_{in} \quad (1.62)$$

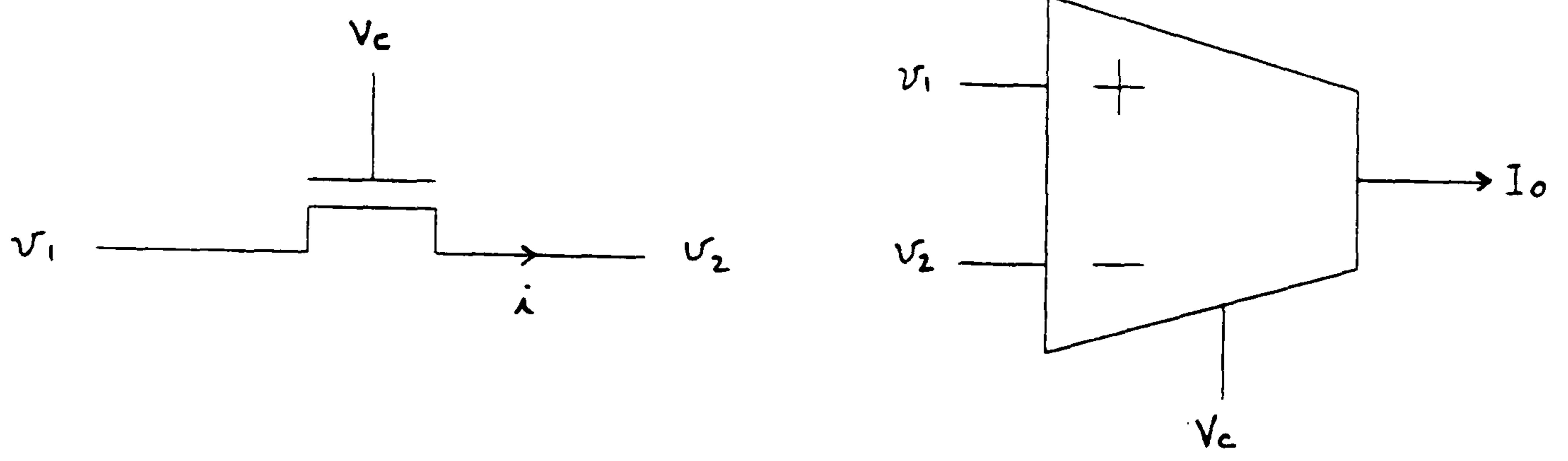
As in the LTP or SDP, each branch current is independently linearised. The main disadvantage is that the stacked structure limits the tunability. Czarnul el al. [73] have suggested a modification replacing the current source with a negative impedance convertor (NIC) as shown in Fig. 1.17. For the modified arrangement, the bias current is $I_C = I_{d1} + I_{d2} - I_{d3} - I_{d4}$. The branch currents are $I_1 = I_{d1} + I_{d2}$ and $I_2 = I_{d3} + I_{d4}$. The NIC maintains a virtual short between points A and B but draws equal currents into its terminals. Given these conditions, the transfer function becomes

$$G_m = \frac{dI_o}{dV_{in}} = \frac{d(I_1 - I_2)}{dV_{in}} = \frac{I_C}{V_B} \quad (1.63)$$

The resulting structure is independent on K provided both control variables I_C and V_B are defined externally. However, the problem of tunability remains unsolved. The tunability of the OBDP circuit has been extended [74] by connecting

the OBDP sources to a negative supply. However, this approach leads to very large steady-state power consumption in comparison with other schemes.

A Grounded-Source Triode Pair (GSTP) has been proposed by Pennock [75] as an alternative to conventional saturation-based LTP input stages. The basic operating principle is based on Fig. 1.13(e) but the single transistor is replaced by a pair of transistors operating in a fully balanced mode which reduces the input signal across each transistor, further improving the linearity in the presence mobility degradation. In order to reduce the internal resistance, Pennock adopted the shunt-feedback voltage source. Since this scheme uses current differences, the offset components are eliminated. Other authors [76]→[78] followed a similar strategy to implement their transconductors. All designs achieve high linearity combined with a wide range of tunability. The structures [75],[78] are somewhat sensitive to parasitics at the outputs of the transconductor because they rely on complicated common-mode design. A further disadvantage is that a regulated supply circuit is required to control the tuning in [76] and complex biasing circuitry in [78]. These schemes increase the design burden when compared to saturation transconductor schemes.



(a) MOS resistor symbol (b) MOS transconductor symbol

Figure 1.1: MOS resistor and transconductor symbol

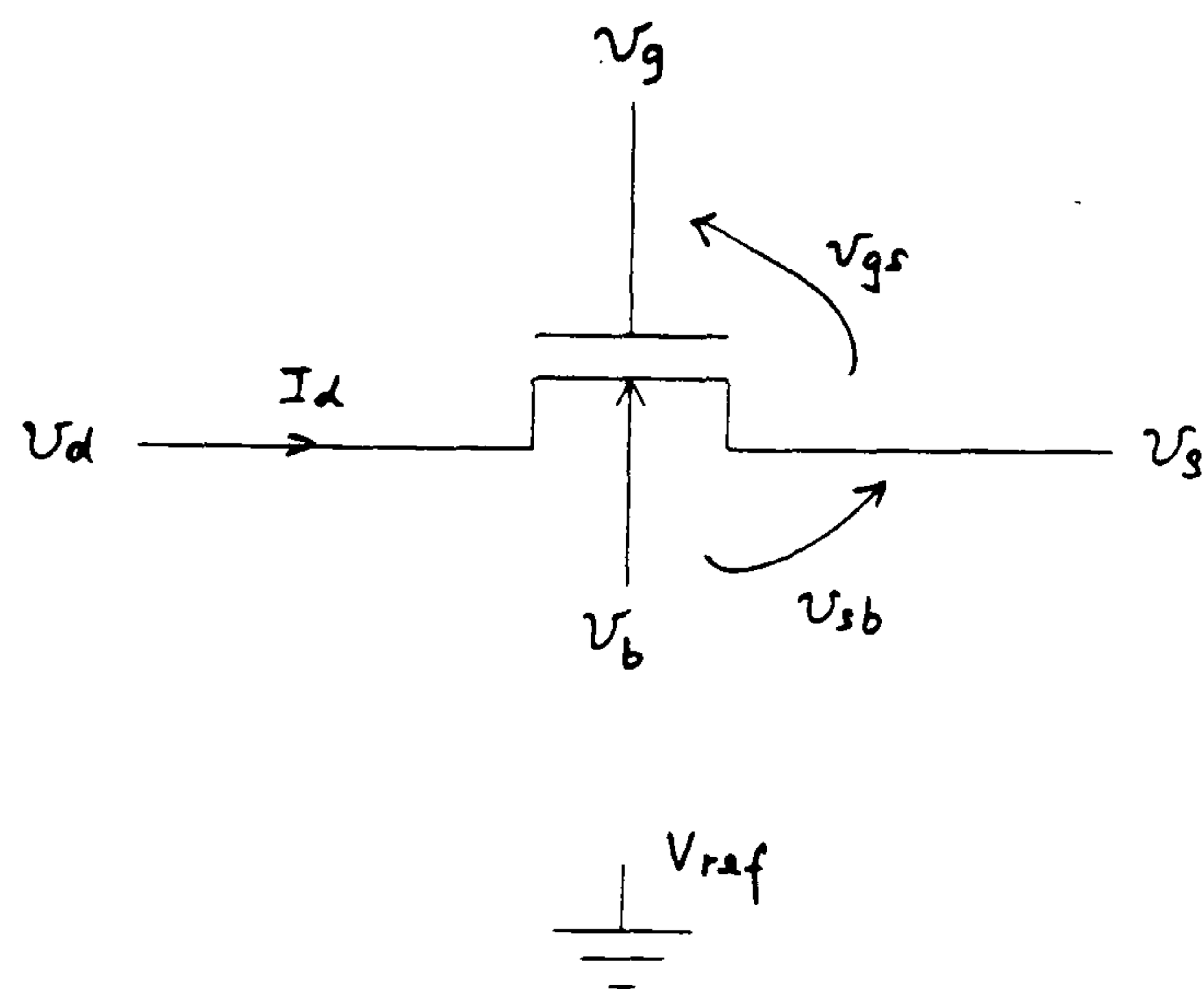


Figure 1.2: Notation for NMOS resistor/transconductor elements

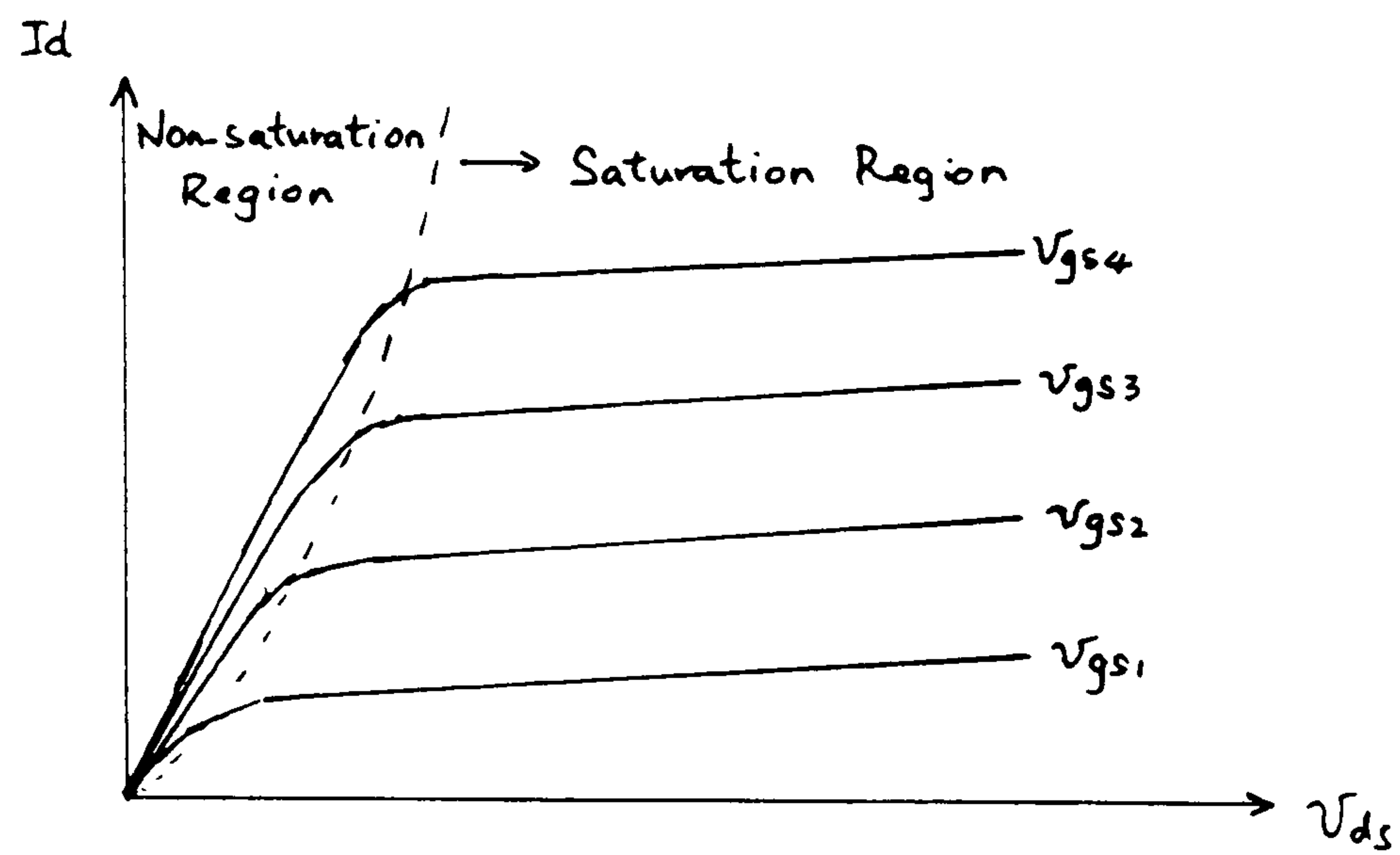


Figure 1.3: Typical output characteristics for an NMOS transistor

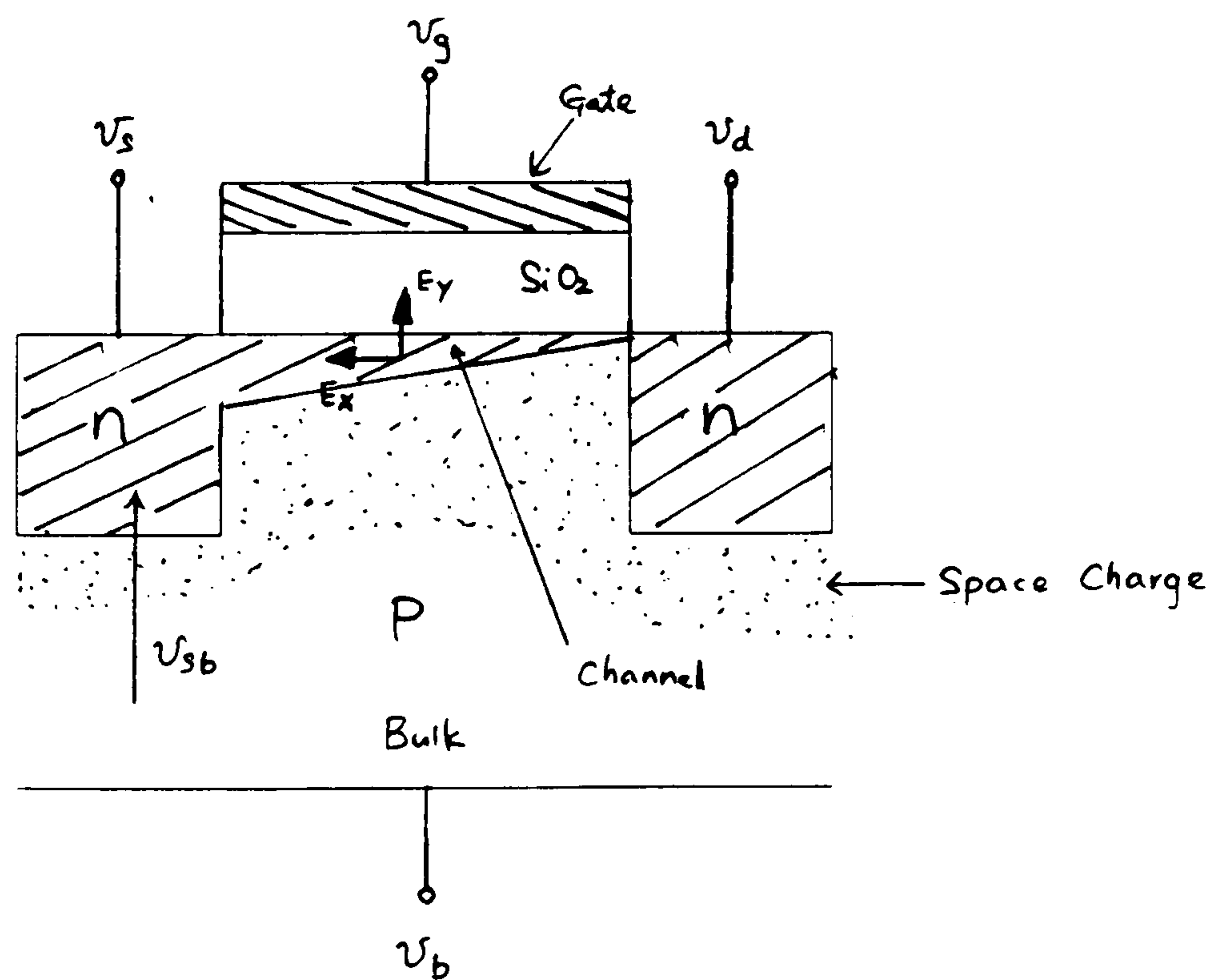
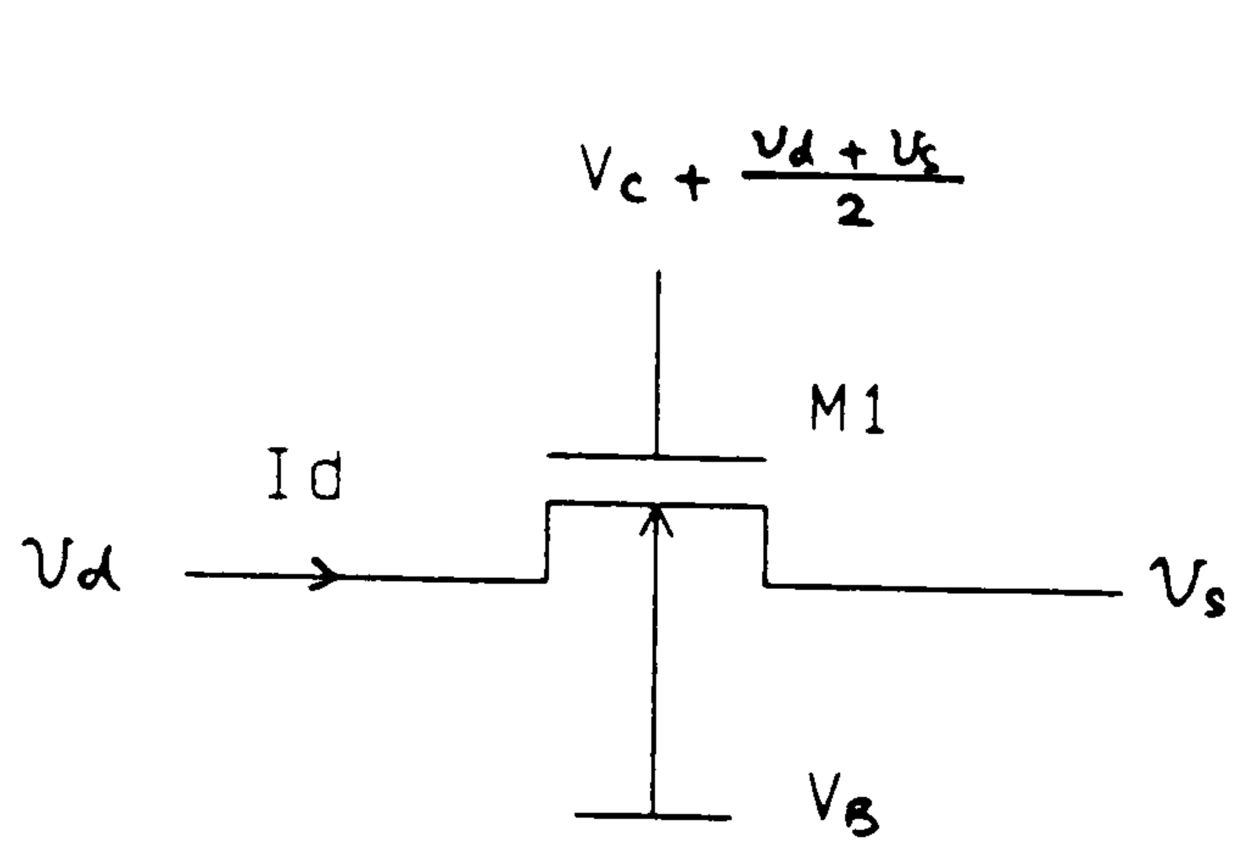
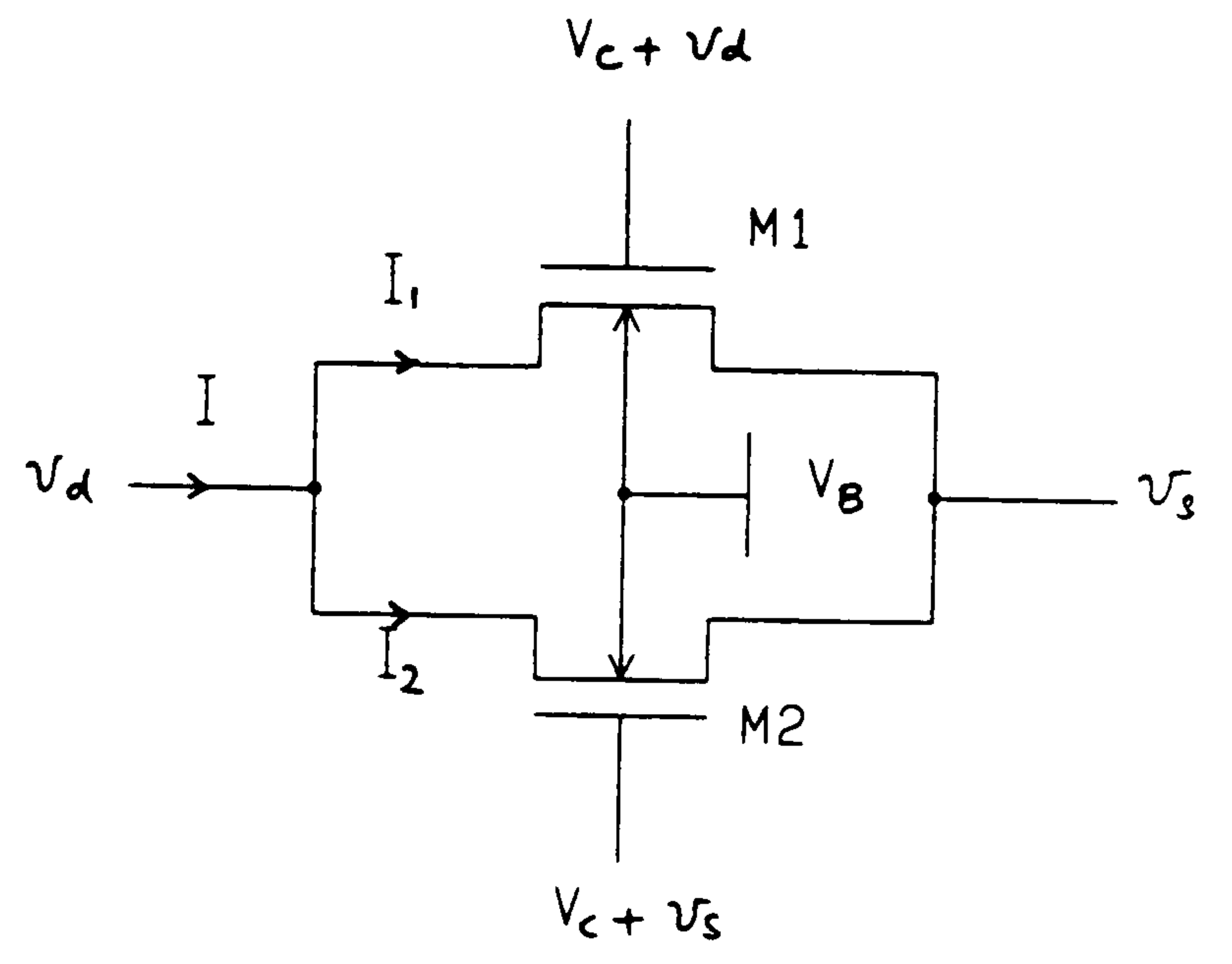


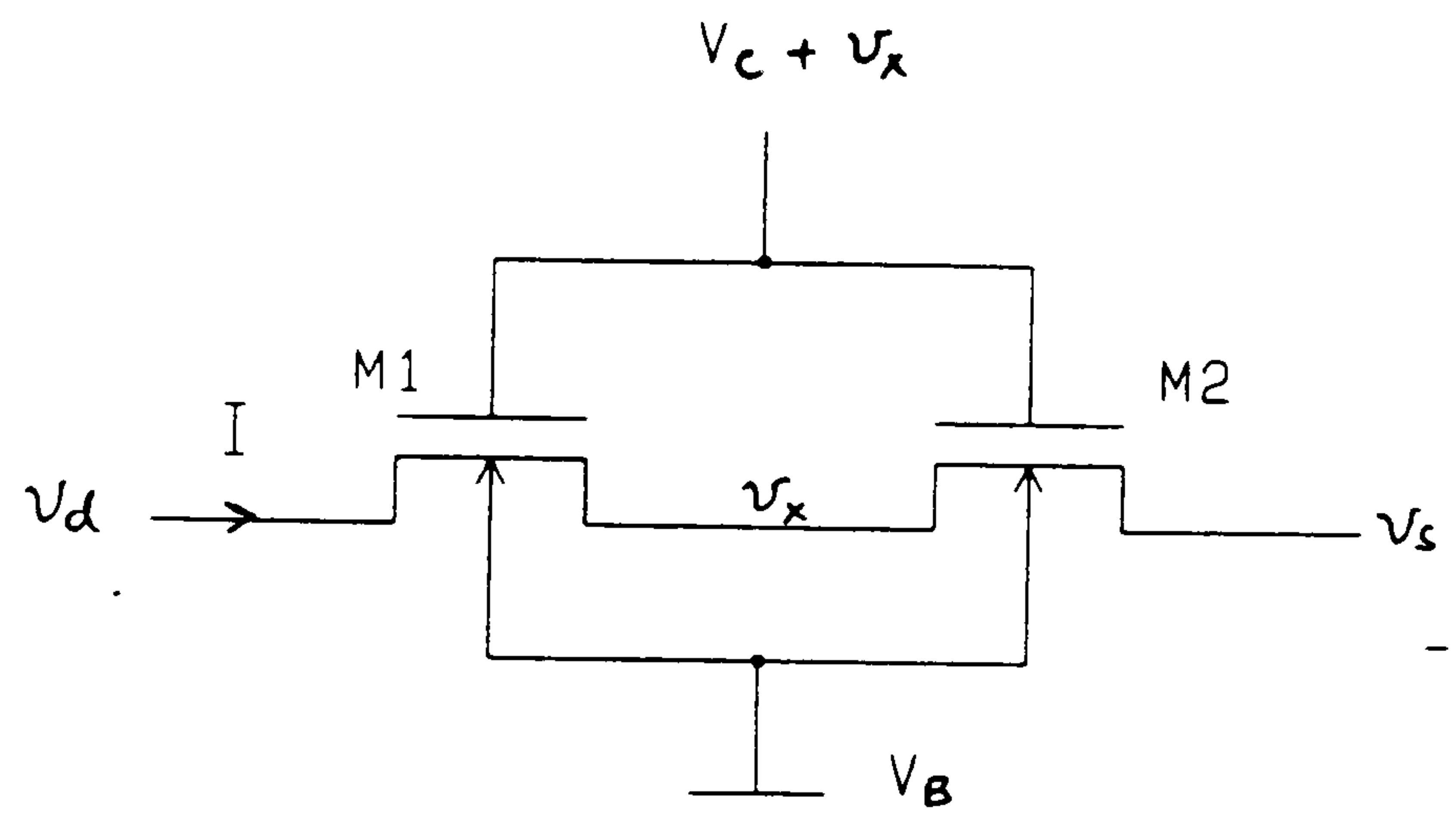
Figure 1.4: Normal and lateral electric field



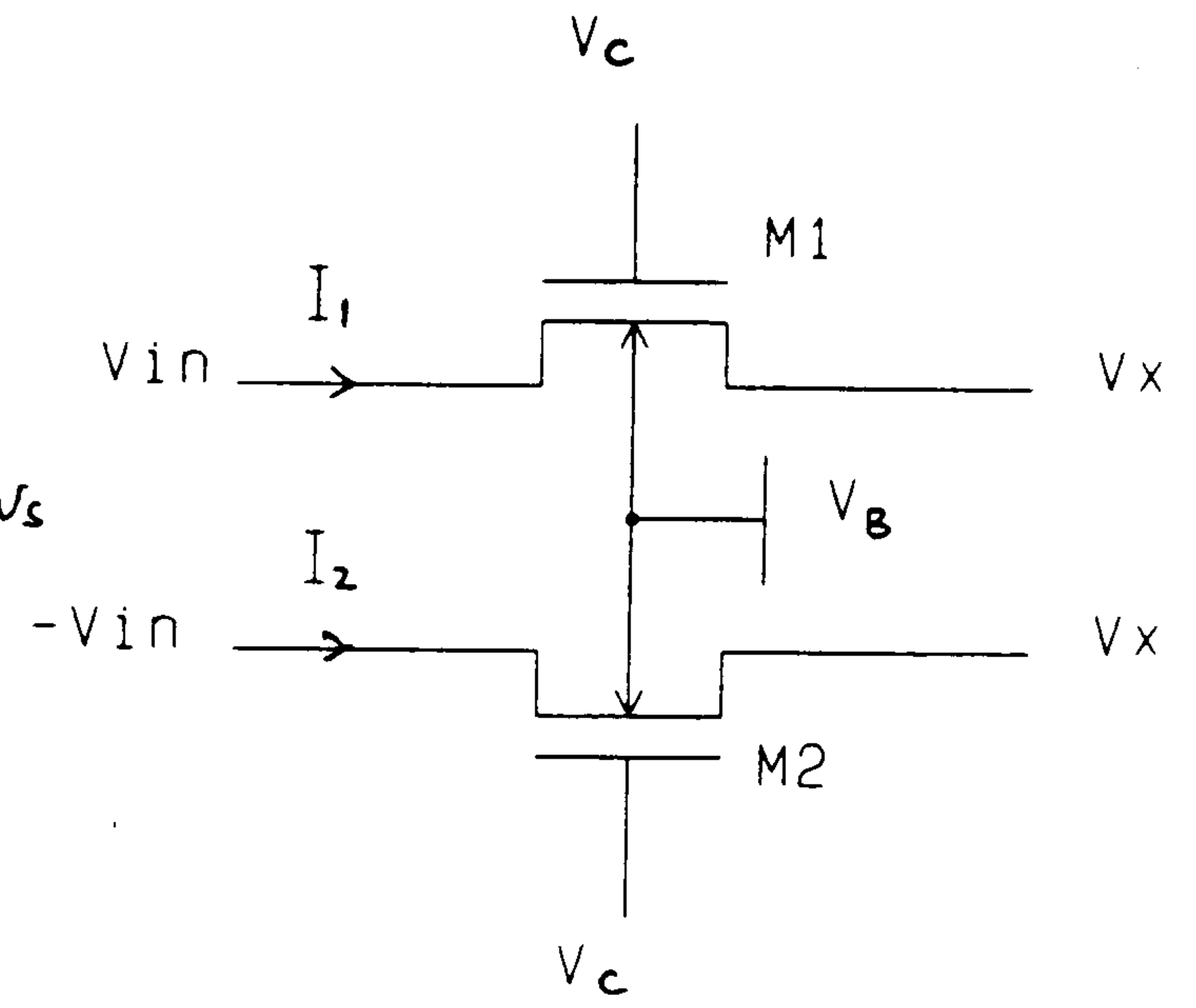
(a) STR



(b) PFR



(c) SPR



(d) DPR

Figure 1.5: Resistor linearisation schemes

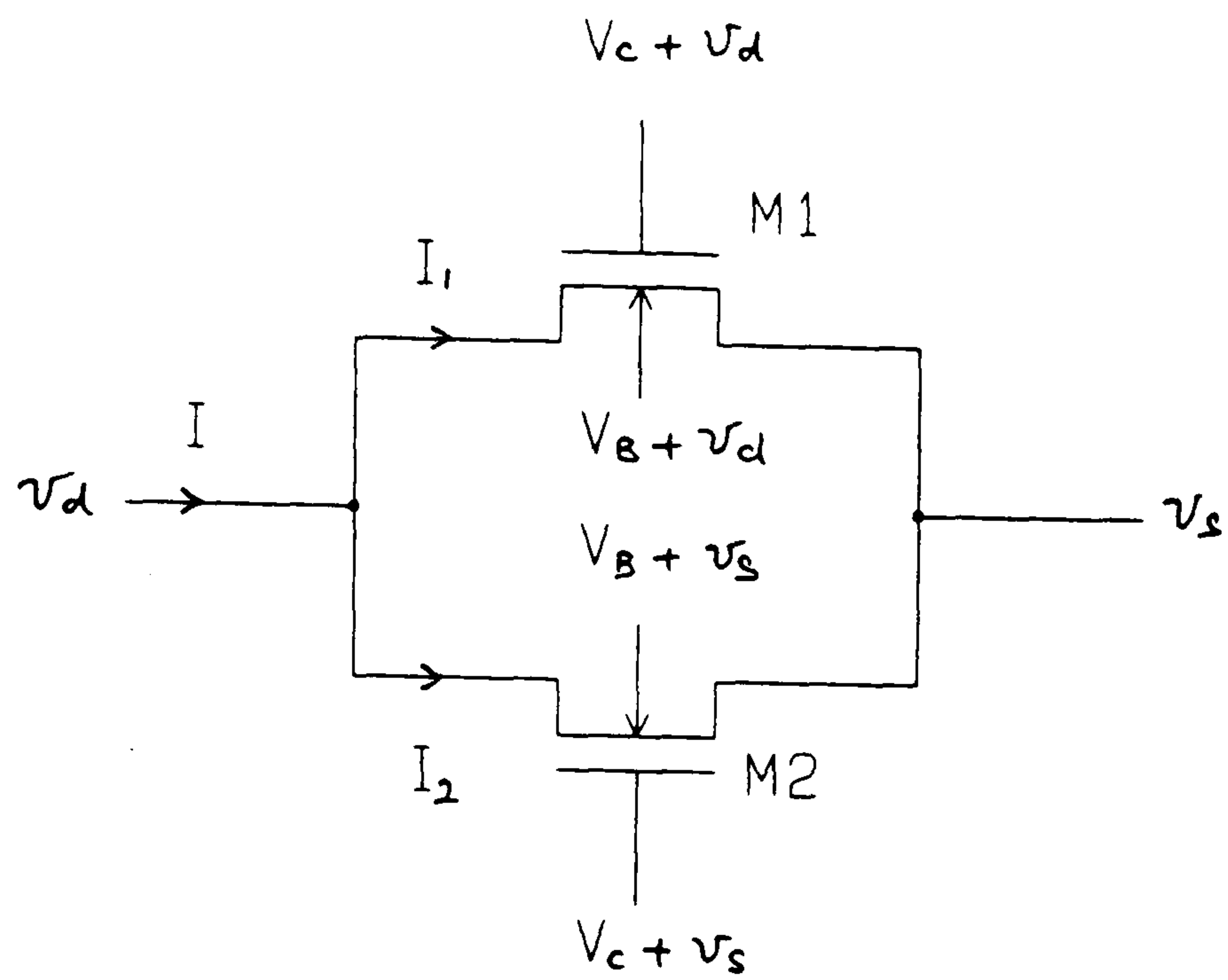


Figure 1.6: Dual gate-bulk compensation PFR

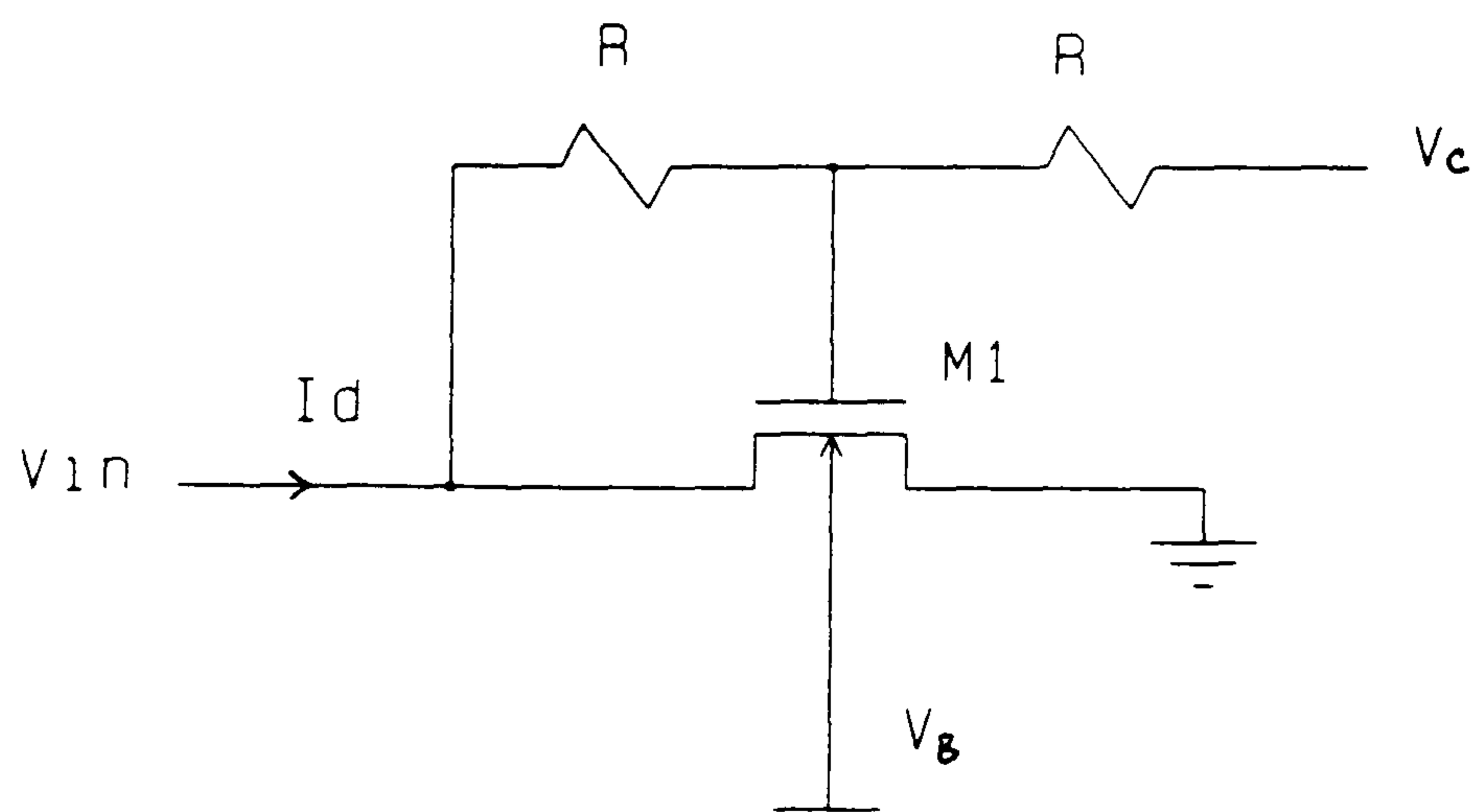


Figure 1.7: Shunt-feedback grounded resistor (SFGR)

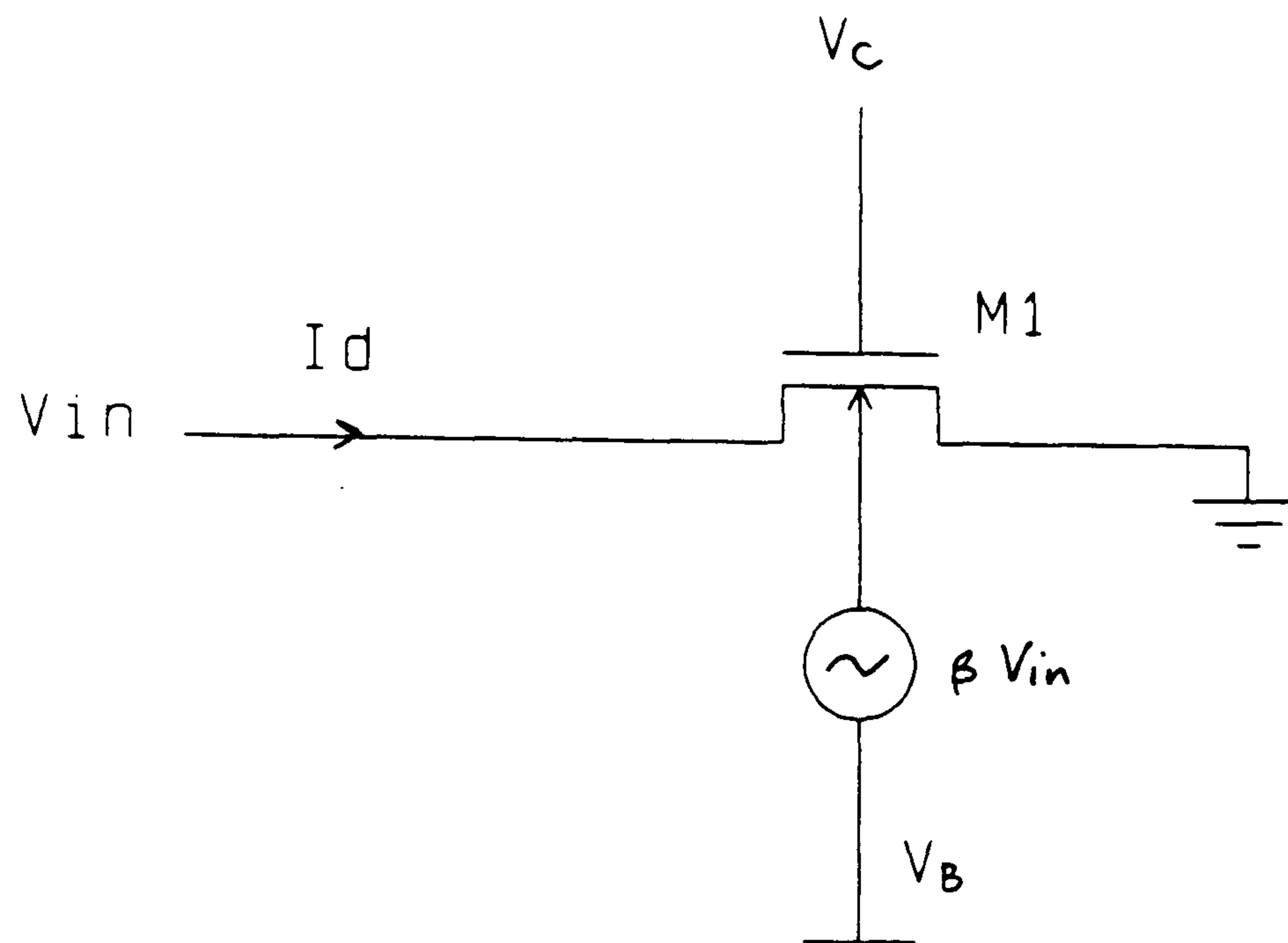


Figure 1.8: Body-driven grounded resistor (BDGR)

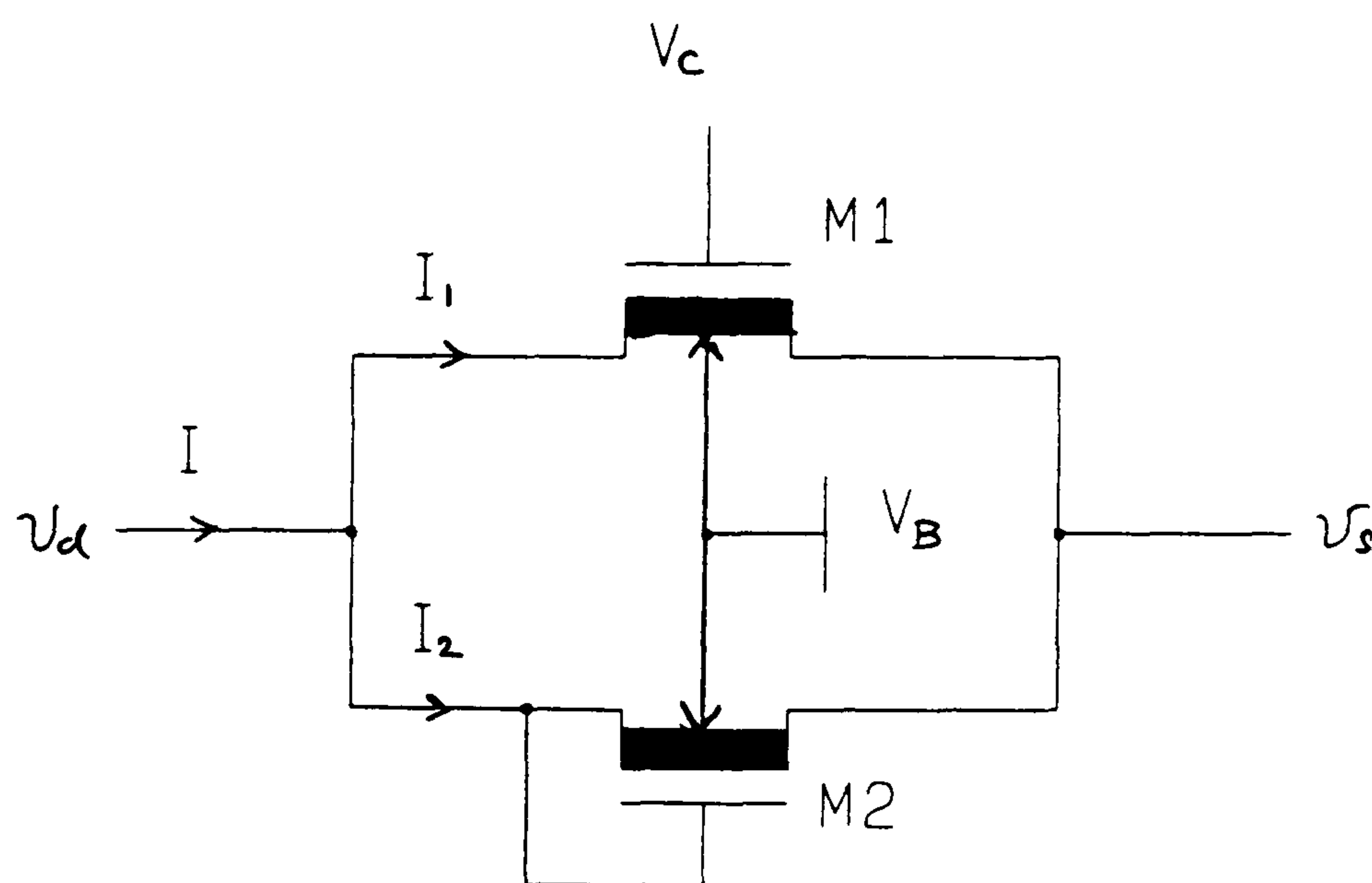


Figure 1.9: Depletion-mode parallel-form resistor structure

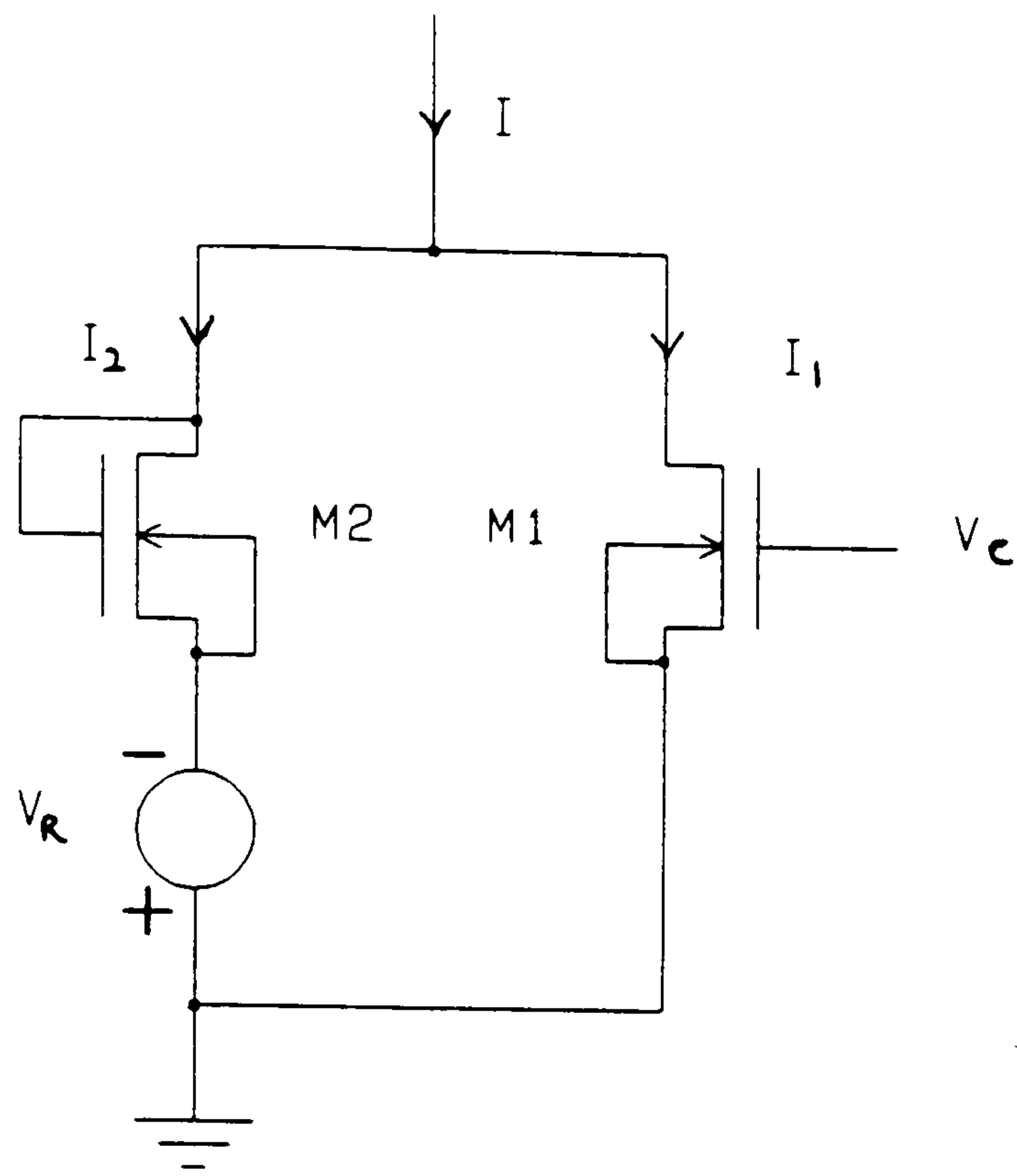


Figure 1.10: Alternative parallel-form resistor structure

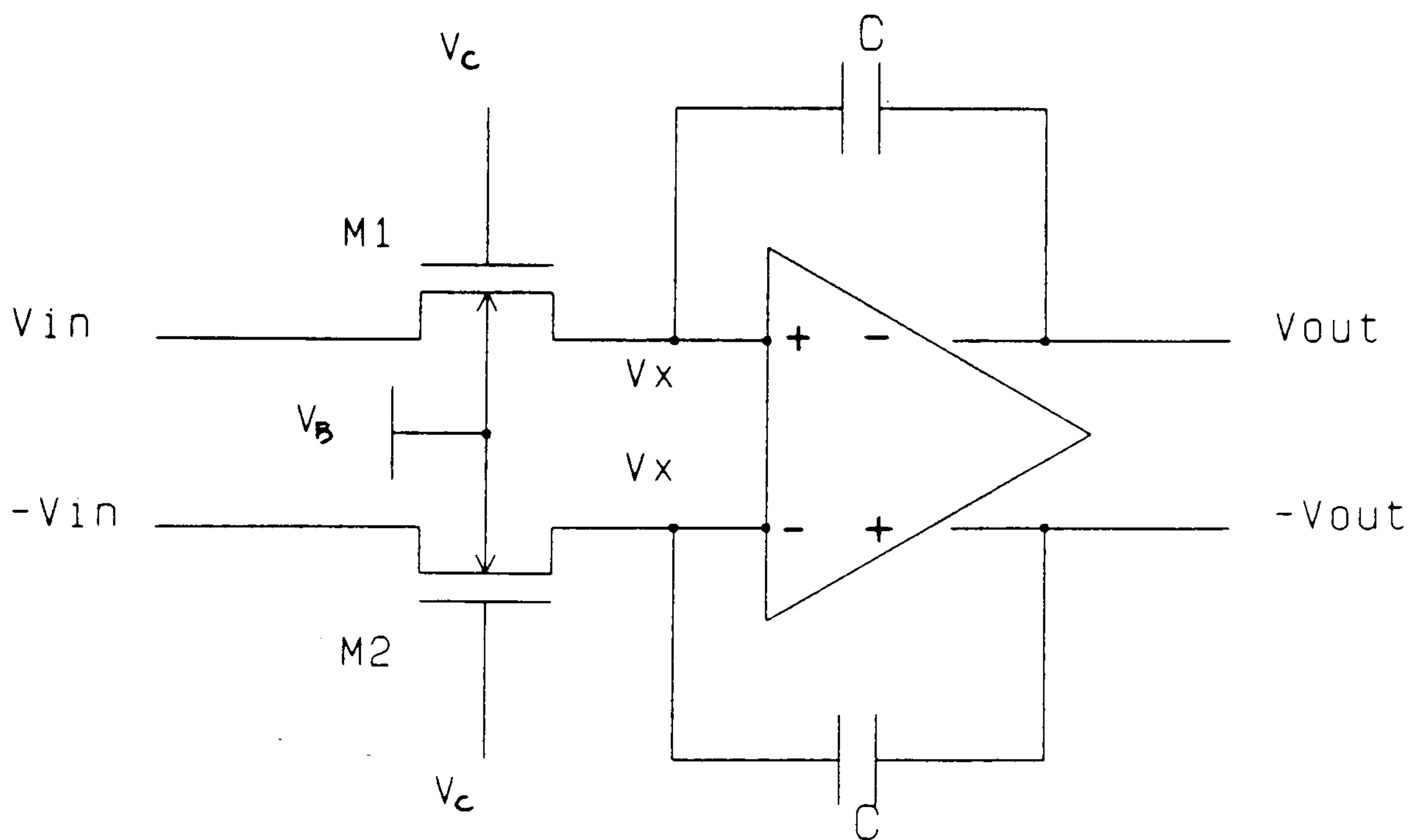


Figure 1.11: DPR-based balanced integrator

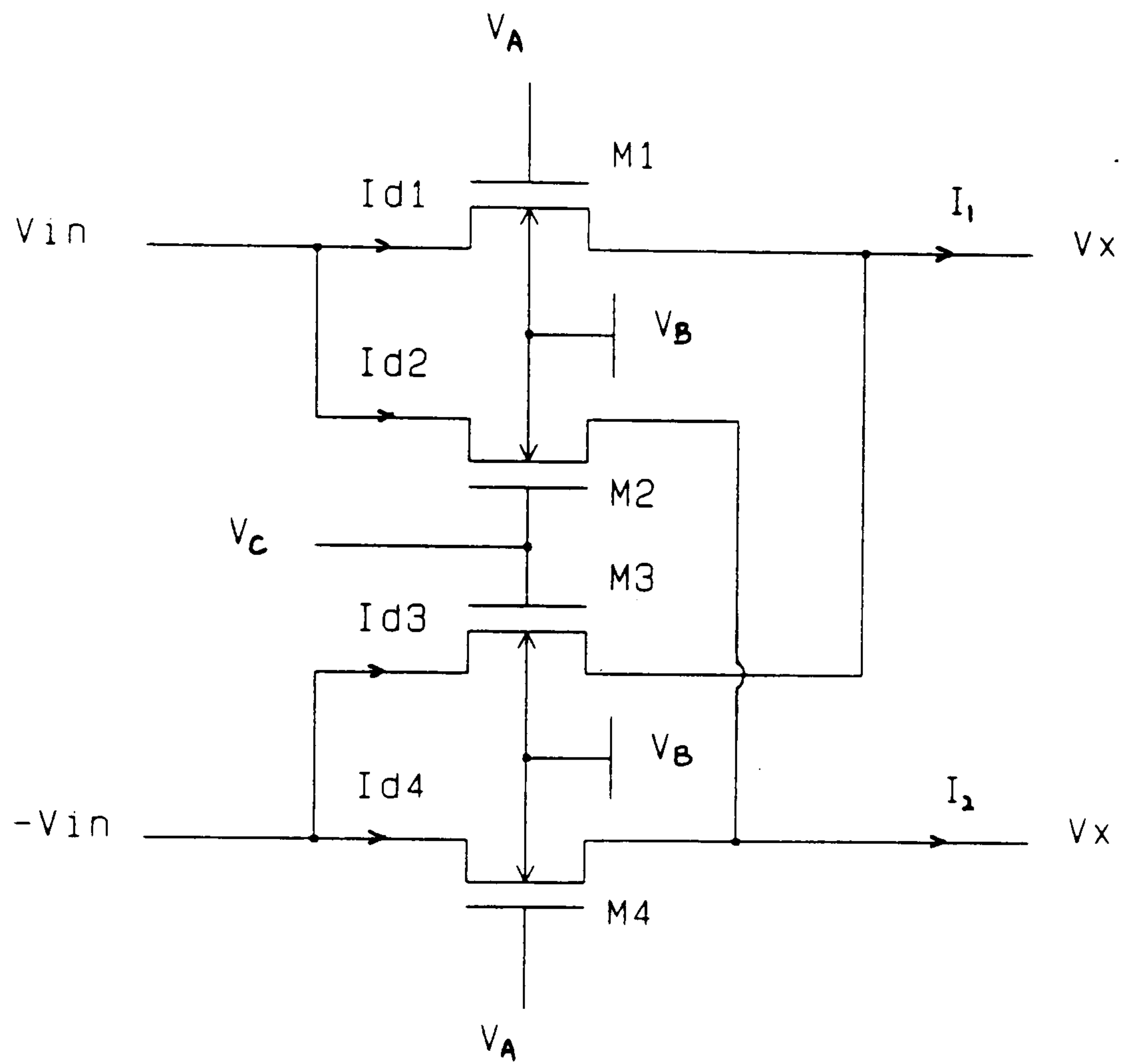


Figure 1.12: Four-transistor DPR

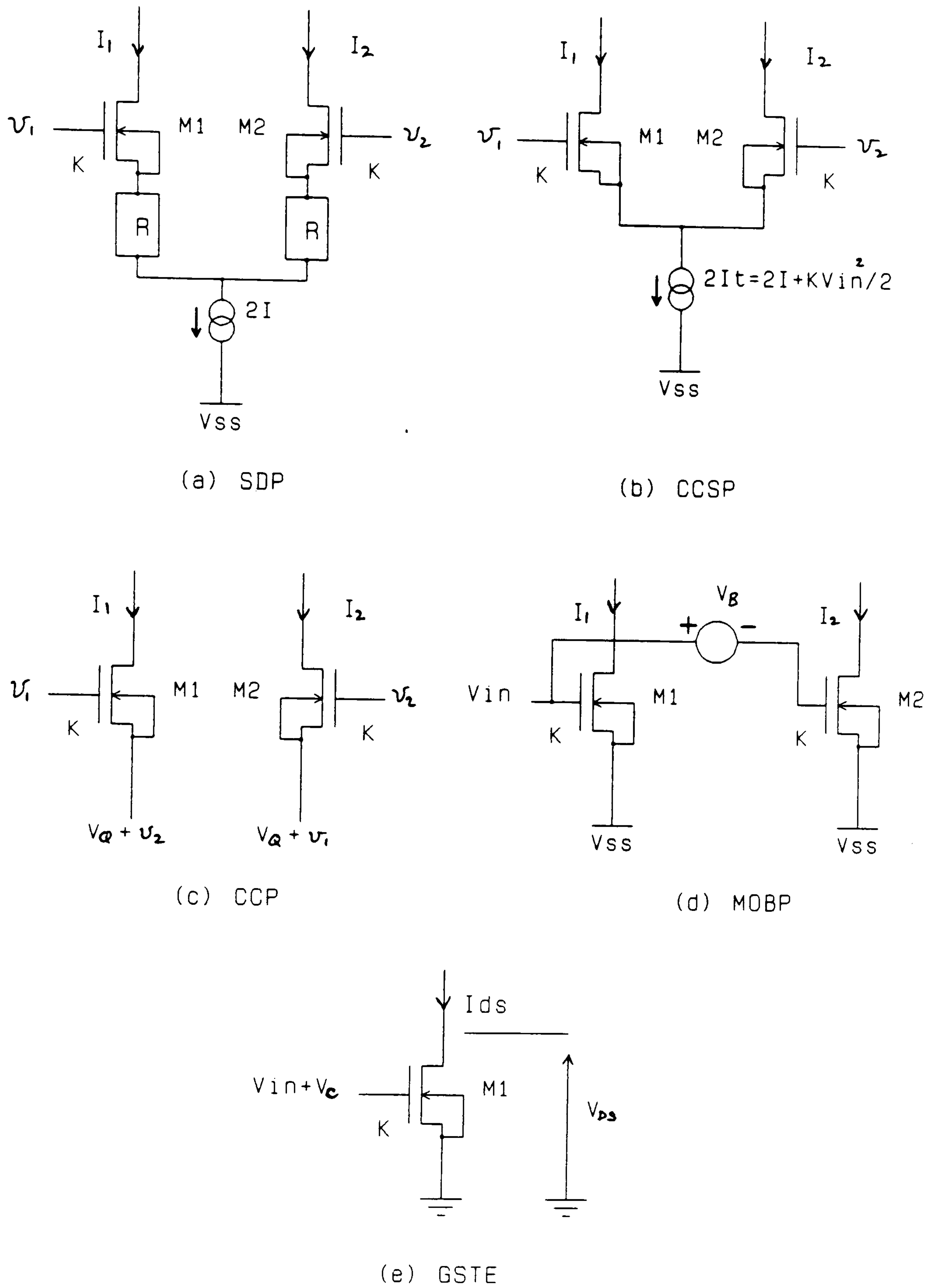


Figure 1.13: Transconductor linearisation schemes

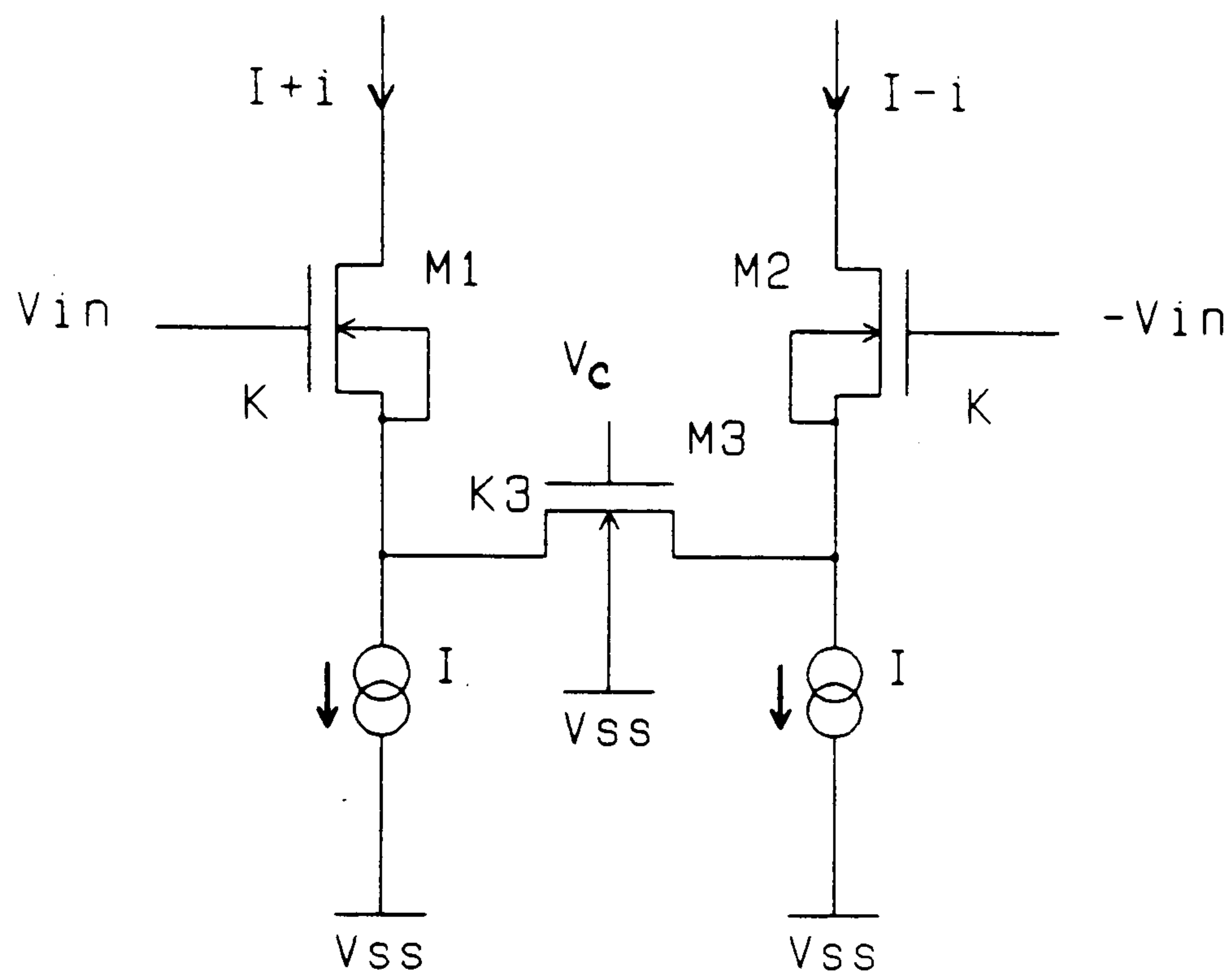
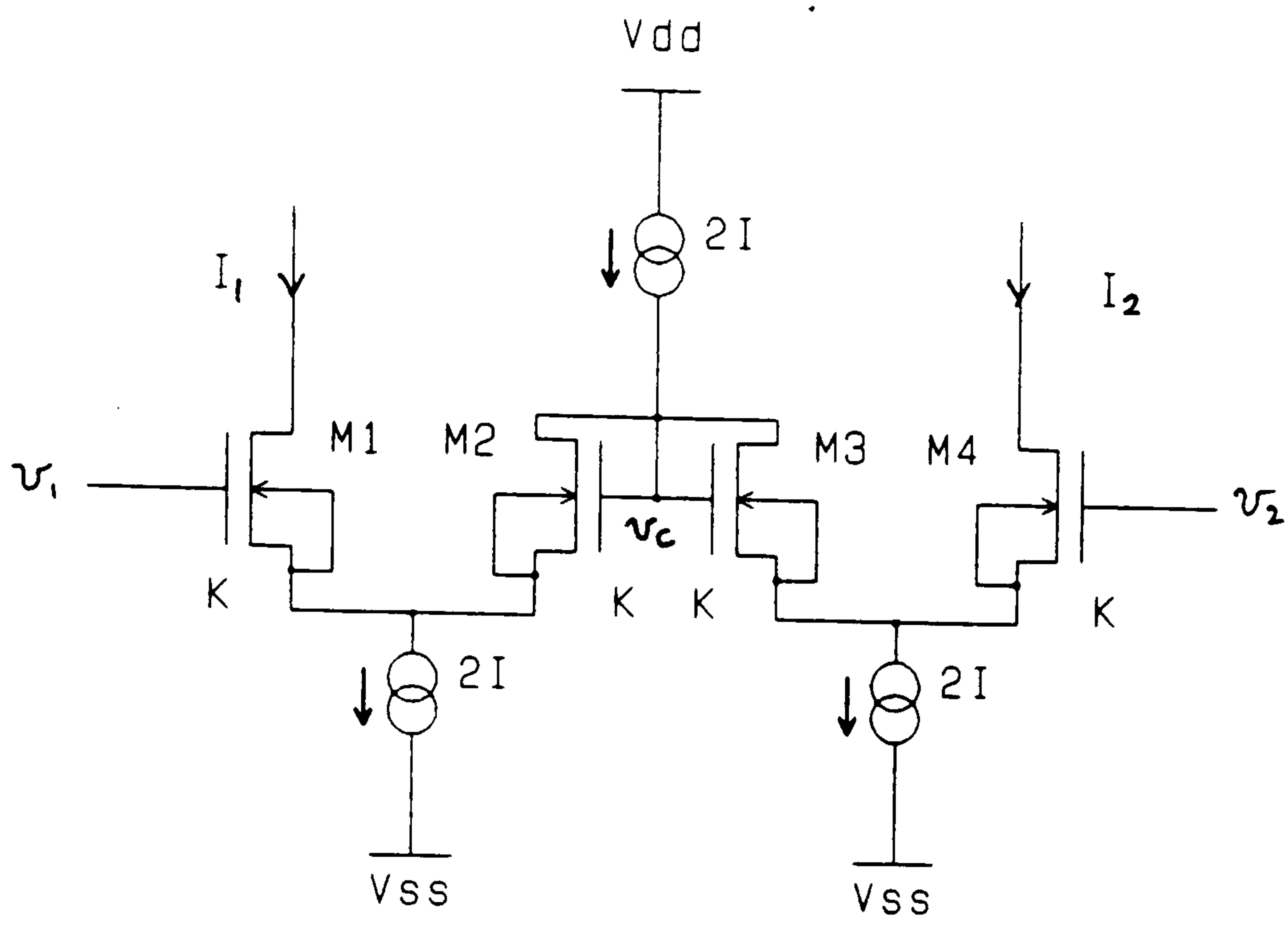
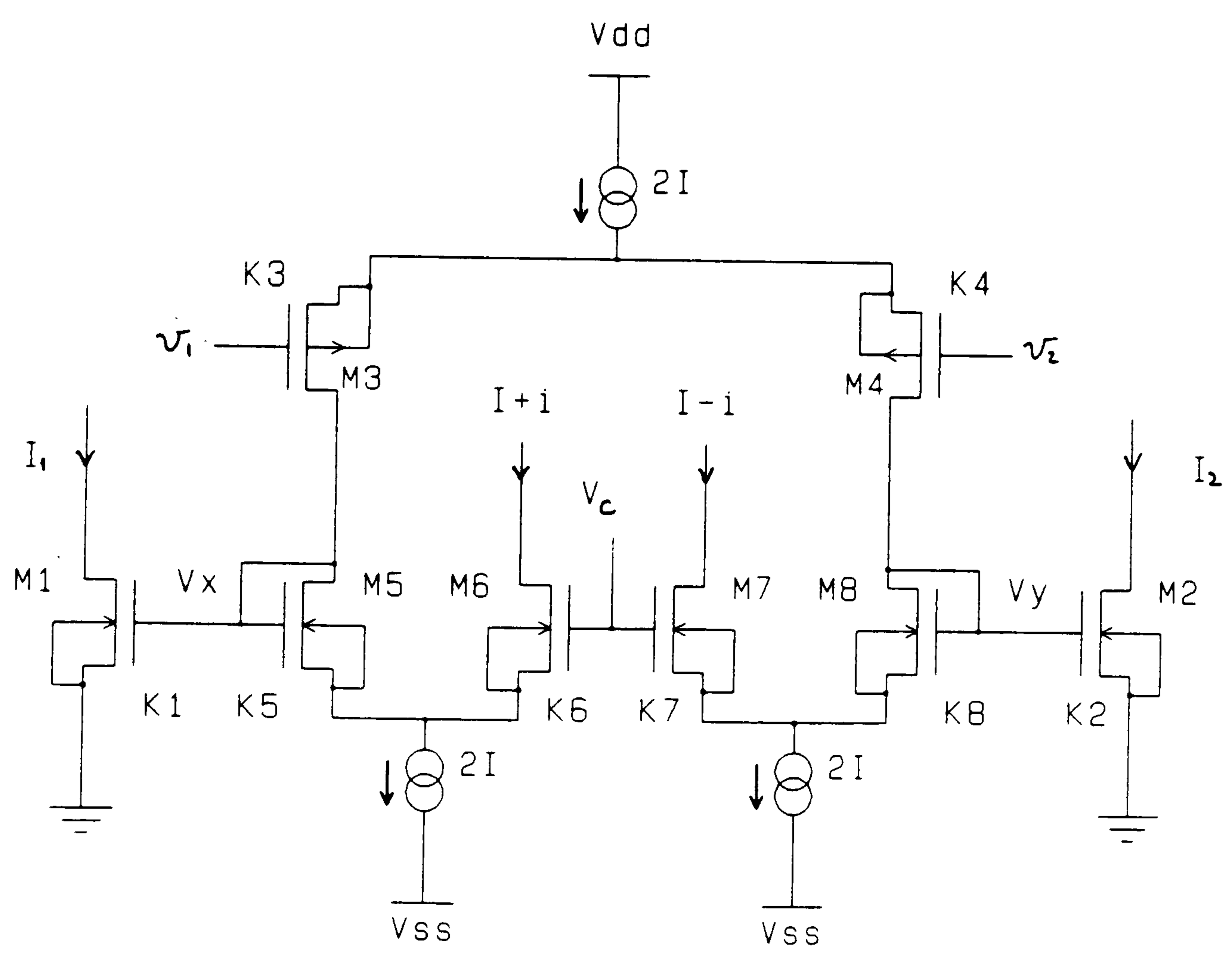


Figure 1.14: Balanced source-degenerated transconductor



(a) Series-connected LTP



(b) Transconductor using regeneration approach

Figure 1.15: Multiple differential-pair-based linearisation schemes

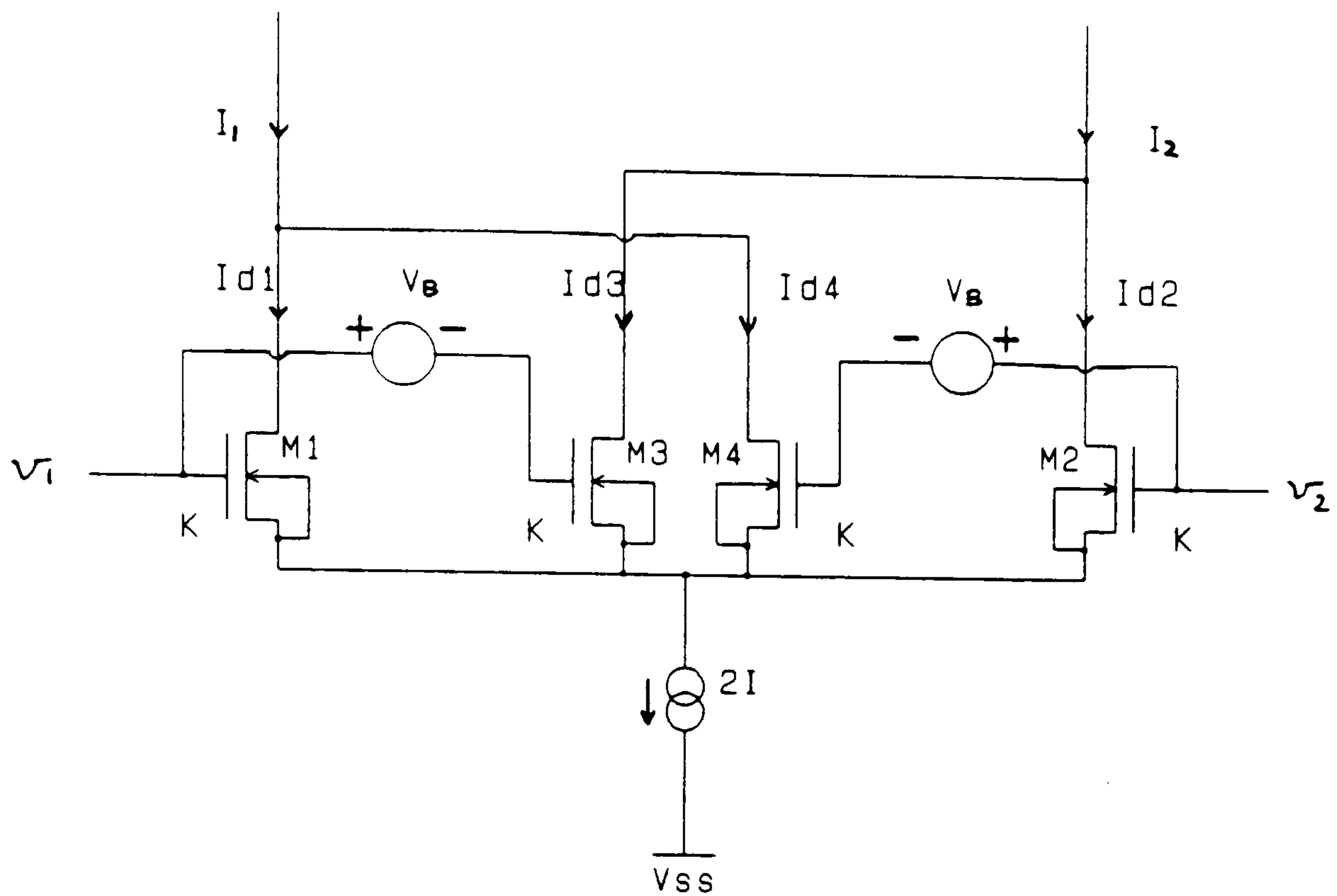


Figure 1.16: Current-source-based OBDP transconductor

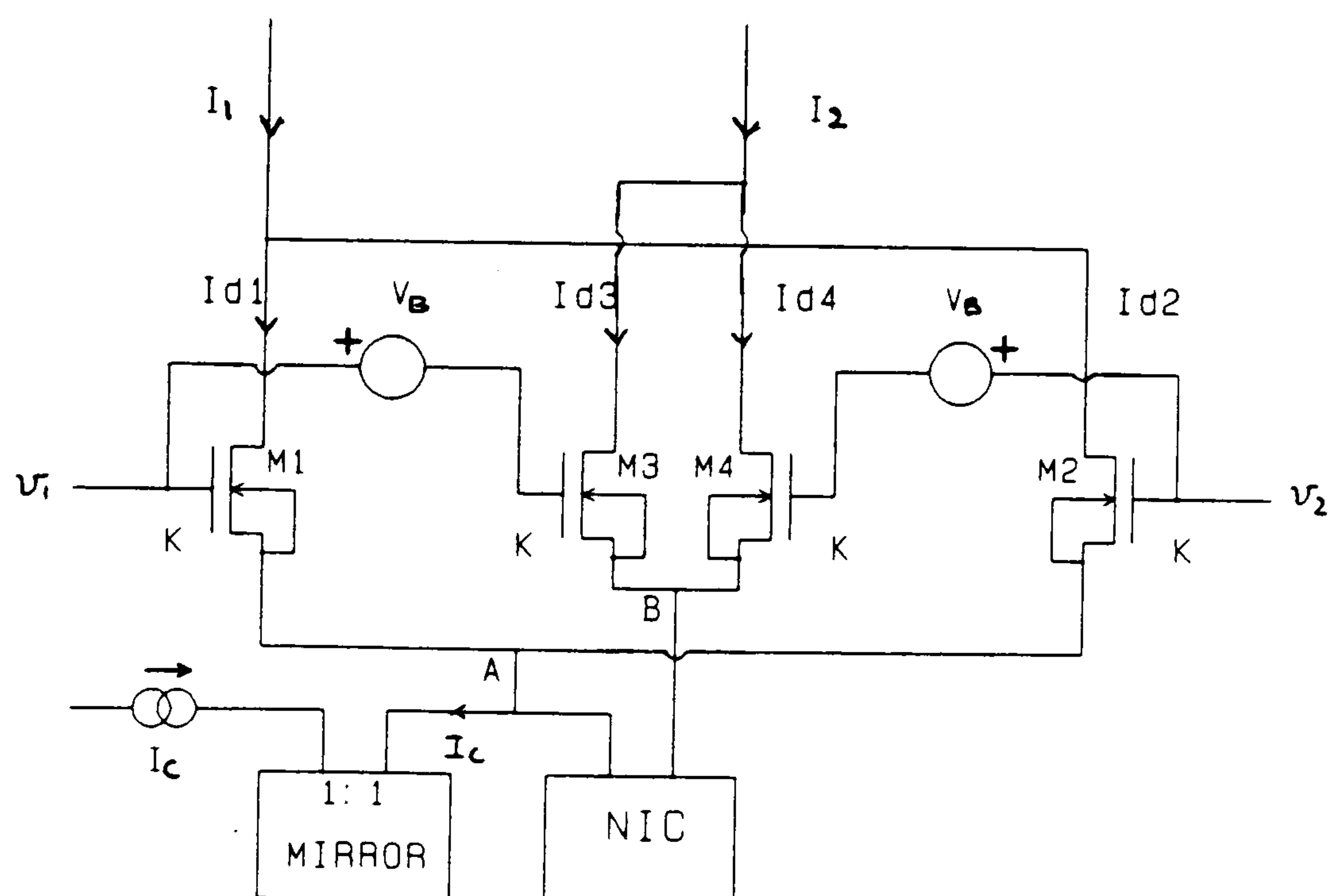


Figure 1.17: OBDP transconductor based on Negative Impedance Convertor

Chapter 2

Fully Integrated MOS Resistors

In this chapter, it is shown that a family of CMOS resistors can be developed based on building blocks consisting of a single buffered transistor operating in the linear region. Linearization techniques such as unscaled-gate compensation and dual gate-bulk compensation are described for a range of resistive structures involving parallel, series and series-parallel configurations. The problems of the parallel-form [8]→[15] and series-form resistors [16]→[18] as discussed in Chapter 1 are highlighted, and a solution to this via series-parallel form resistors [19] is described. In addition, scaled-gate compensation leads to two alternative resistors [7] : a single-device-based resistor and a double-device-based parallel-form resistor. However, the overall objective is to examine how the linearity of individual resistors is affected by various techniques using different terminal coupling arrangements. The manner in which the new structures [7],[19] together with other proposed circuits improve on previously published circuits [3]→[6],[8]→[18] is investigated. More importantly, analytical expressions and their implications are discussed. The impact of second-order effects on the resistors is also considered. Finally, the application of these resistors in continuous-time filters is described.

2.1 MOS Resistor Synthesis Elements

Linear floating resistors can be constructed using two basic elements: MOS transistors and buffers. Elementary combinations of the two building blocks are shown in Fig. 2.1. The structure of Fig. 2.1(a) is termed as a Terminal-Coupled Resistor Type I (TCR-I) and the Fig. 2(b) arrangement as a Terminal-Coupled Resistor Type II (TCR-II).

Unless otherwise stated, it will be assumed throughout this chapter that the MOS transistor has constant mobility and the drain current (Eqn (1.6)) is given by the second-order approximation

$$I_d \approx 2K[(v_{gs} - V_t)v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb}}})v_{ds}^2] \tag{2.1}$$

With $v_g = V_C + v_d$, and $v_b = V_B$, the current in TCR-I is obtained as

$$I_1 = 2K[(V_C - V_T)v_{ds} + \frac{1}{2}v_{ds}^2 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \tag{2.2}$$

where V_T is defined in Eqn (1.14) and V_C is a dc control bias. Equation (2.2) reveals that the quadratic nonlinearity has two components: the first being dependent only on v_{ds} and the second dependent on the substrate potential V_B and the bulk modulation factor γ. With $v_g = V_C + v_s$ and $v_b = V_B$, the drain current expression for TCR-II is

$$I_2 = 2K[(V_C - V_T)v_{ds} - \frac{1}{2}v_{ds}^2 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \tag{2.3}$$

It should be noted that neither TCR-I nor TCR-II is useful as a resistor because the quadratic terms produce relatively high levels of distortion. However, it should be noted that the currents in (2.2) and (2.3) contain anti-phase quadratic terms but co-phasal gamma-related quadratic terms. These interesting properties can be exploited to construct a family of CMOS resistors with improved linearity as described in the following sections.

2.2 MOS Resistors with Unscaled-Gate Compensation

This section describes the implementation of a buffer for use in unscaled-gate compensation of MOS resistors. Practical limitations and advantages for this group of resistors are also discussed.

As discussed in Chapter 1, unscaled-gate compensation makes use of a buffer for dc biasing and direct coupling of signal to the gate of a MOSFET. The most straightforward implementation of the buffer is that of the CMOS source follower. Fig. 2.2 illustrates the circuit diagram for a p-channel source follower. With the transistors of the p-channel source follower operating in saturation, the output voltage (see Eqn (E.16)) is

$$v_o = V_C + v_i \tag{2.4}$$

and the dc component is given as

$$V_C = V_{DD} - V'_{BIAS} = \sqrt{\frac{I'_B}{K'_B}} + V_{TOp} \tag{2.5}$$

where I'_B is the dc bias for the p-channel source follower, K'_B is the transconductance parameter of M1 and M2 (assuming two transistors have the same aspect ratio) and V_{TOp} is the threshold voltage of the p-channel transistor at zero bulk voltage. It will be appreciated that the dc control voltage: V_C, is a function of the process parameters of the p-channel transistors.

The source-follower-based TCR-I and TCR-II provide an economical basis for the synthesis of linear CMOS resistors but the buffer transistors must be of opposite type to that of the gate-coupled MOSFET. Thus, resistance is dependent on both the p-channel and n-channel process parameters.

2.2.1 Parallel-Form Resistor with Unscaled-Gate Compensation

Fig. 2.3 shows the parallel combination of a TCR-I and TCR-II denoted in a PFR [9]. Given the assumptions as in Section 2.1, the drain currents (Eqns (2.1) and (2.4)) for M1 and M2 are

$$I_1 = 2K_p[(V_C - V_T)v_{ds} + \frac{1}{2}v_{ds}^2 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \tag{2.6}$$

and

$$I_2 = 2K_p[(V_C - V_T)v_{ds} - \frac{1}{2}v_{ds}^2 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \tag{2.7}$$

where K_p and V_T represent the transconductance parameter and threshold voltage, respectively for the n-channel transistor pair in parallel form. The other symbols are as described above. Addition of the two drain currents gives

$$I_p = 4K_p[(V_C - V_T)v_{ds} - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \tag{2.8}$$

Although the major quadratic terms are cancelled, the remaining bulk-dependent quadratic term imposes a limit on the linearity. Clearly, linearity can only be improved by increasing the bulk voltage and/or decreasing the γ value. This is why most of the PFRs [9], [10]→[12] adopt high supply voltages. Since V_C is a function of the p-channel process parameters and V_T is a function of the n-channel process parameters, the resistance is therefore sensitive to both sets of process parameters.

2.2. Series-Pair Resistors with Unscaled-Gate Compensation

When the gates of a pair of series-connected MOSFETs are driven by one or more unscaled terminal voltages offset by a dc control gate bias, an unscaled-gate compensation series resistor is formed. Since the bulk terminals of the series transistor pair are connected to the bulk supply, the terminal coupling function

combined with gate bias can be easily achieved via simple source followers as described earlier in section 2.2.

There are two possible arrangements of TCR-I and TCR-II in series form; SPR-I and SPR-II as shown in Fig. 2.4(a) and (b), respectively. However, the SPR-II can be reduced to the single buffer structure, SPR-III, as shown in Fig. 2.4(c). This structure is similar to that already reported [16],[17] which also included a circuit technique aimed at cancelling the bulk effect. The reduction of the SPR-II to the SPR-III form does not, of course, maintain the modularity of the TCR-I or TCR-II. However, the SPR-III structure clearly offers a reduced silicon area and component count.

Using Eqns (2.1) and (2.4), it can be shown that the current expression for the SPR-I is

$$I_{s1} = K_s[(V_C - V_T)v_{ds} - \frac{(1+\delta)}{8(V_C - V_T)}v_{ds}^3 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \tag{2.9}$$

where $\delta = \gamma/2\sqrt{\phi_B - V_B}$. Note that K_s is used to identify the transconductance parameter for the MOSFET in series form. When Eqn (2.9) is compared with either (2.6) or (2.7), it can be seen that the dominant quadratic term in (2.6) is replaced by a bias-dependent cubic term. It can be appreciated that this linearisation process suppresses the bias-independent quadratic component without relying on a balanced or parallel-form structure. The bulk-dependent quadratic term illustrates that the bulk effect remains a dominant factor affecting the overall distortion performance of the resistor. The (identical) current expressions for the SPR-II and SPR-III can be written as

$$I_{s2} = I_{s3} = K_s[(V_C - V_T)v_{ds} - \frac{(1-\delta)}{8(V_C - V_T)}v_{ds}^3 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \tag{2.10}$$

Since $\delta << 1$, the three series resistors exhibit virtually identical terminal char-

acteristics. Their mid-point voltages which are obtained as

$$v_{m1} = \frac{v_d + v_s}{2} + \frac{(1-\delta)}{8(V_C - V_T)} v_{ds}^2 \tag{2.11}$$

$$v_{m2} = v_{m3} = \frac{v_d + v_s}{2} - \frac{(1+\delta)}{8(V_C - V_T)} v_{ds}^2 \tag{2.12}$$

are also similar, being composed of a linear common-mode term plus a quadratic term. It can be seen that the quadratic components are dependent on the biases, process parameters and signal levels.

With reference to Eqns (2.9) and (2.10), the nonlinearity can be reduced by increasing the gate-overdrive bias ($V_C - V_T$), bulk voltage (V_B) and using processes with the lowest possible bulk modulation parameter. It may be noted that for the same resistor value (identical channel width W and the channel lengths for the PFR and SPR in a ratio of 1:4), the bulk quadratic terms in PFR and SPRs would be the same. Thus the SPR would suffer higher distortion than the PFR if the gate-overdrive bias is low. This argument is based on the observation that in practice, the bulk quadratic term is usually greater than the bias-dependent distortion term. Since shorter channel lengths are required in the SPRs, the relative silicon area is smaller than PFR. In certain series architectures, such as SPR-III, a smaller component count results. These claim a potential advantage in that series-pair resistors can replace the parallel-form resistor whenever the silicon requirement is the important design factor. In practice, the limit of the channel length depends upon the technology supported. The longer the channel length, the smaller the channel-length modulation. There is, however, a trade-off between the silicon area and distortion for small channel-length design.

2.2.3 Series-Parallel Quad Resistor with Unscaled-Gate Compensation

The cubic distortion generated in the series-form resistors can be eliminated by adopting a series-parallel structure. This is achieved by disconnecting the buffer input at the centre of the SPR-III and applying the signal from the mid-point of the SPR-I. Such a modification produces a new series-parallel quad resistor, which is denoted as (SPQR-I), in Fig. 2.5(a). The upper branch current in the SPQR-I is

$$I_1 = K_{sp}[(V_C - V_T)v_{ds} - \frac{(1-\delta)}{8(V_C - V_T)}v_{ds}^3 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \qquad (2.13)$$

and the lower branch current is

$$I_2 = K_{sp}[(V_C - V_T)v_{ds} + \frac{(1-\delta)}{8(V_C - V_T)}v_{ds}^3 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \qquad (2.14)$$

where K_{sp} is the transconductance parameter for the MOSFET in series-parallel configuration. The cubic distortion terms in both Eqns (2.13) and (2.14) have opposite-phases. Consequently, the sum of these branch currents is

$$I_{sp} = 2K_{sp}[(V_C - V_T)v_{ds} - \frac{\gamma}{4\sqrt{\phi_B - V_B}}(v_d^2 - v_s^2)] \qquad (2.15)$$

The remaining distortion is that due to bulk modulation effect.

It is notable that the drain-to-source voltage for each transistor in the SPR is reduced to approximately half of that in the PFR. The reduction in v_{ds} lowers the nonlinearity and improves the operating range [4]. The improvement occurs because of the increase in drain-to-source signal swing before the MOSFET is driven into saturation. This advantage can be applied to the PFR equally well by splitting the individual TCR-I and TCR-II into identical structures. The resulting structure is a series-parallel type which is named as SPQR-II in Fig. 2.5(b).

Under ideal conditions, the signals generated at the mid-points of SPQR-II

are

$$v_x = v_y = \frac{v_d + v_s}{2} \tag{2.16}$$

This is a purely common-mode signal because two identical nonlinear TCR-I's and TCR-II's function as potential dividers. This is in contrast to the SPR structures where the mid-point voltage is the common-mode signal plus a nonlinearity. Analysis shows that the SPQR-II has the same current expression as the SPQR-I. The SPQR-II structure can be further simplified to the SPQR-III (Fig. 2.5(c)) which only uses 3 buffers, thus saving hardware, power consumption and silicon area. Although the SPQR-II requires more elements, it does however maintain a modular structure.

Using the former criteria for the resistance comparison, the channel length for PFR, SPR and SPQR are in a ratio of 4:1:2. Under this condition, the bulk quadratic distortion in SPQR is the same as that for the PFR and SPR. Assuming that the three resistor structures adopt the same dimension buffer, the area of the transistor pairs for the PFR, SPR and SPQR are in a ratio of 4:1:4. Even though the SPQR requires the channel length to be a factor of two lower than that in the PFR, since there are four transistors, the silicon area for the SPQR and PFR are the same.

2.3 MOS Resistors with Dual Gate-Bulk Compensation

The preceding section has demonstrated the influence of the bulk modulation effect in the unscaled-gate compensation resistors. This section describes dual gate-bulk compensation techniques that can significantly improve the linearity.

Prior to discussion of the linearisation techniques, modified arrangements of the TCR-I and TCR-II together with their CMOS implementation approaches are described.

The dual gate-bulk compensation schemes attempt to eliminate bulk or body effect by simultaneously modulating the gate and bulk terminal of a MOSFET. This can be achieved by converting the gate-compensated TCR-I and TCR-II into their gate-bulk-compensated counterparts (Fig. 2.6) accordingly. Consider the simplified Level-2 non-saturation drain-current expression of (2.1) with the assumption that carrier mobility is constant. The currents in the gate-bulk-compensated TCR-I and TCR-II become

$$I_1 = 2K[(V_C - V_T)v_{ds} + \frac{1}{2}v_{ds}^2 + \frac{\gamma}{4\sqrt{\phi_B - V_B}}v_{ds}^2] \tag{2.17}$$

and

$$I_2 = 2K[(V_C - V_T)v_{ds} - \frac{1}{2}v_{ds}^2 - \frac{\gamma}{4\sqrt{\phi_B - V_B}}v_{ds}^2] \tag{2.18}$$

where

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V_B} \tag{2.19}$$

Contrast Eqns (2.17) and (2.18) with Eqns (2.2) and (2.3). It can be seen that the independent quadratic terms are the same but the bulk-dependent quadratic terms exhibit opposite signs. Furthermore, these bulk-dependent quadratic terms are a function of the difference potential v_{ds}. Although these modified TCR-I and TCR-II circuits produce distortion levels comparable with the gate-compensated TCR structures, the oppositely signed quadratic terms can be suppressed when the blocks are used as in the previous linearisation schemes.

There are two approaches to implementing a CMOS buffer for this dual gate-bulk compensation technique. The first is to use a simple source follower [9] as discussed in section 2.1. Generation of V_C in Eqns (2.17) and (2.18) relies on

the p-channel source follower of Fig. 2.2. The relationship is described by Eqn (2.5). Since the n-channel gate-coupled transistor pair is no longer connected to a negative bulk supply, n-channel source followers must be used to provide the negative bias as well as coupling the terminal voltage to the bulk terminals. Fig. 2.7 shows the circuit diagram of an n-channel source follower. The dc bulk voltage can be obtained as

$$V_B = -(V_{BIAS} - V_{SS}) = -\sqrt{\frac{I_B}{K_B}} - V_{TO} \tag{2.20}$$

where I_B is the dc bias current for the n-channel source follower, K_B is the transconductance parameter of the transistors M1 and M2 in the source follower and V_{TO} is the threshold voltage for an n-channel transistor at zero bulk voltage. Substituting Eqns (2.5), (2.20) into (2.17) and (2.18), the current expressions for source-follower-based TCR-I and TCR-II are

$$I_1 = 2K[(\sqrt{\frac{I'_B}{K'_B}} + V_{TOp} - V_T)v_{ds} + \frac{1}{2}v_{ds}^2 + \frac{\gamma}{4\sqrt{\phi_B + \sqrt{\frac{I_B}{K_B}} + V_{TO}}}v_{ds}^2] \tag{2.21}$$

and

$$I_2 = 2K[(\sqrt{\frac{I'_B}{K'_B}} + V_{TOp} - V_T)v_{ds} - \frac{1}{2}v_{ds}^2 - \frac{\gamma}{4\sqrt{\phi_B + \sqrt{\frac{I_B}{K_B}} + V_{TO}}}v_{ds}^2] \tag{2.22}$$

Therefore, the resistance is dependent on the p-channel and n-channel process parameters, as discussed previously.

The second approach is the differential-pair-based level-shifting buffer (LSB) [16],[17]. Fig. 2.8 illustrates the schematic diagram of the n-channel LSB. The saturation-mode NMOS buffers produce level shifted outputs

$$v_g = v_x + V'_C \tag{2.23}$$

and

$$v_b = v_x + V'_B \tag{2.24}$$

where

$$V'_C = \sqrt{\frac{I_B}{K_B}} + V_T \tag{2.25}$$

$$V'_B = -\sqrt{\frac{I_B}{K_B}} - V_{TO} \tag{2.26}$$

The LSB performs dual buffer and gate-bulk bias function. It can be noticed that both V'_C (Eqn (2.25)) and V'_B (Eqn (2.26)) are defined by a set of n-channel process parameters. This is in contrast to the simple source-follower approach described previously, where the term V_C (Eqn (2.5)) is quantified by the p-channel process parameters. Replacing V_C and V_B by V'_C and V'_B, respectively, in the Eqns (2.17) and (2.18), the resulting current expressions for the TCR-I and TCR-II are

$$I_1 = 2K[\sqrt{\frac{I_B}{K_B}}v_{ds} + \frac{1}{2}v_{ds}^2 + \frac{\gamma}{4\sqrt{\phi_B + \sqrt{\frac{I_B}{K_B}} + V_{TO}}}v_{ds}^2] \tag{2.27}$$

and

$$I_2 = 2K[\sqrt{\frac{I_B}{K_B}}v_{ds} - \frac{1}{2}v_{ds}^2 - \frac{\gamma}{4\sqrt{\phi_B + \sqrt{\frac{I_B}{K_B}} + V_{TO}}}v_{ds}^2] \tag{2.28}$$

Any variance in the bias-transistor process parameters in the external network (not shown in Fig. 2.8) may cause the shift of threshold voltage, and thus a change in the bias current and the resistor value. It is also the same situation for I'_B in the equations (2.21) and (2.22). Unlike the earlier-mentioned source follower, the transistor-type of the LSB is identical to the gate-bulk-coupled MOSFETs. This scheme avoids the problem of matching the p-channel and n-channel devices. The resistor reduces the parameter dependent terms when compared with the source-follower-based TCR-I or TCR-II where the resistance depends on V_{TO_p} and V_T terms (equations 2.21 and 2.22). The only disadvantage is that the gate-bulk-compensated TCR-I or TCR-II requires two extra transistors when compared with the gate-compensated TCR-I or TCR-II, but in a VLSI context this would not be a significant issue.

2.3.1 Parallel-Form Resistor with Dual Gate-Bulk Compensation

Replacing the gate-compensated TCR-I and TCR-II by gate-bulk compensated TCR-I and TCR-II circuits, respectively, a dual gate-bulk compensated PFR is formed. In contrast with the earlier floating resistor [8],[9] in which p-channel controlled devices are biased via n-channel buffers, the LSB can be directly utilised in implementing the general parallel-form resistor as shown in Fig. 2.9. Assuming the transistors in the buffer are identical to the controlled devices M1 and M2, an analysis (using Eqns (2.1) and (2.23) to (2.26)) has shown that

$$I_1 = 2K_p[\sqrt{\frac{I_{Bp}}{K_p}}v_{ds} + \frac{1}{2}(1+\delta_{Bp})v_{ds}^2] \tag{2.29}$$

and

$$I_2 = 2K_p[\sqrt{\frac{I_{Bp}}{K_p}}v_{ds} - \frac{1}{2}(1+\delta_{Bp})v_{ds}^2] \tag{2.30}$$

with

$$\delta_{Bp} = \frac{\gamma}{2\sqrt{\phi_B + \sqrt{\frac{I_{Bp}}{K_p}} + V_{TO}}} \tag{2.31}$$

where I_{Bp} is the bias current for the parallel form resistor and K_p is the transconductance parameter for the matched set of transistors. The addition of these two currents yields

$$I_p = 4K_p\sqrt{\frac{I_{Bp}}{K_p}}v_{ds} \tag{2.32}$$

Although the resistance dependence on threshold voltage is not completely eliminated (since the bias current I_B will be sensitive to threshold parameter variations), the resistance of this modified PFR can exhibit a smaller dependence on process parameters when compared with source-follower-based structures [8],[9]. The remaining distortion is principally due to the small cubic term and other second-order factors such as mobility degradation and geometrical mismatches which are ignored in the approximate analysis.

2.3.2 Series-Pair Resistors with Dual Gate-bulk Compensation

The principal merit that series-pair structures offer, i.e. lower silicon area as discussed in Section 2.2, is offset by the large quadratic bulk distortion component. As a result, this usually requires that they operate in high-supply-voltage applications so as to improve the nonlinearity. This restriction can be relaxed by applying the gate-bulk compensation technique [16],[17]. Following the gate-compensated series resistor schemes of Fig. 2.4, a group of gate-bulk-compensated SPR can be formed as shown in Fig. 2.10. Given the constant mobility assumption in Section 2.1, the currents I_{s1} and I'_{s1} flowing via SPR-I are obtained by solving the mid-point voltage based on Eqn (2.1) and substituting back the obtained value into the branch currents. Since the branch currents are identical, only one branch current is sufficient to define the transfer function. It is given by

$$I_{s1} = K_s[\sqrt{\frac{I_{Bs}}{K_s}}v_{ds} - \frac{(1+\delta_{Bs})^2}{8\sqrt{\frac{I_{Bs}}{K_s}}}v_{ds}^3] \tag{2.33}$$

where

$$\delta_{Bs} = \frac{\gamma}{2\sqrt{\phi_B + \sqrt{\frac{I_{Bs}}{K_s}} + V_{TO}}} \tag{2.34}$$

The distortion is the bias-dependent cubic term. As expected, however, the two currents for the SPR-II and SPR-III as shown in Figs 2.10(b) and (c) would be equal: $I_{s2} = I_{s3} = I_{s1}$. The linearisation process can be appreciated by noting that SPR-I is a transformation of SPR-III [16]-[17] and as such, has similar terminal characteristics. Analysis shows that the mid-point voltage for the SPR-I is

$$v_m = \frac{v_d + v_s}{2} + \frac{(1+\delta_{Bs})}{8\sqrt{\frac{I_{Bs}}{K_s}}}v_{ds}^2 \tag{2.35}$$

and for the SPR-II and SPR-III is

$$v_n = \frac{v_d + v_s}{2} - \frac{(1+\delta_{Bs})}{8\sqrt{\frac{I_{Bs}}{K_s}}}v_{ds}^2 \tag{2.36}$$

These two expressions are very similar to those described previously in Eqns (2.11) and (2.12).

2.3.3 Series-Parallel Quad Resistors with Dual Gate-bulk Compensation

Although the dominant quadratic distortion terms are absent in SPR-I and SPR-III structures, the cubic nonlinearity generated can significantly degrade the THD performance. Fig. 2.11(a) illustrates a gate-bulk compensation series-parallel quad resistor (SPQR-I) [19] which cancels both the cubic nonlinearity and the bulk-dependent quadratic term. It is easily seen that the upper branch consisting of M1 and M2 together with the arrangement of the LSBs is the SPR-I. With the mid-point potential buffered to the "commoned" gates and bulk terminals of M3 and M4, the dominant quadratic nonlinearity in the lower branch current is also suppressed but in this case, the concomitant cubic distortion component appears with reversed sign.

Linearisation in this series/parallel quad resistor (SPQR-I) configuration is therefore enhanced in relation to that of SPR structures by distributing the signal across pairs of devices without having the associated cubic non-linearity appearing in the net terminal current. Since the signal potential is distributed almost equally across the devices, the residual distortion (due to mobility degradation) would be expected to be lower than that in parallel schemes where individual devices support the full signal potential. This strategy can be applied for the PFR to generate the gate-bulk- compensated SPQR-II and SPQR-III as shown in Fig. 2.11.

Noting that the upper portion of the SPQR-I is an SPR-I, the upper branch

current of Eqn (2.33) is the same. Thus,

$$I_1 = K_{sp}[\sqrt{\frac{I_{Bsp}}{K_{sp}}}v_{ds} - \frac{(1+\delta_{Bsp})^2}{8\sqrt{\frac{I_{Bsp}}{K_{sp}}}}v_{ds}^3] \tag{2.37}$$

with

$$\delta_{Bsp} = \frac{\gamma}{2\sqrt{\phi_B + \sqrt{\frac{I_{Bsp}}{K_{sp}}} + V_{TO}}} \tag{2.38}$$

where K_{sp} is the transconductance parameters for the controlled series-parallel devices and the matched set of transistors in the LSB. The lower branch current is

$$I_2 = K_{sp}[\sqrt{\frac{I_{Bsp}}{K_{sp}}}v_{ds} + \frac{(1+\delta_{Bsp})^2}{8\sqrt{\frac{I_{Bsp}}{K_{sp}}}}v_{ds}^3] \tag{2.39}$$

Since the first cubic terms in these branch currents are oppositely signed, then adding the two branch currents gives

$$I_{sp1} = 2K_{sp}\sqrt{\frac{I_{Bsp}}{K_{sp}}}v_{ds} \tag{2.40}$$

As shown earlier, the dominant cubic distortion terms and bulk quadratic terms are cancelled. The remaining distortion is principally influenced by the mobility degradation effect. A comparison of this effect with other group of resistors is carried out in a later section.

In the case of the SPQR-II and SPQR III, the mid-point voltages are purely common-mode. Their current expressions, under the constant mobility assumption, are equal to the SPQR-I; $I_{sp2} = I_{sp3} = I_{sp1}$.

2.4 MOS Resistors with Scaled-Gate Compensation

The objective of this section is to introduce an alternative technique which can suppress the major quadratic components in the signal current of a MOSFET.

First, the circuit elements required by this technique are described and then the linearisation of a grounded and floating MOSFET.

The scaled-gate compensation scheme [5] scales the terminal signal used to linearise MOS transistors. The magnitude of the scaled signal is chosen to correlate with the process parameters such that application to the gate only, completely suppresses the quadratic terms. Although passive resistors and operational amplifiers are available for scaled signal generation, this method is not suitable for integrated circuits. A new CMOS compatible network is proposed [7] which solves this problem. Fig. 2.12 shows the circuit diagram of the scaled signal generator based on the 'inverse function approach' [47].

The circuit essentially consists of two sections: 'drive' and 'copy'. The drive section is formed by transistors M1,M2, M5 and M7 whereas the copy section is formed by transistors M3,M4, M6 and M8. Transistors M1-M4 constitute two differential pairs with tail currents equal to $2I$. By means of the p-channel current mirror M7-M8, the voltage V_{in} is copied to the scaled differential pair M3-M4, yielding the required weighted voltage.

Let the transconductance parameters for M1/M2 and M3/M4 to be K_1 and K_2, respectively. Using the saturation drain current given by Eqn (E.18) and assuming constant mobility:

$$v_{gs1} = \sqrt{\frac{I_1}{K_1}} + V_{TO} \tag{2.41}$$

$$v_{gs2} = \sqrt{\frac{I_2}{K_1}} + V_{TO} \tag{2.42}$$

$$v_{gs3} = \sqrt{\frac{I_1}{K_2}} + V_{TO} \tag{2.43}$$

$$v_{gs4} = \sqrt{\frac{I_2}{K_2}} + V_{TO} \tag{2.44}$$

Given that

$$V_{in} = v_{gs1} - v_{gs2} = \sqrt{\frac{I_1}{K_1}} - \sqrt{\frac{I_2}{K_1}} \tag{2.45}$$

the generated scaled voltage is thus obtained as

$$v_g = V_C + v_{gs3} - v_{gs4} = V_C + \sqrt{\frac{K_1}{K_2}} V_{in} \tag{2.46}$$

It will be appreciated that the gate drive is tunable via the control voltage V_C and the ac signal magnitude is governed by the ratio of the aspect ratios of the differential transistor pairs. This tuning scheme differs from FPR, SPR and SPQR in that tuning does not change the bias current nor, as result, the power consumption.

2.4.1 Scaled-Gate Compensation: Grounded Resistor

The most straightforward implementation is to linearise a grounded resistor as shown in Fig. 2.13 using the scaled generator of Fig. 2.12. Assuming constant mobility and zero cubic terms, the non-saturation drain current of Eqn (1.11) flowing into the grounded transistor is

$$I_d \;=\; 2K[(V_C + \sqrt{\frac{K_1}{K_2}} V_{in} - V_T)V_{in} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})V_{in}^2] \tag{2.47}$$

where V_T is defined in Eqn (1.14). If it were possible to set the aspect ratio of the differential transistor pair in the generator such that

$$\sqrt{\frac{K_1}{K_2}} = \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}}) \tag{2.48}$$

then Eqn (2.47) reduces to

$$I_d = 2K(V_C - V_T)V_{in} \tag{2.49}$$

The quadratic term would be eliminated with the remaining odd nonlinearity (which is ignored in the analysis) being relatively small. It may be noted that the

resistance is tuned via the control voltage V_C but is dependent on the threshold voltage parameters. Since the differential-pair structure of the scaled generator offers an extremely high input impedance, the loading effect is much reduced, and resistance values in the $M\Omega$ range are readily available. This is in sharp contrast with the Bilotti grounded resistor [3] for which the dc bias network must offer a very high resistance in order not to disturb the controlled MOSFET resistance. In practice, it may not be possible to achieve the necessary precision in setting K_1 and K_2 to satisfy Eqn (2.48) and some even-order distortion will remain.

2.4.2 Scaled-Gate Compensation: Floating Resistors

Scaling the gate drive as in the grounded-resistor scheme can be applied equally to the synthesis of new floating resistors by employing identical parallel structures as shown in Fig. 2.14. This symmetrical arrangement essentially drives the gates with scaled version of v_d and v_s. Using the usual assumptions as above, the upper branch current of Eqn (1.11) is

$$I_1 = 2K[(V_C + \sqrt{\frac{K_1}{K_2}}v_d - V_T)(v_d - v_s) - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(v_d^2 - v_s^2)] \quad (2.50)$$

and the lower branch current is

$$I_2 = 2K[(V_C + \sqrt{\frac{K_1}{K_2}}v_s - V_T)(v_d - v_s) - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(v_d^2 - v_s^2)] \quad (2.51)$$

In this case, choosing the aspect-ratio relationship as

$$\sqrt{\frac{K_1}{K_2}} = 1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}} \quad (2.52)$$

produces a sum current

$$I_1 + I_2 = I_p = 4K(V_C - V_T)v_{ds} \quad (2.53)$$

It should be noted that by comparison with the grounded resistor case where $\sqrt{\frac{K_1}{K_2}} \approx \frac{1}{2}$, the ratio of the aspect ratio is close to 1. The structure is an alternative

implementation of the PFR with the difference that the gate-compensated signal is scaled according to the process parameters. Setting $\sqrt{\frac{K_1}{K_2}} = 1$, the scaled generator performs as an unscaled buffer and can be applied as previously described, taking advantage of the fact that tuning of the control voltage V_C does not alter the power consumption.

2.5 Second-Order Effects

That bulk effect is the dominant factor affecting distortion has been established both by simulation and by experiment. However, with the bulk effect adequately suppressed, mobility degradation, geometrical mismatches and channel-length modulation must be considered as factors affecting the linearity of MOS resistors. Practical designs normally employ long channel transistors in order to minimise the channel-length modulation. Geometrical mismatches depend both on the size of the transistors and their layout but can be reduced to low levels. Mobility degradation effects on the other hand constitute a particularly important secondary source of distortion. Emphasis in this section is placed on analysis of the mobility effect in gate-bulk-compensated MOS resistors.

With reference to the proof in Appendix G-I, the current expression of Eqn (G.19) for the PFR with mobility degradation effect is approximated as

$$\begin{aligned} I_p \approx\ & 4K'_p[\sqrt{\frac{I_{Bp}}{K'_p}}v_{ds} - \frac{1}{2}\theta_p(1+\delta_{Bp})\sqrt{\frac{I_{Bp}}{K'_p}}v_{ds}^2 \\ & - \frac{1}{4}\theta_p(1+\delta_{Bp})^2 v_{ds}^3] \end{aligned} \quad (2.54)$$

where K'_p and θ_p are defined in Eqns (G.7) and (G.11), respectively. It should be noted that this approximation assumes the mobility-related cubic term is significantly larger than the gamma-related cubic term as is the case for the process

parameters given in the Appendix B. The remaining symbols have been described in the above sections. Similarily, the approximate Eqn (H.18) for the SPR structures is

$$I_{s1} = I_{s2} = I_{s3} \approx K'_s[\sqrt{\frac{I_{Bs}}{K'_s}}v_{ds} - \frac{1}{4}\theta_s(1+\delta_{Bs})\sqrt{\frac{I_{Bs}}{K'_s}}v_{ds}^2 + \frac{1}{8}\theta_s(1+\delta_{Bs})^2 v_{ds}^3 - \frac{(1+\delta_{Bs})^2 v_{ds}^3}{8\sqrt{\frac{I_{Bs}}{K'_s}}}] \tag{2.55}$$

where K'_s and θ_s are defined in Eqns (H.11) and (H.16), respectively. Then, the equation for the SPQR structures can be approximated as

$$I_{sp1} = I_{sp2} = I_{sp3} \approx 2K'_{sp}[\sqrt{\frac{I_{Bs}}{K'_{sp}}}v_{ds} - \frac{1}{4}\theta_{sp}(1+\delta_{Bsp})\sqrt{\frac{I_{Bsp}}{K'_{sp}}}v_{ds}^2 - \frac{1}{16}\theta_{sp}(1+\delta_{Bsp})^2 v_{ds}^3] \tag{2.56}$$

where K'_{sp} and θ_{sp} are described in Eqns (I.3) and (I.4), respectively.

To achieve identical resistance value, the channel lengths and bias currents are chosen so as to equalise the nominal resistance values and quiescent buffer voltage levels. For a given channel width W, the channel lengths L_p, L_s and L_{sp} are required in the ratio 4:1:2 when I_{Bp}, I_{Bs} and I_{Bsp} are in a 1:4:2. For $K_s = K'$ and $I = I_{Bs}$, the relationship is

$$\sqrt{\frac{I}{K'}} = \sqrt{\frac{I_{Bp}}{K'_p}} = \sqrt{\frac{I_{Bs}}{K'_s}} = \sqrt{\frac{I_{Bsp}}{K'_{sp}}} \tag{2.57}$$

Substituting Eqn (2.57) into (G.11), (G.12), (H.16), (H.17), (I.4), and (I.5) accordingly, gives we have

$$\delta'_B = \delta_{Bp} = \delta_{Bs} = \delta_{Bsp} = \frac{\gamma}{2\sqrt{\phi_B + \sqrt{\frac{I}{K'}} + V_{TO}}} \tag{2.58}$$

and

$$\theta' = \frac{\theta}{(1+\theta\sqrt{\frac{I}{K'}})} \tag{2.59}$$

Consequently, Eqn (2.54) for the PFR (2.54) can be re-written as

$$I_p \approx K'[\sqrt{\frac{I}{K'}}v_{ds} - \frac{1}{2}\theta'(1+\delta'_B)\sqrt{\frac{I}{K'}}v_{ds}^2 - \frac{1}{4}\theta'(1+\delta'_B)^2 v_{ds}^3] \tag{2.60}$$

and that for the SPR in Eqn (2.55) becomes

$$\begin{aligned} I_{s1} = I_{s2} = I_{s3} \approx\ & K'[\sqrt{\frac{I}{K'}}v_{ds} - \frac{1}{4}\theta'(1+\delta'_B)\sqrt{\frac{I}{K'}}v_{ds}^2 \\ & + \frac{1}{8}(1+\delta'_B)^2\theta' v_{ds}^3 - \frac{(1+\delta'_B)^2 v_{ds}^3}{8\sqrt{\frac{I}{K'}}}] \end{aligned} \tag{2.61}$$

The final expression for the SPQR in Eqn (2.56) is

$$\begin{aligned} I_{sp1} = I_{sp2} = I_{sp3} \approx\ & K'[\sqrt{\frac{I}{K'}}v_{ds} - \frac{1}{4}\theta'(1+\delta'_B)\sqrt{\frac{I}{K'}}v_{ds}^2 \\ & - \frac{1}{16}\theta'(1+\delta'_B)^2 v_{ds}^3] \end{aligned} \tag{2.62}$$

The mobility-degradation effect generates quadratic and cubic nonlinear products. The coefficents of the quadratic and cubic mobility-related term in the PFR is related to the SPR in a ratio of 2:1, 2:1 and to the SPQR in a ratio of 2:1, 4:1, respectively. Apart from the sign of the cubic mobility term, the SPR has approximately the same mobility-degradation product terms as the SPQR. However, the large bias-dependent cubic term in the SPR still dominates the overall distortion performance despite the presence of this non-ideal effect. In this respect, the SPQR circuit offers a better distortion performance than the PFR and SPR circuits.

2.6 Applications of MOS Resistors

In this section, illustrative examples of the application of MOS resistors to fully integrated continuous-time filters are discussed. First the conversion of the classical Tow-Thomas biquadratic filter [88],[89] into the GVCR-based MOSFET-C

filter is discussed. This is followed by a description of simple Sallen-Key filters [90] and how such filter modules can be built using MOS buffers, buffer-based MOS resistors and capacitors. A fourth-order SPQR-based Sallen-Key lowpass filter example is given.

The starting point in GVCR MOSFET-C filter design is an active RC prototype network in which the resistors can be replaced by linearised grounded or virtually grounded MOS transistor networks. These operate in triode region such that the input-output operation of the resulting MOS filter is linear over an extended voltage range. The conversion of active-RC networks to GVCR MOSFET-C implementation is therefore restricted to filter circuit topologies based on virtually grounded resistors. Similar approaches are applied for the buffer-based MOS filter but the essential resistive elements must be of the floating form.

2.6.1 A Tow-Thomas Second-Order Lowpass Filter

The second-order section is perhaps the most important practical building block in the design of active filter. The Tow-Thomas section [88,[89] offers simultaneous second-order lowpass, and bandpass filtering of the input signal. With minor changes or additions, virtually any other second-order function (such as bandstop, allpass and highpass) can be realized.

With reference to the circuit diagram of Fig. 2.15, it can be seen to consist of two integrators (one of which is the summing lossy integrator) and one inverter. Routine analysis shows that the transfer functions at different tapping points are

$$\frac{V_4}{V_1}(s) = \frac{\frac{-1}{C_1R_3}s}{s^2 + \frac{1}{C_1R_1}s + \frac{1}{C_1C_2R_2R_4}} \tag{2.63}$$

$$\frac{V_3}{V_4}(s) = \frac{-1}{sC_2R_4} \tag{2.64}$$

$$\frac{V_2}{V_3}(s) = -1 \tag{2.65}$$

As a result,

$$\frac{V_2}{V_1}(s) = \frac{V_4}{V_1} \times \frac{V_3}{V_4} \times \frac{V_2}{V_3} \tag{2.66}$$

$$= \frac{\frac{-1}{C_1C_2R_3R_4}}{s^2 + \frac{1}{C_1R_1}s + \frac{1}{C_1C_2R_2R_4}} \tag{2.67}$$

Such a transfer function is equivalent to the lowpass standard form [43]:

$$\frac{V_2}{V_1}(s) = \frac{Hw_o^2}{s^2 + \frac{w_o}{Q}s + w_o^2} \tag{2.68}$$

where H is the passband gain, w_o is the natural radian cutoff frequency and Q is the quality factor. By comparing the coefficients of Eqns (2.68) and (2.69), the following relationships are obtained

$$w_o = \frac{1}{\sqrt{C_1C_2R_2R_4}} \tag{2.69}$$

$$Q = \sqrt{\frac{R_1^2C_1}{R_2R_4C_2}} \tag{2.70}$$

$$H = \frac{R_2}{R_3} \tag{2.71}$$

Since it is usual to use both the frequency and magnitude scaling, the following choices are made

$$C_1 = C_2 = 1F \tag{2.72}$$

$$R_2 = R_4 = 1\Omega \tag{2.73}$$

These choices set the parameters as

$$w_o = 1rad/s \tag{2.74}$$

$$R_1 = Q \tag{2.75}$$

$$R_3 = \frac{1}{H} \tag{2.76}$$

and giving the normalised form shown in Fig. 2.16. This circuit [7] form the basis for the design of a MOSFET-C second-order section.

Fig. 2.17 shows the circuit diagram for the classical RC active filter implementing a second-order Chebyshev lowpass function with 0.5 dB passband ripple. The low-frequency gain (H) of the filter is taken to be unity. For the Chebyshev response, Q is chosen to be 0.86 which sets the ratio of R_1 with respect to 1Ω. The conversion to its equivalent GVCR-based filter structure is demonstrated in Fig. 2.18. The 3 dB cut-off frequency is scaled at 4.7 KHz (The simulation of this filter will be described in chapter 3). It may be noted that the presence of common inputs could reduce the number of (identical) control circuits required (as embodied in Fig. 2.12) to only four, thus leading to the simplified structure shown in Fig. 2.19.

It is of particular interest to note that grounded GVCRs and MOS operational amplifiers can be pre-designed and stored as standard cells in a computer library and would therefore make effective use of available VLSI CAD tools.

2.6.2 Fourth-Order Sallen-Key Lowpass Filter

The circuit given in Fig. 2.20 was originally described by Sallen and Key [90] and is a second-order lowpass filter utilizing single feedback. In this circuit, the non-inverting amplifier provides a relationship between V_2 and V_a, which is

$$\frac{V_2}{V_a}(s) = K \tag{2.77}$$

and the transfer function becomes:

$$\frac{V_2}{V_1}(s) = \frac{K\frac{1}{R_1R_2C_1C_2}}{s^2 + (\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1}{R_2C_2} - \frac{K}{R_2C_2})s + \frac{1}{R_1R_2C_1C_2}} \tag{2.78}$$

This transfer function has the general form

$$\frac{V_2}{V_1}(s) = \frac{Kw_o^2}{s^2 + (\frac{w_o}{Q})s + w_o^2} \tag{2.79}$$

Setting $K = 1$, the non-inverting amplifier reduces to a voltage follower which can easily be implemented in CMOS form. Choosing $R_1 = R_2 = 1\Omega$ and also $w_o = 1rad/s$ gives two important design equations

$$C_1 = 2Q \tag{2.80}$$

and

$$C_2 = \frac{1}{2Q} \tag{2.81}$$

In principle, several sections can be cascaded to achieve high-order filtering. The nature of the filter response (Butterworth, Chebyshev etc.) can be selected by choosing the appropriate values for the Q factors and natural frequencies. Similarly, if the Sallen-Key filter is cascaded with a first-order lowpass stage, odd-order filters are formed.

An example of the 4th-order normalised Butterworth lowpass filter is shown in Fig. 2.21. For a Butterworth response, the quality factors Q_1 and Q_2 for the first and second section are required to be 0.54 and 1.31, respectively. This sets the capacitor values according to the Eqns (2.81) and (2.82). The first step for a fully integrated filter implementation is to choose appropriate circuit elements. Since the circuit topology requires floating resistors, MOS types such as PFR, SPR and SPQR can be employed in this filter. The buffer can take any form, for example; MOS operational amplifier, MOS source follower etc. . Fig. 2.22 shows an equivalent SPQR-based Sallen-Key lowpass filter having a 37 KHz 3 dB cut-off frequency. The SPQR-I [19] and unity-gain buffer [91] are used for the filter synthesis. Fig. 2.23 shows the schematic diagram of the buffer (a VanPeteghem-Rice LSB [16],[17] plus a source-follower stage). It is notable that this filter does not require operational amplifiers. This not only reduces the silicon area, but can also extend the filter response to higher-frequency operation because of the

wideband capability of the buffer.

With reference to the indicated dotted outline in Fig. 2.22, the filter can be further reduced to the simplified form (Fig. 2.24) based on the equivalence of the structure of SPR-II and SPR-III as described previously in Chapter 2. The synthesis method is advantangeous especially in the realization of higher-order filters owing to the employment of a common buffer structure and possible reduction in buffer numbers. Furthermore, the buffer design is straightforward, and avoids complicated transistor-level design. As for GVCR-based filters, the filter together with the synthesis technique is also suitable for pre-defined library cells and CAD design automation. Finally, this network avoids the cost of balanced structures and achieves a high degree of linearity by individually linearizing each resistor. The simulation of this filter is also discussed further in Chapter 3.

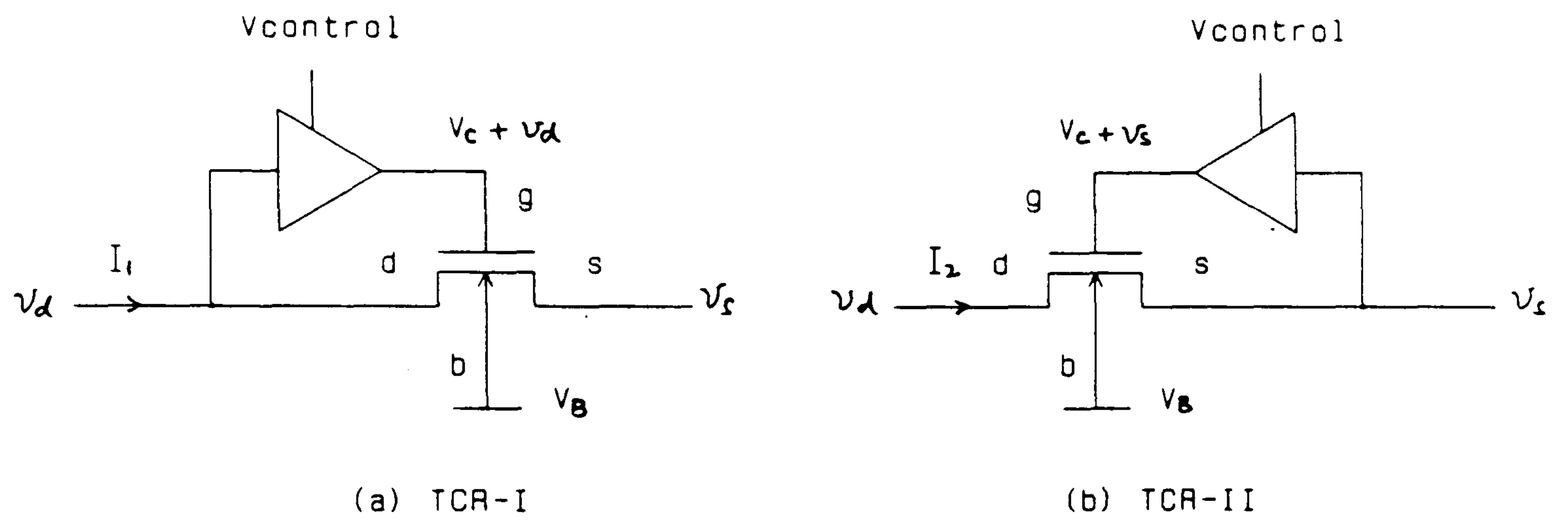


Figure 2.1: Fundamental CMOS resistor building blocks

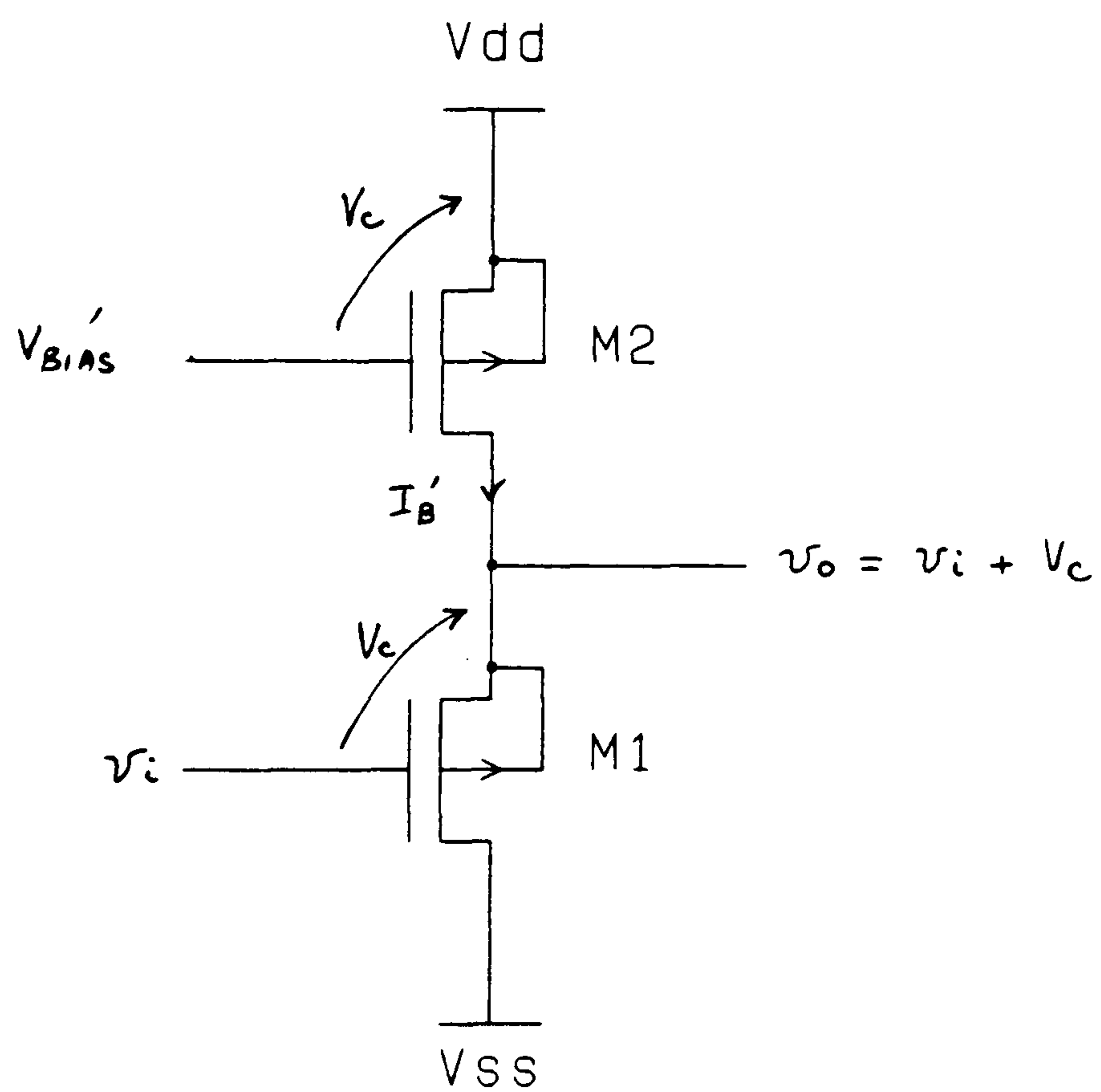


Figure 2.2: P-channel source follower

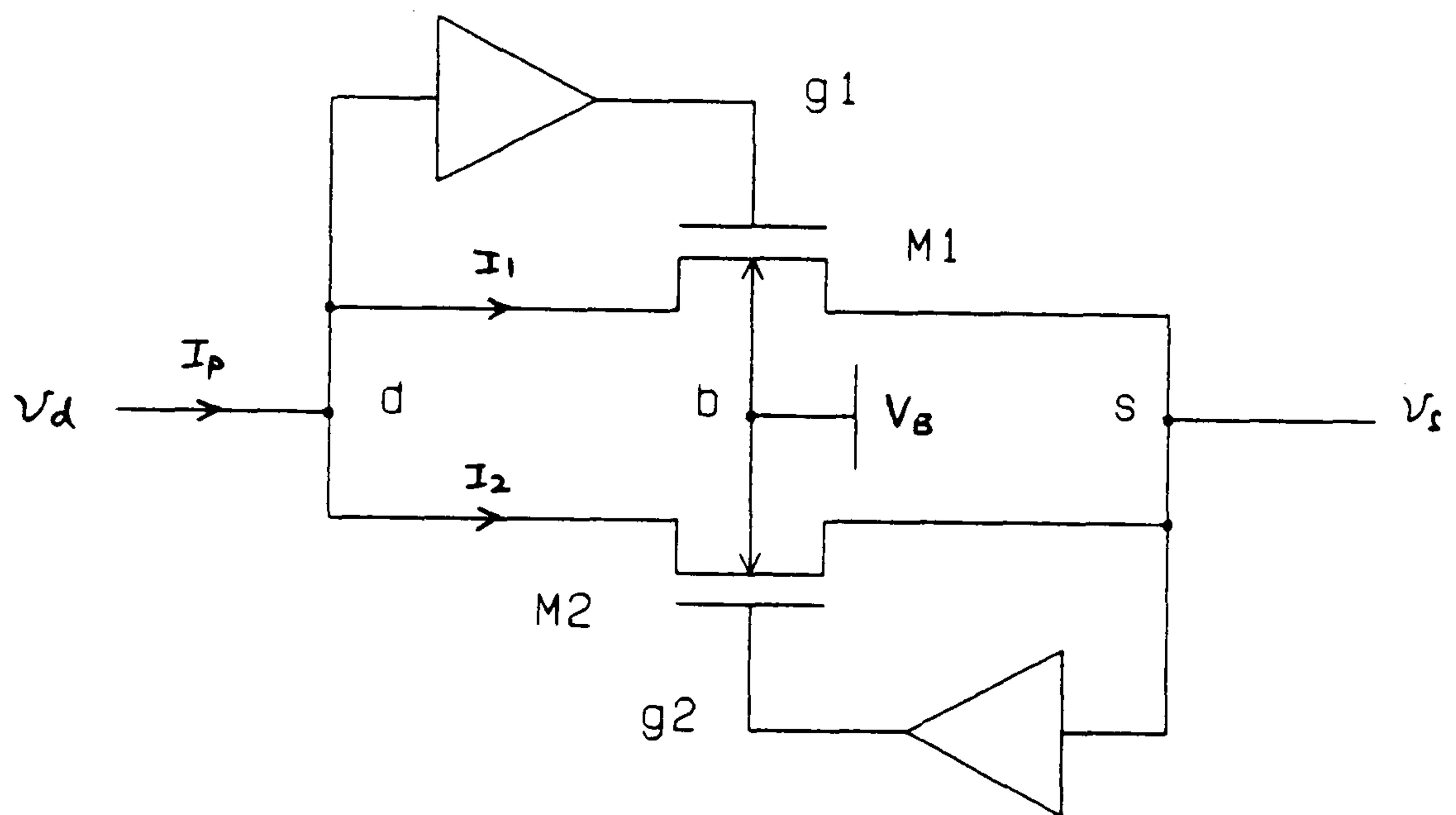
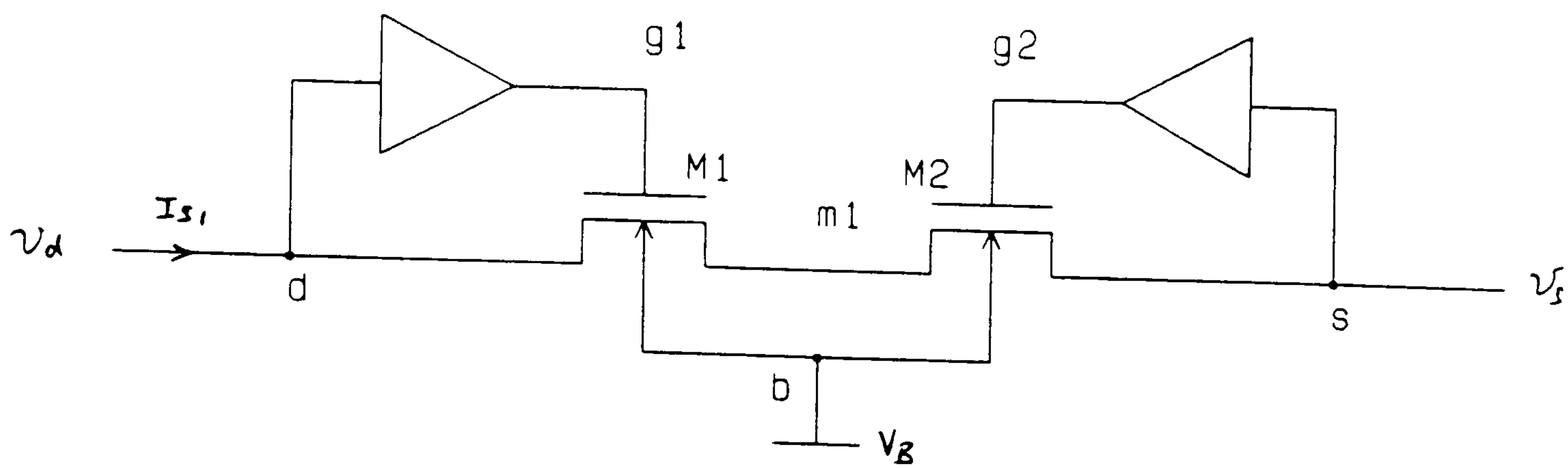
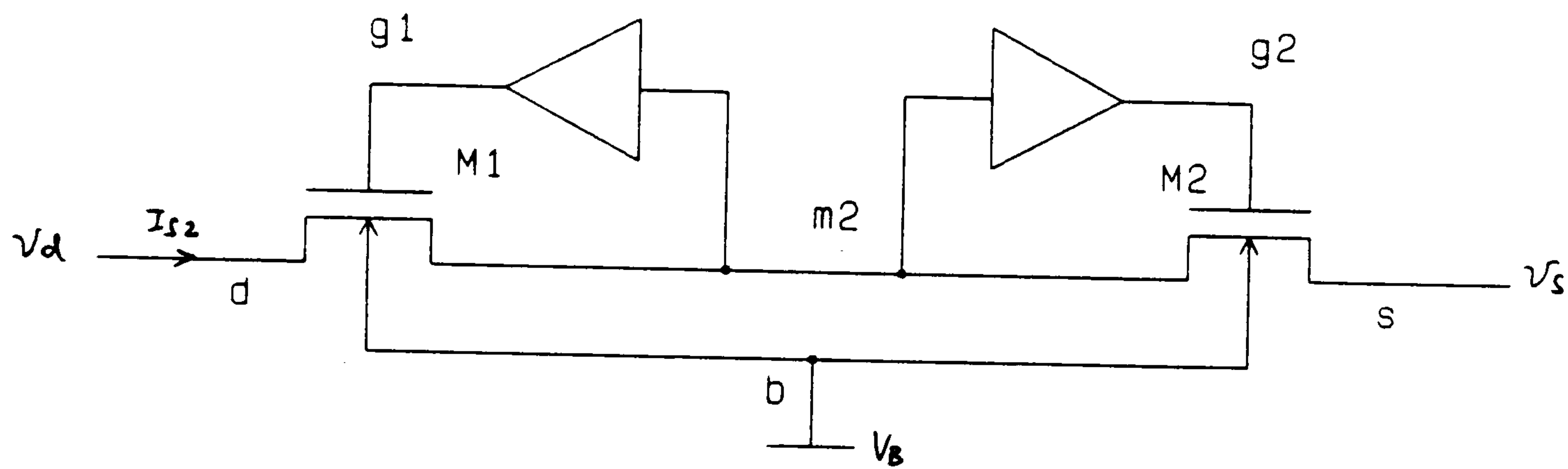


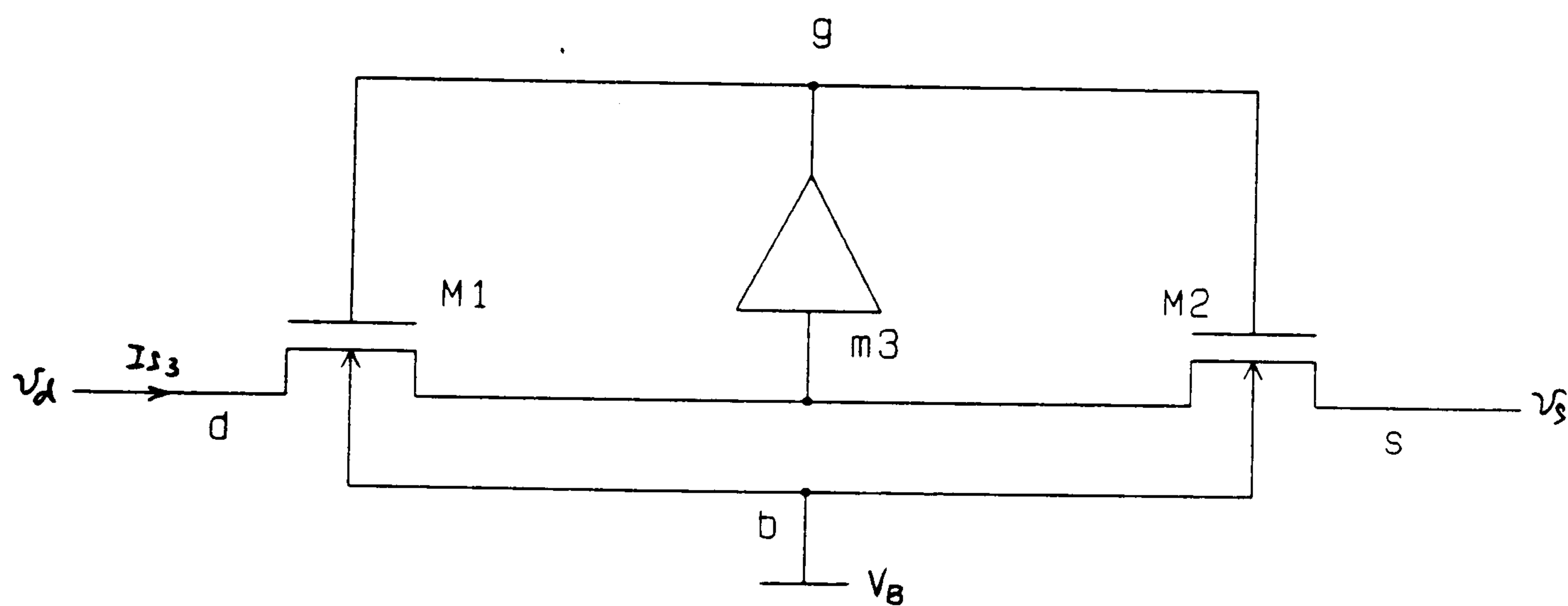
Figure 2.3: Schematic of unscaled-gate compensation parallel-form resistor



(a) SPR-I

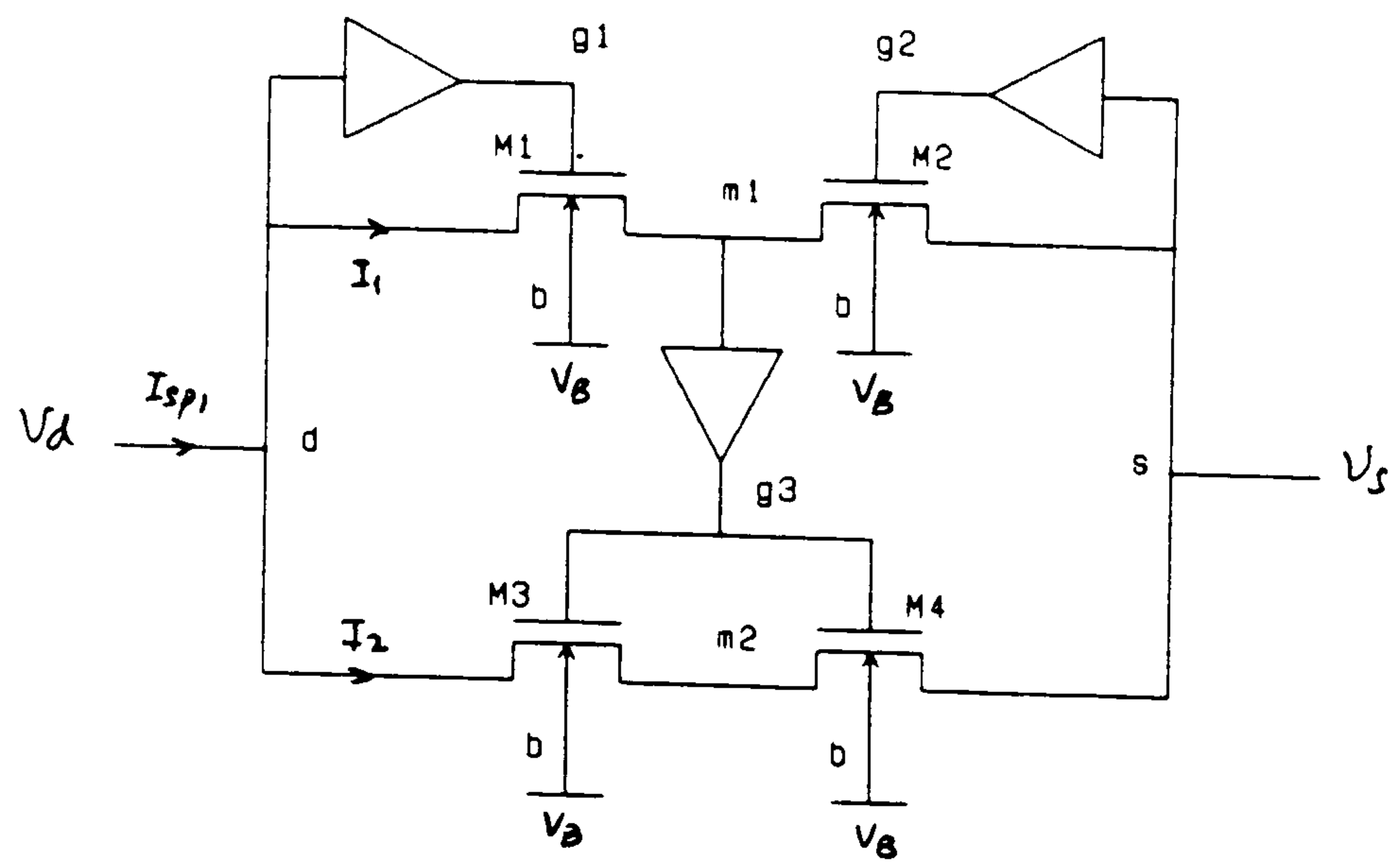


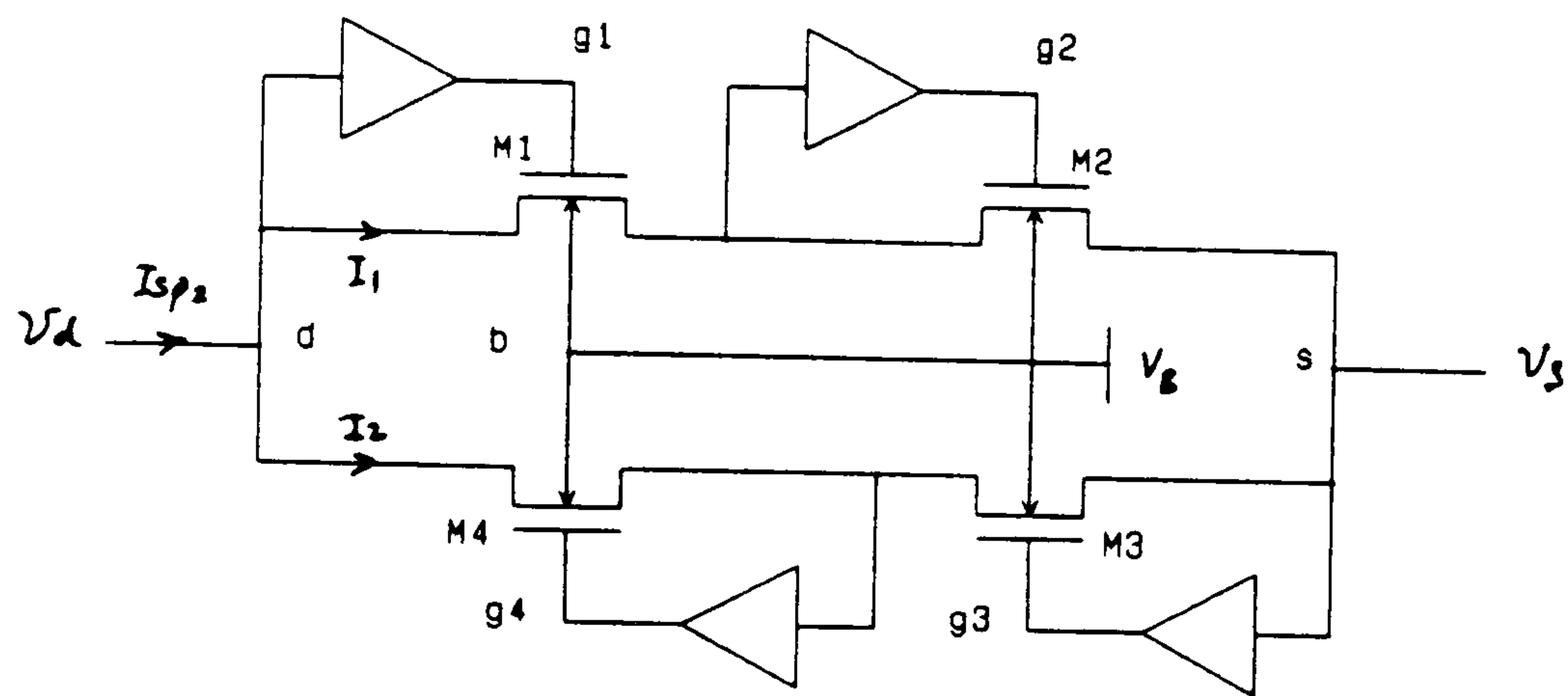
(b) SPR-II



(c) SPR-III

Figure 2.4: Schematic of unscaled-gate compensation series-pair resistors





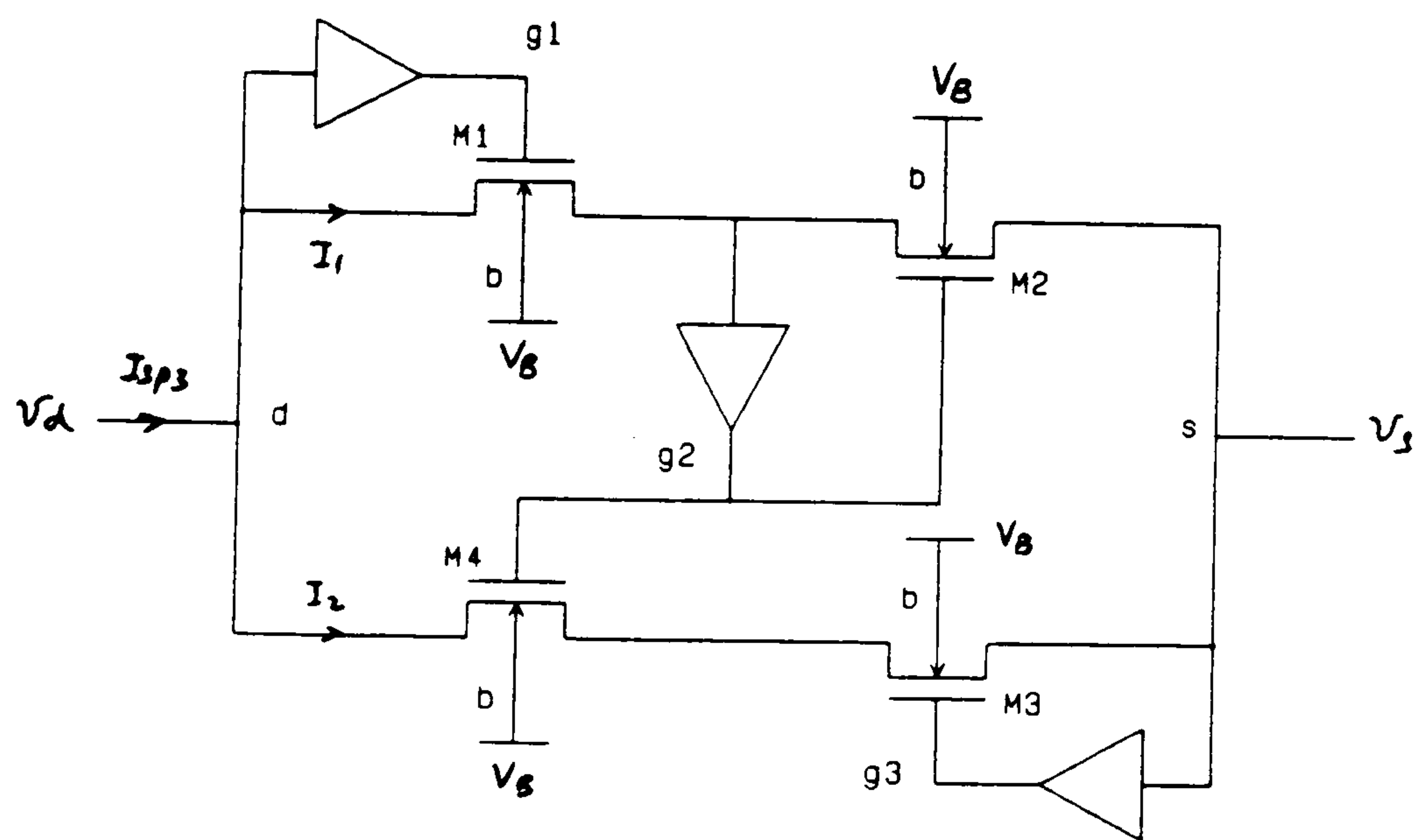


Figure 2.5: Schematic of unscaled-gate compensation series-parallel quad resistors

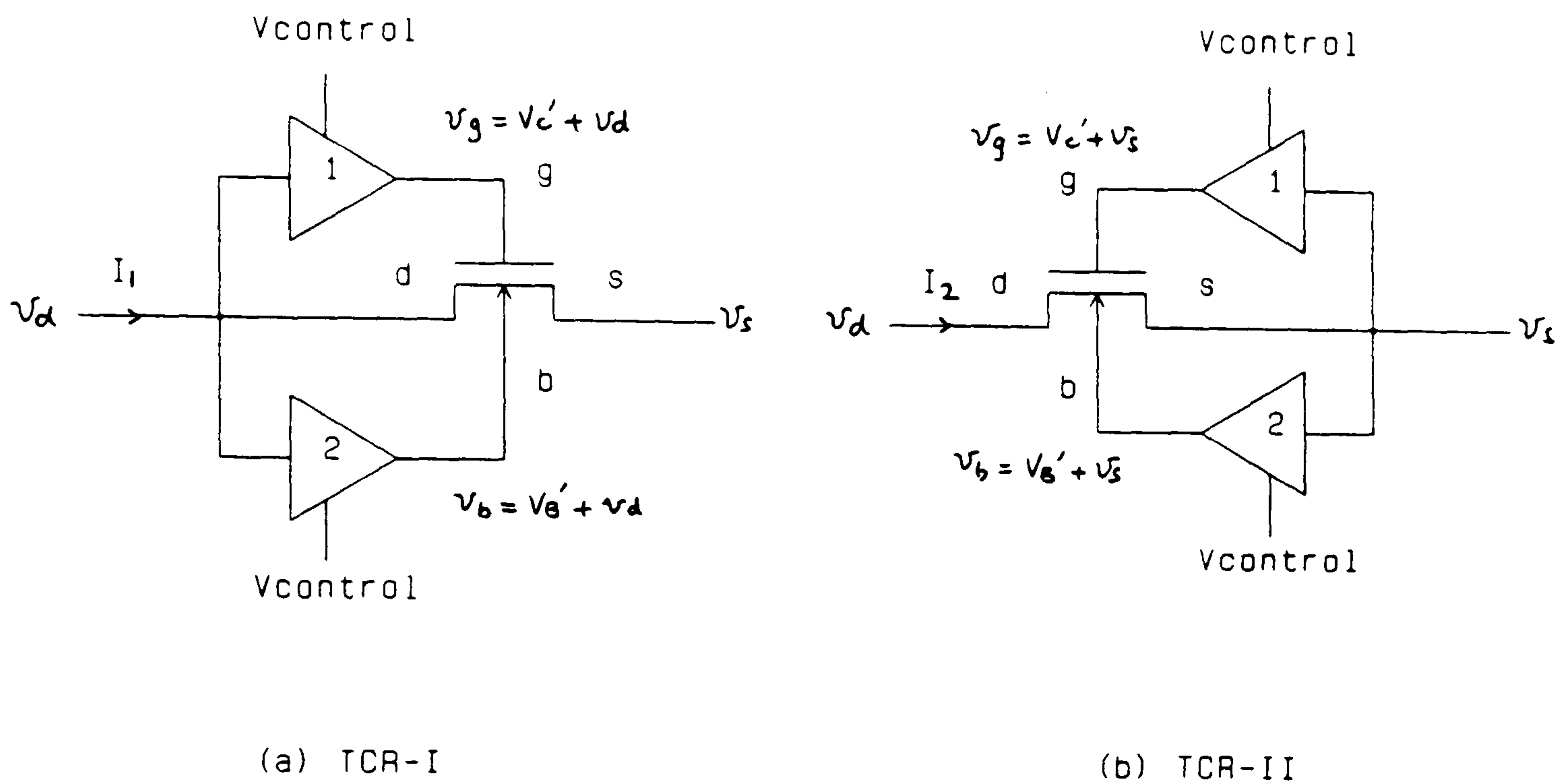


Figure 2.6: Dual gate-bulk compensation TCR-I and TCR-II

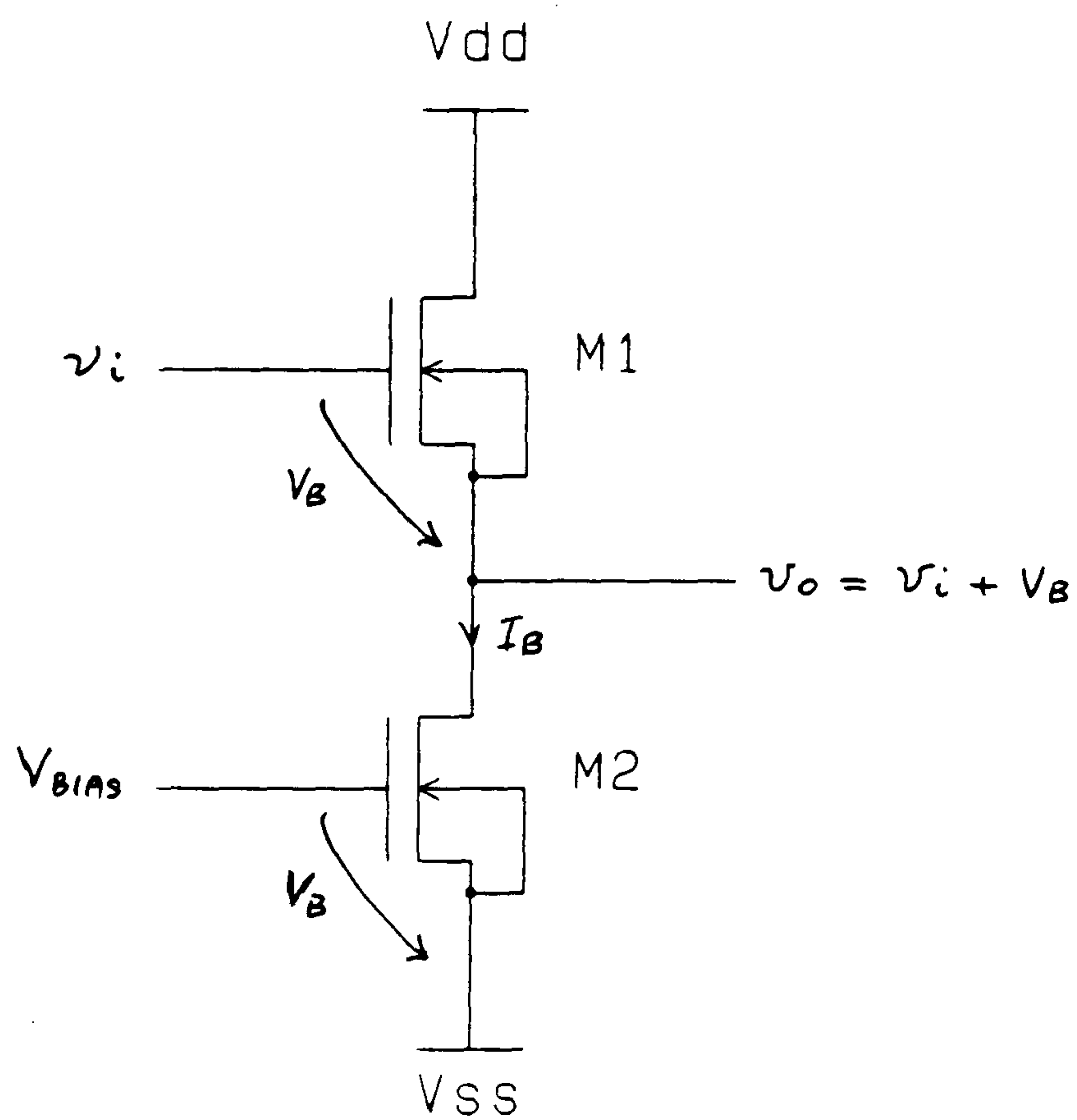


Figure 2.7: N-channel source follower

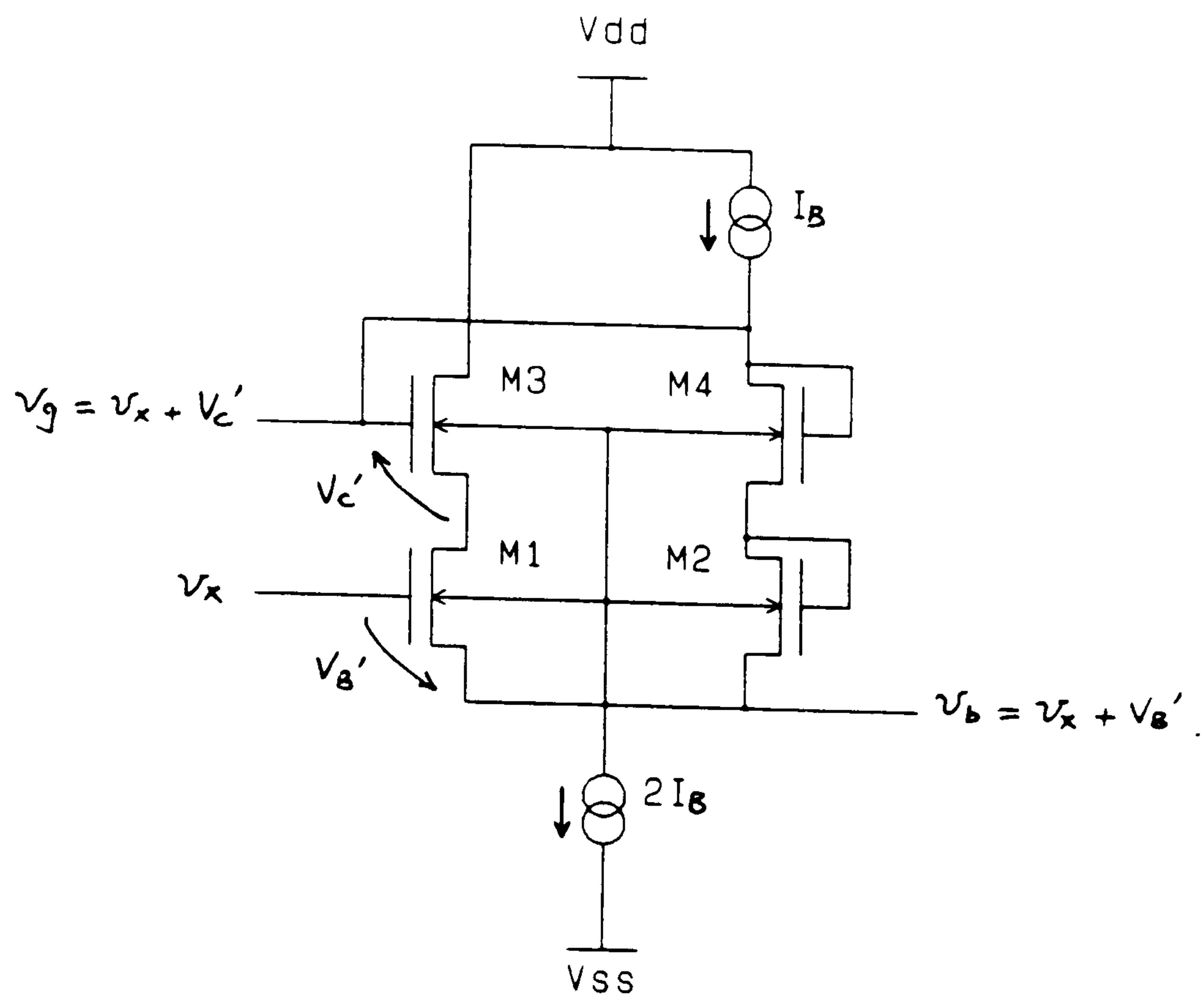


Figure 2.8: N-channel differential-pair-based level-shifting buffer

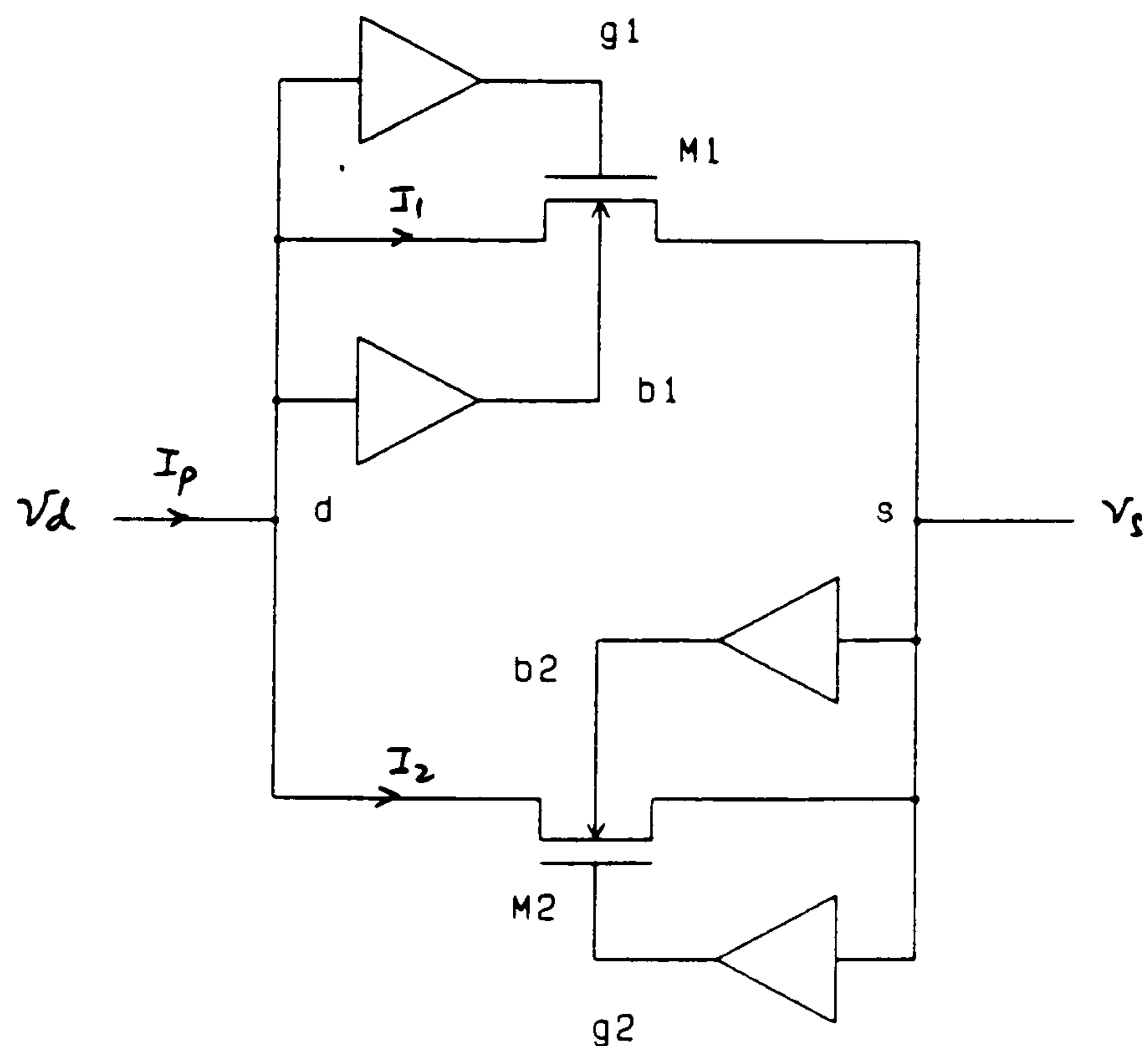
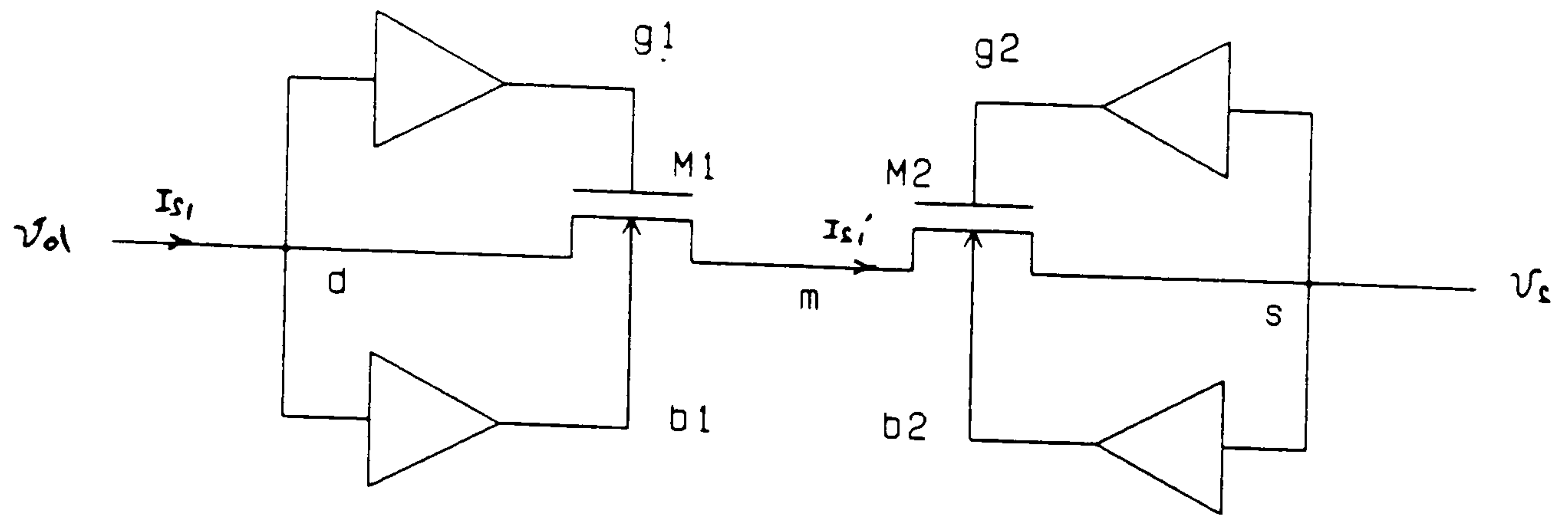
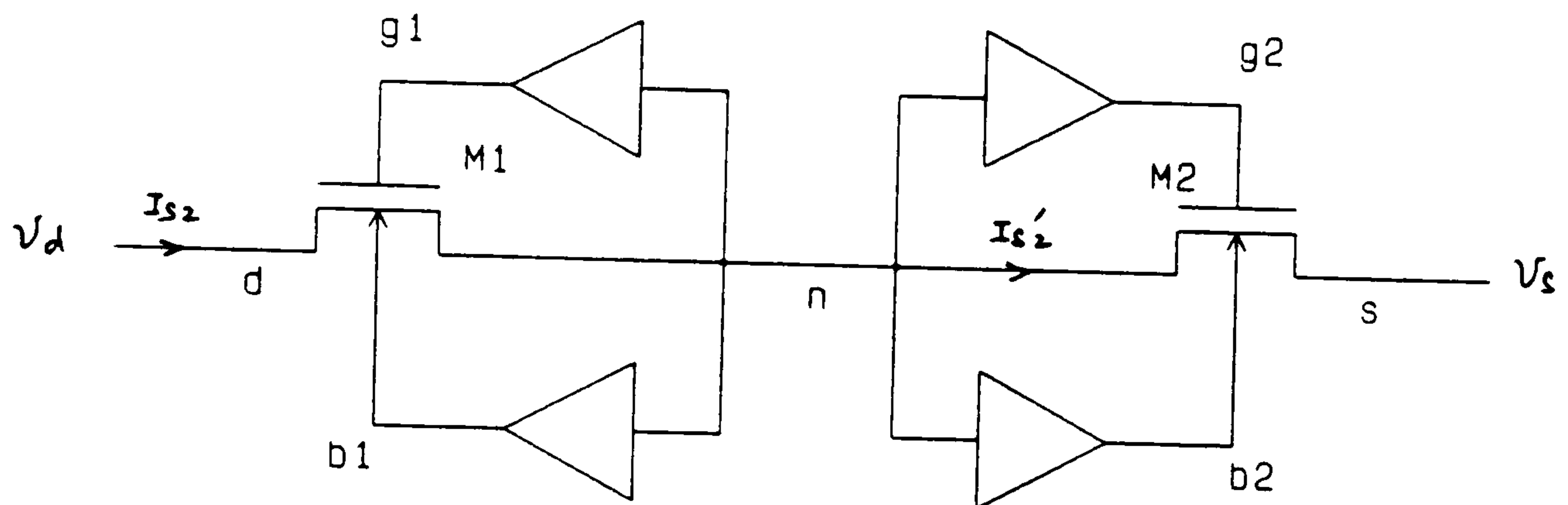


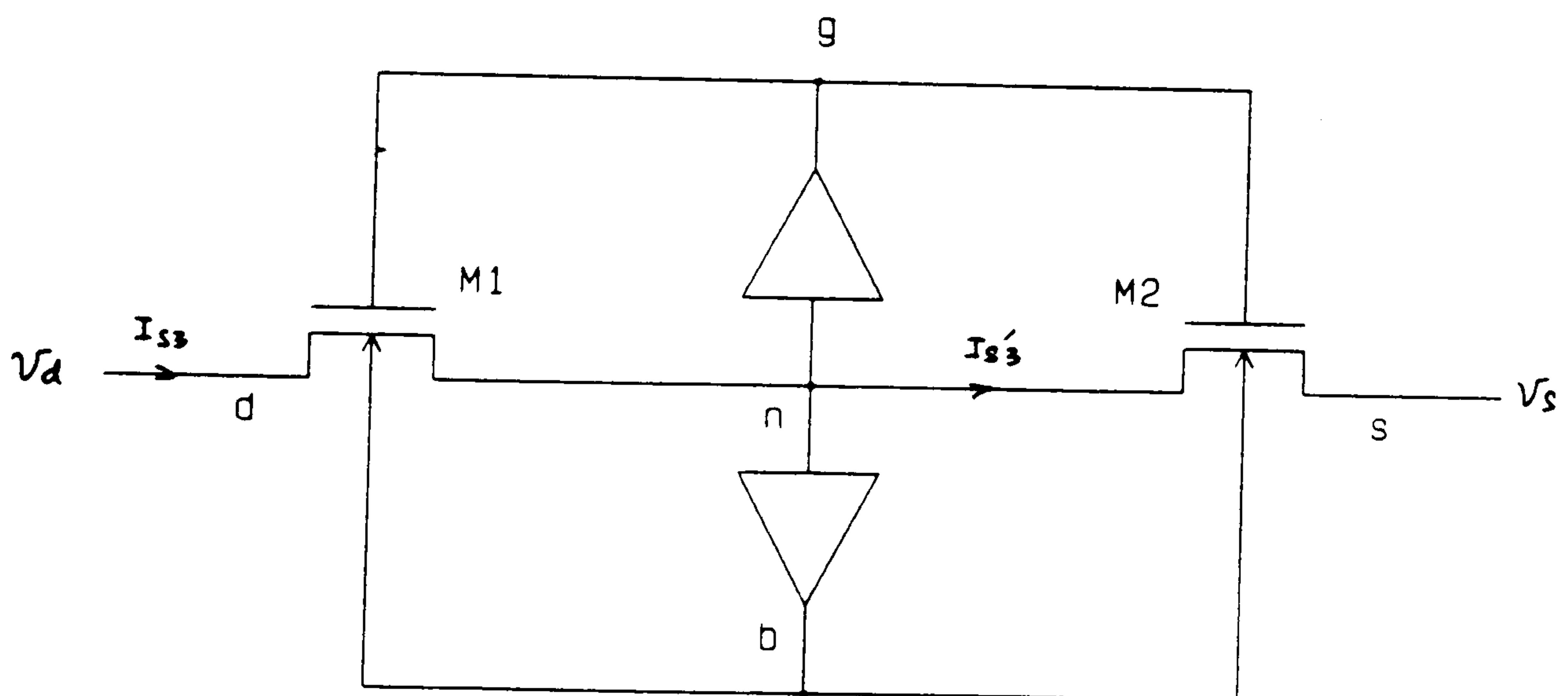
Figure 2.9: Schematic of dual gate-bulk compensation parallel-form resistor



(a) SPR-I

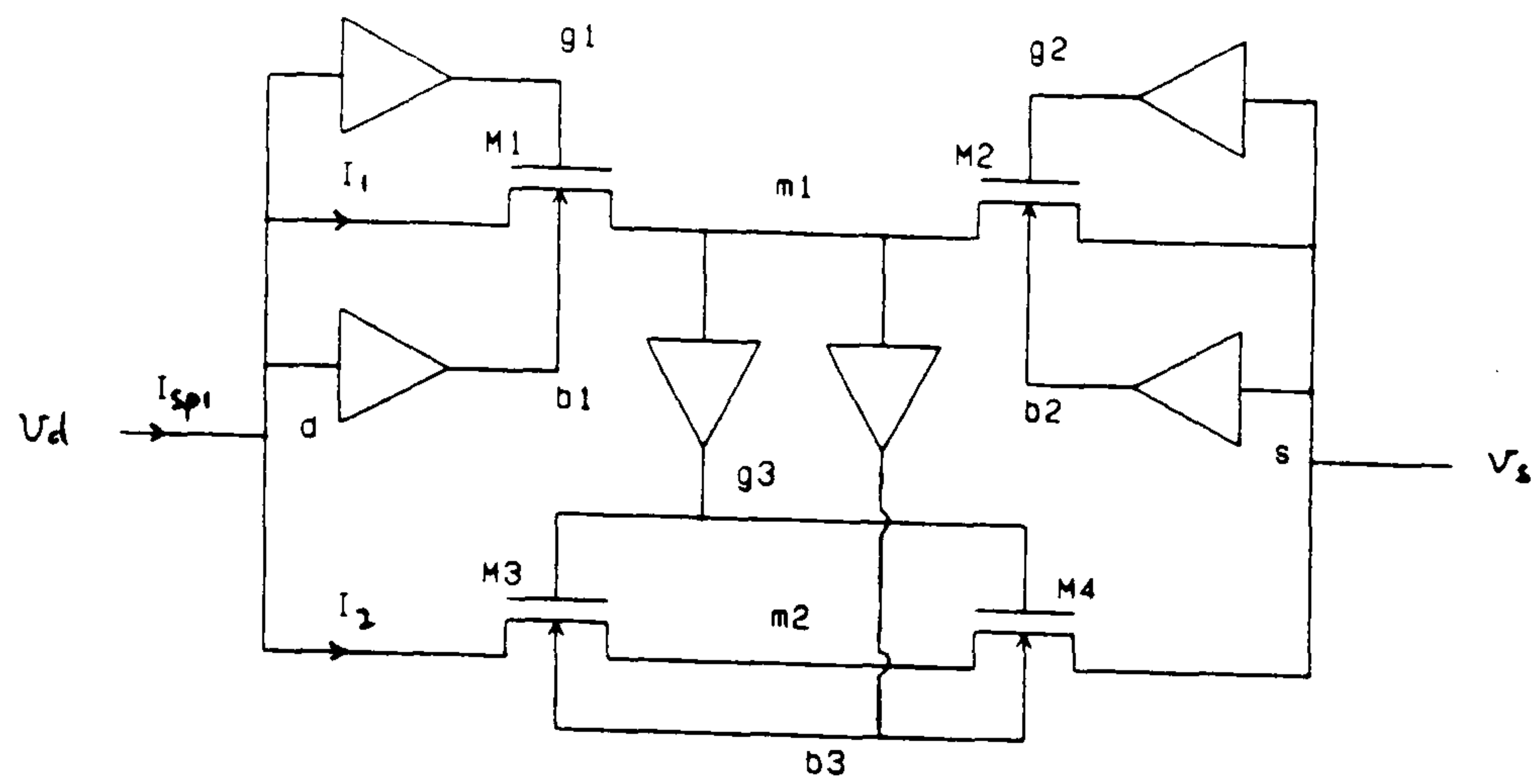


(b) SPR-II

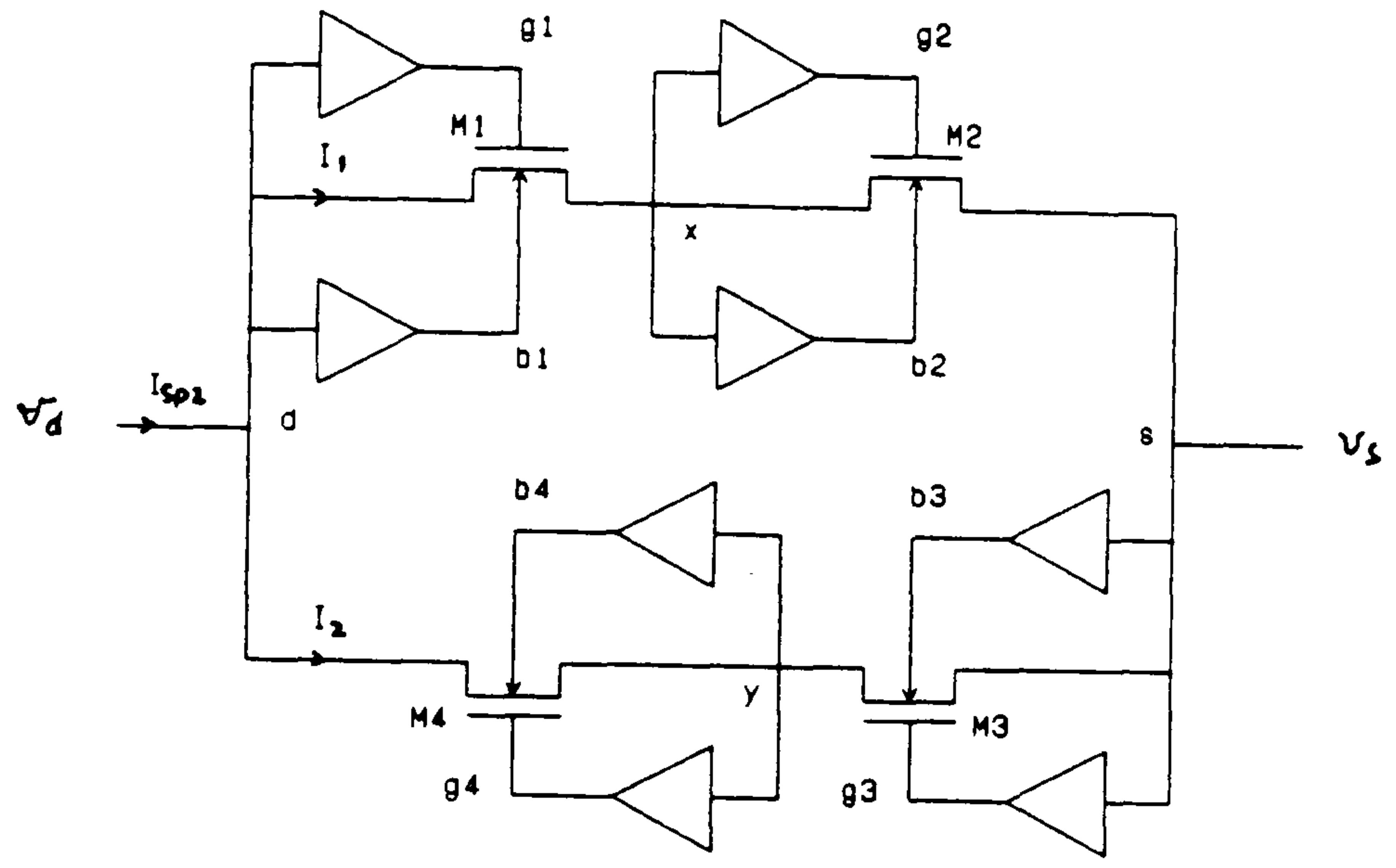


(c) SPR-III

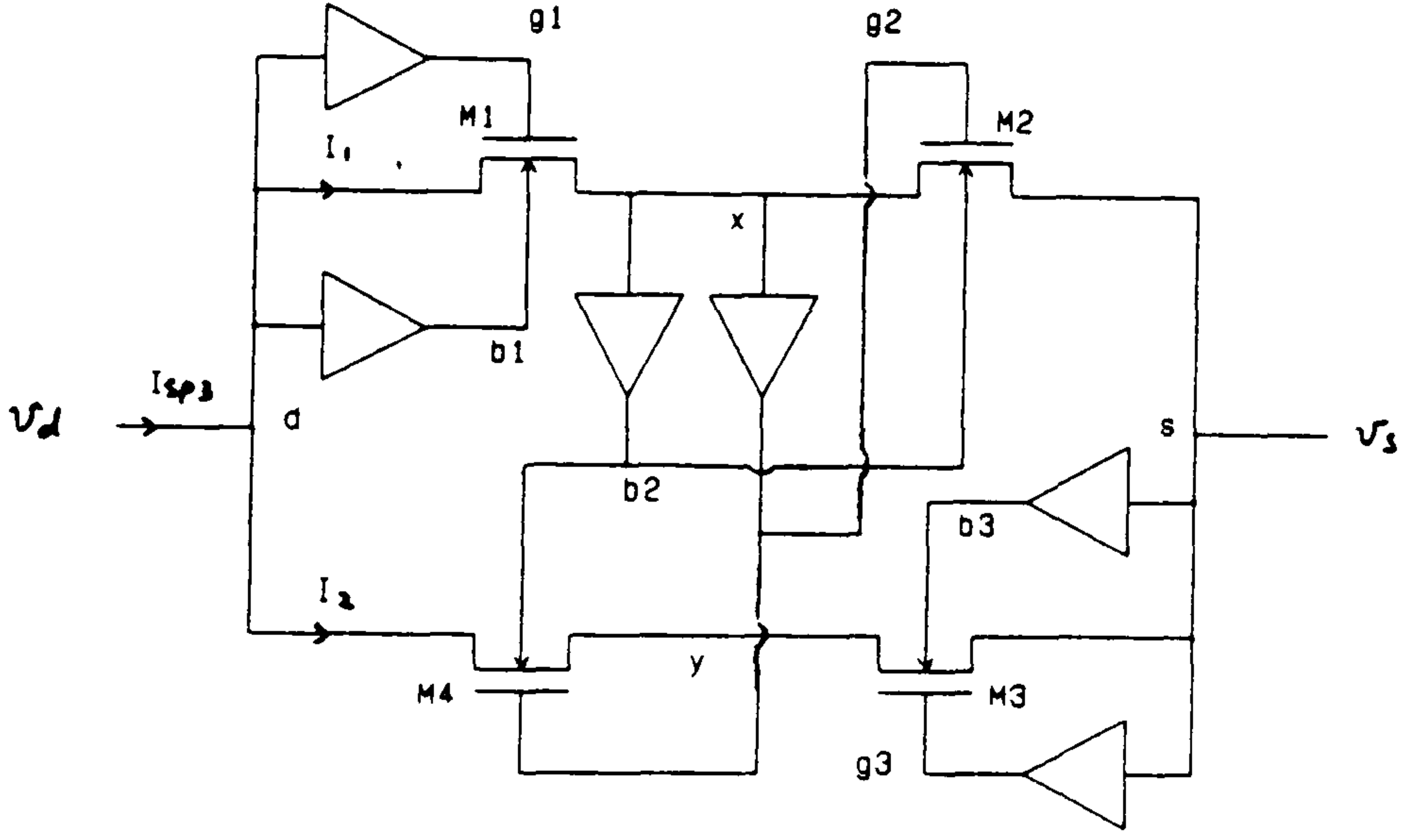
Figure 2.10: Schematic of dual gate-bulk compensation series-pair resistors



(a) SPQR-I



(b) SPQR-II



(c) SPQR-III

Figure 2.11: Schematic of dual gate-bulk compensation series-parallel quad resistors

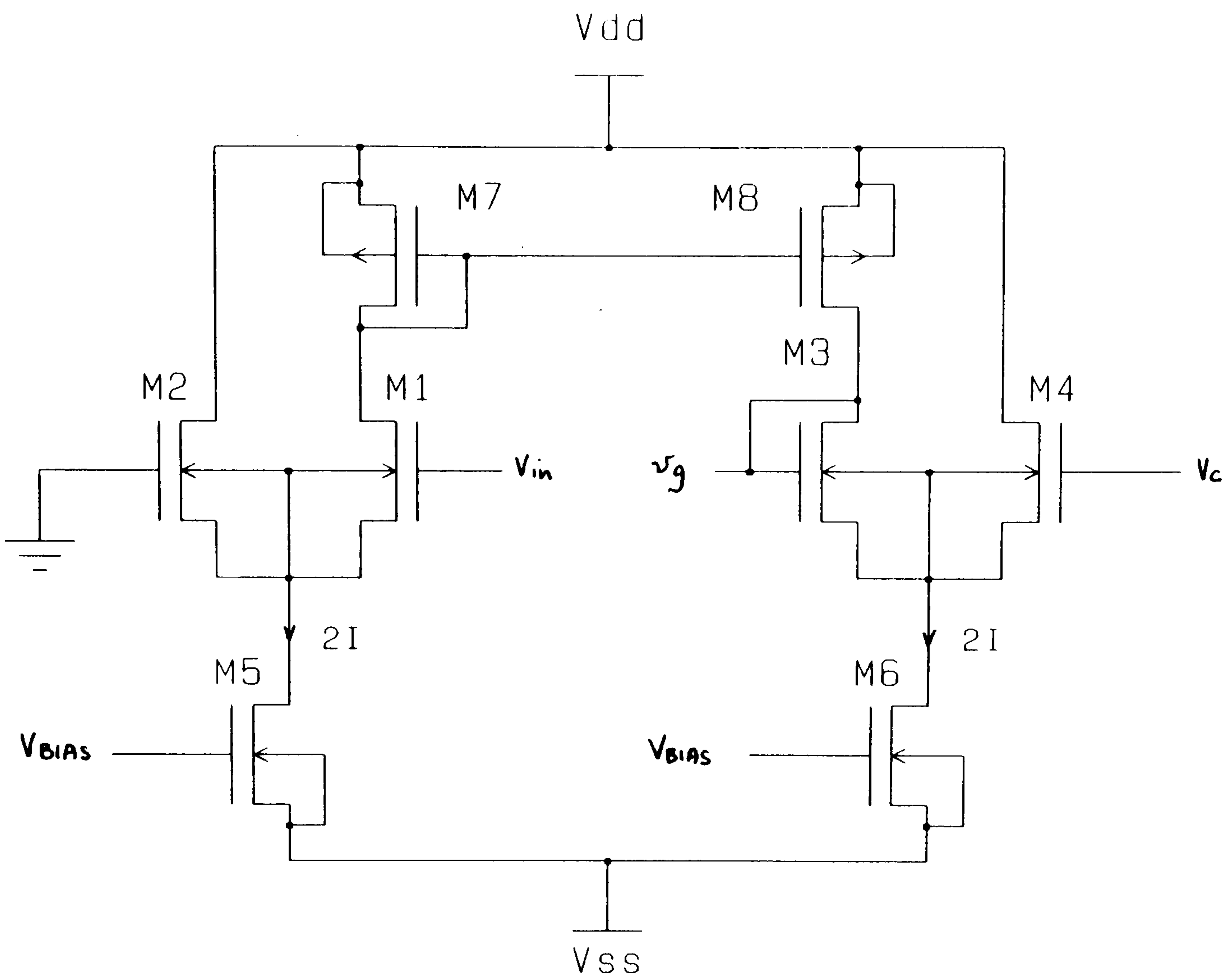


Figure 2.12: Circuit diagram of scaled signal generator

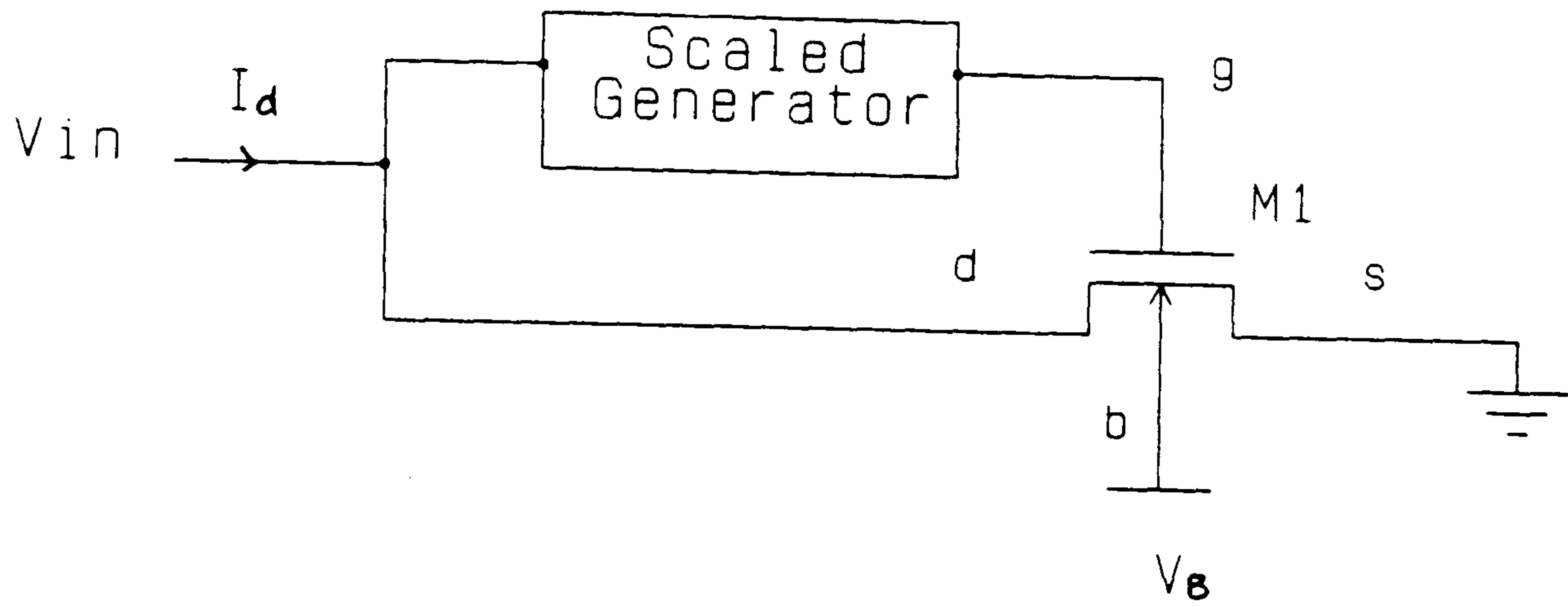


Figure 2.13: Schematic of scaled-gate compensation grounded resistor

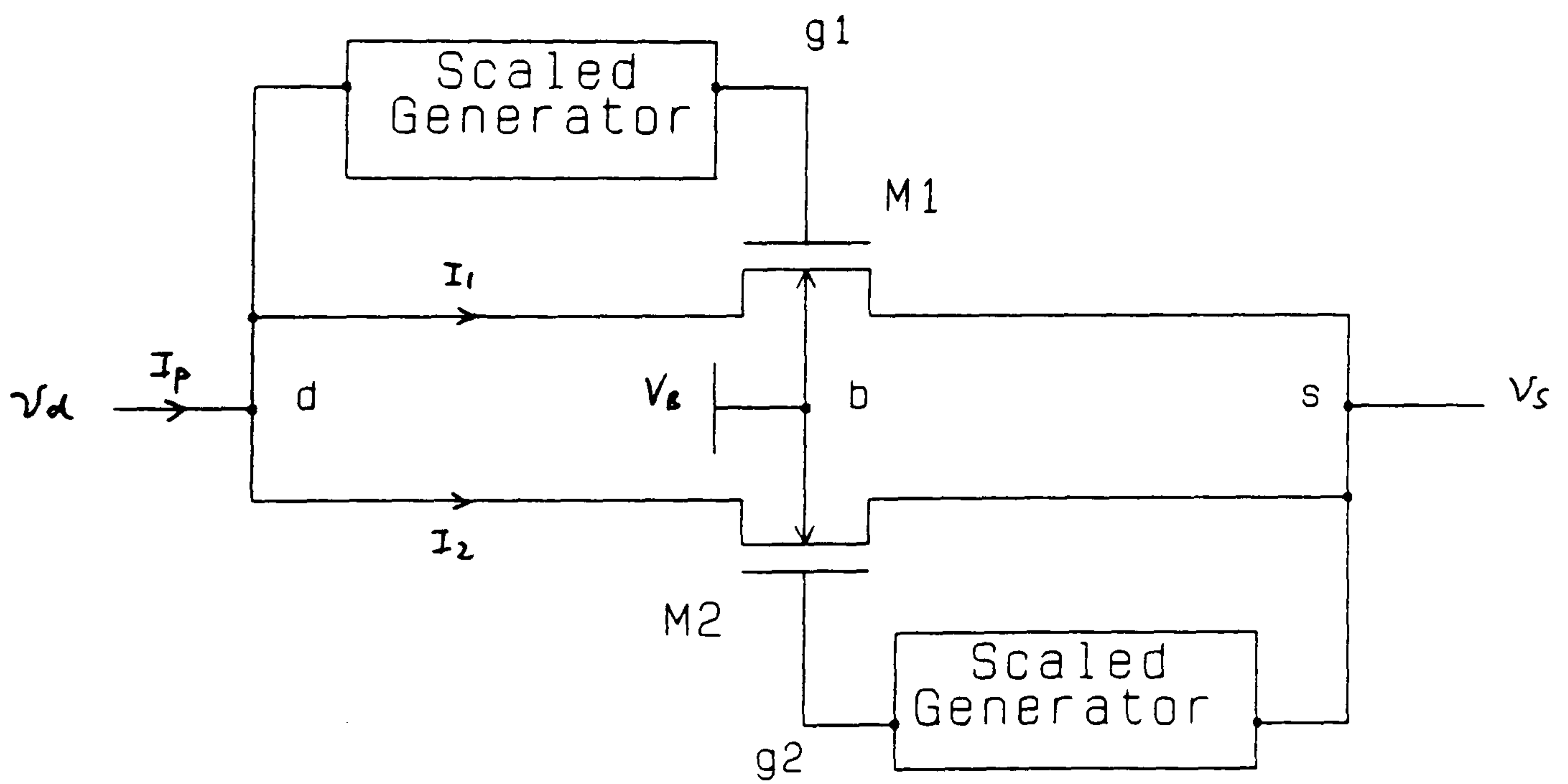


Figure 2.14: Schematic of scaled-gate compensation floating resistor

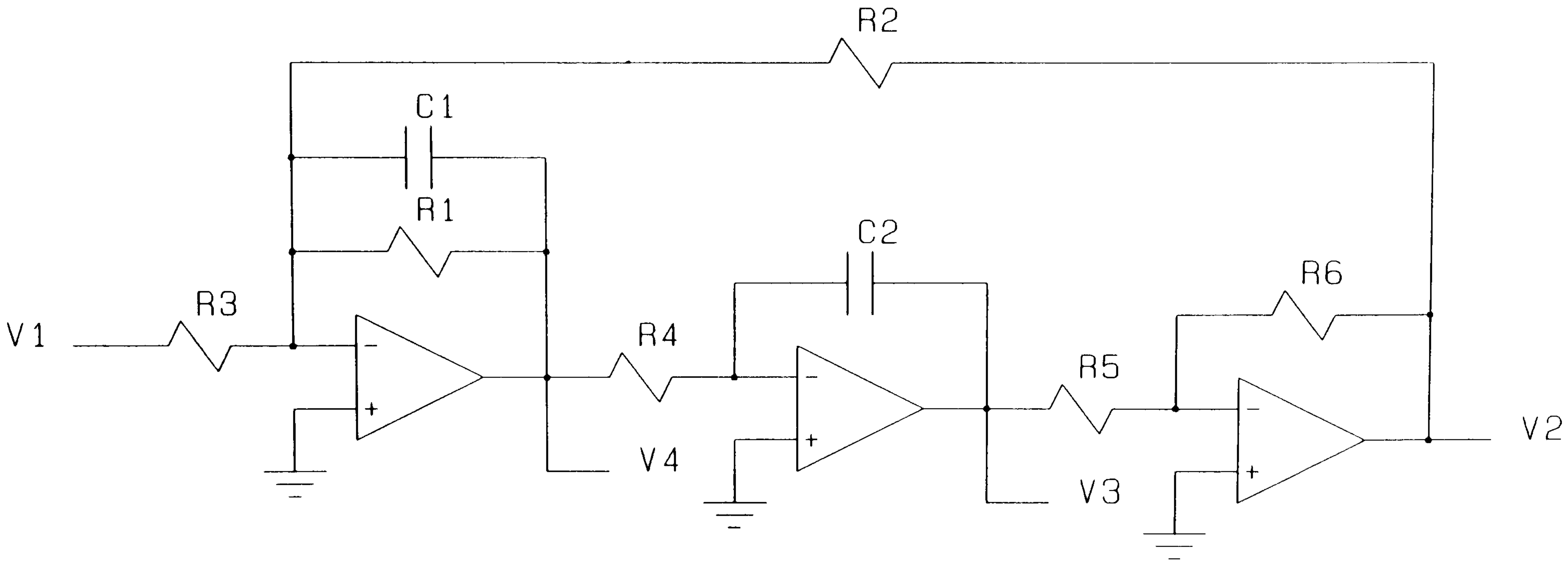


Figure 2.15: Circuit diagram of the Tow-Thomas second-order filter

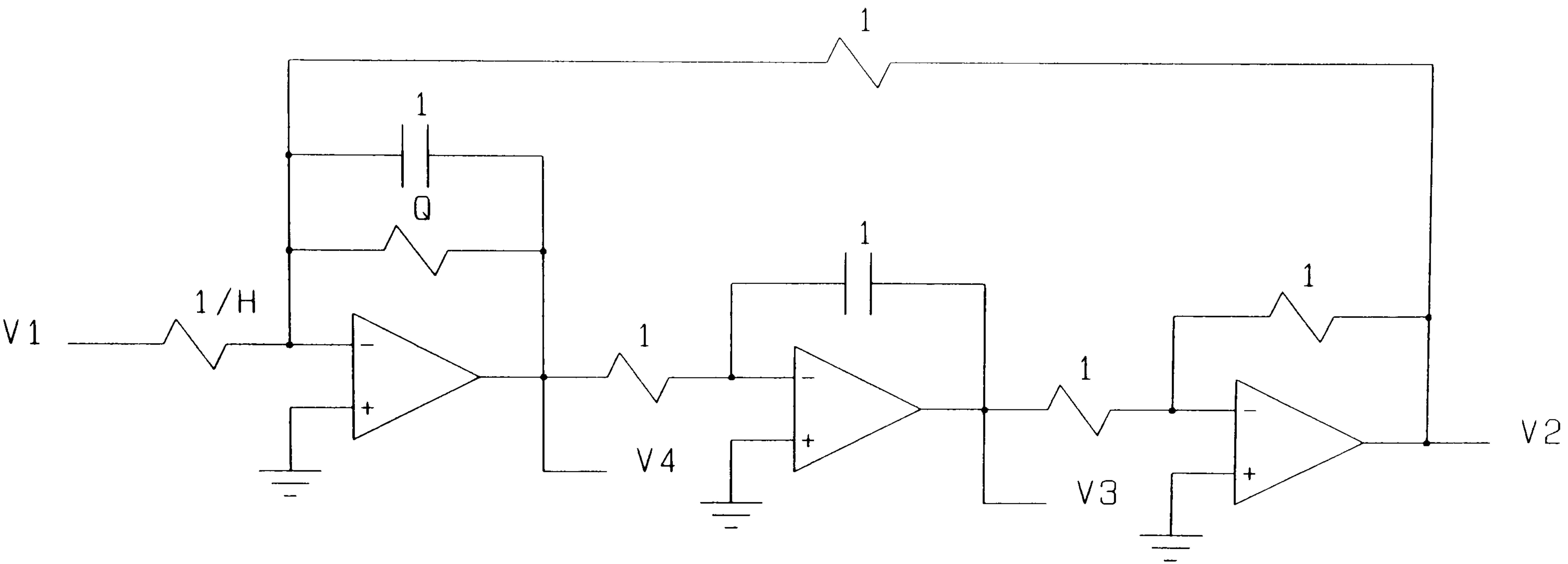


Figure 2.16: Normalised Tow-Thomas second-order filter

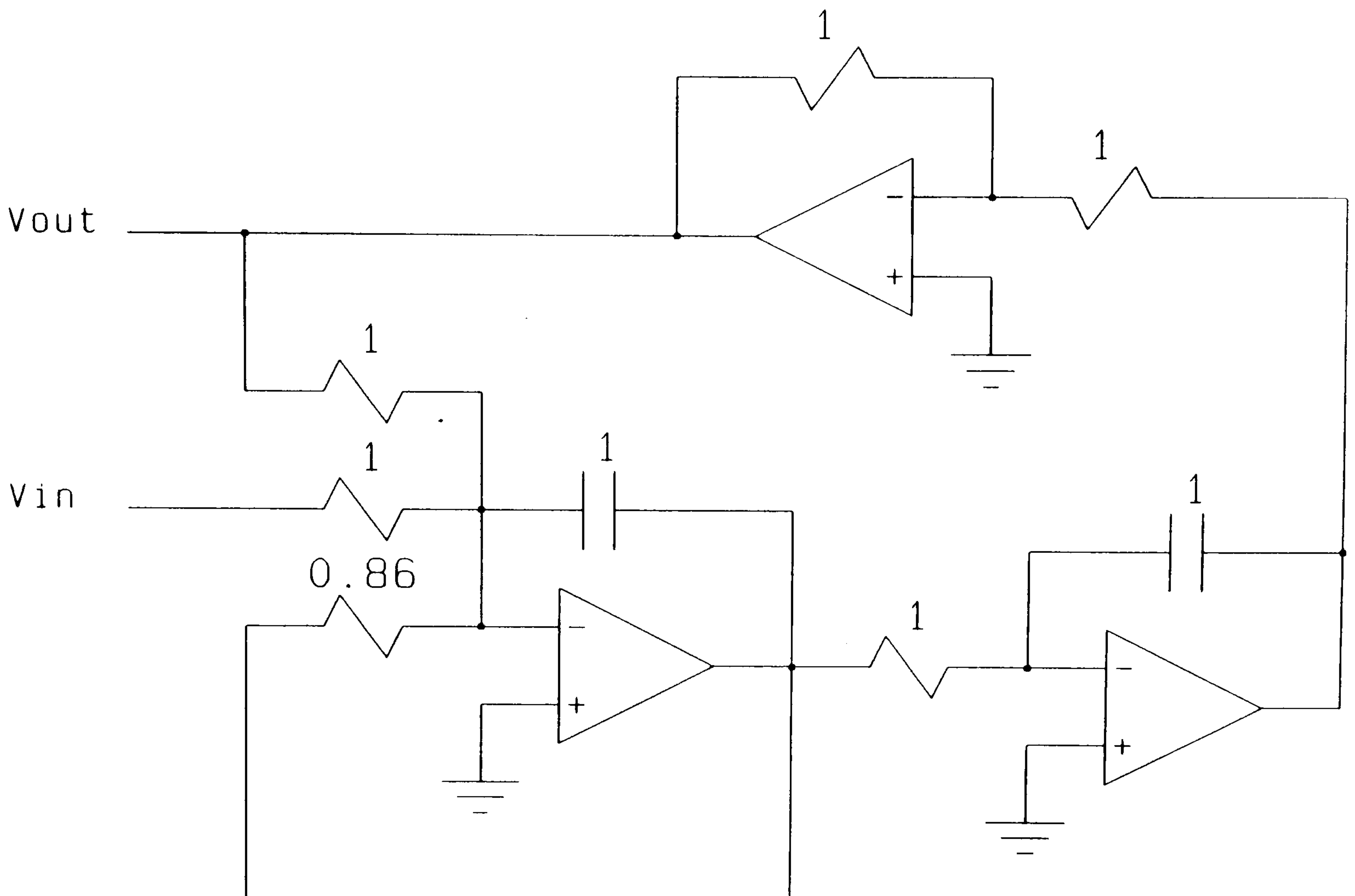


Figure 2.17: RC Tow-Thomas second-order filter at normalised values (Q=0.86)

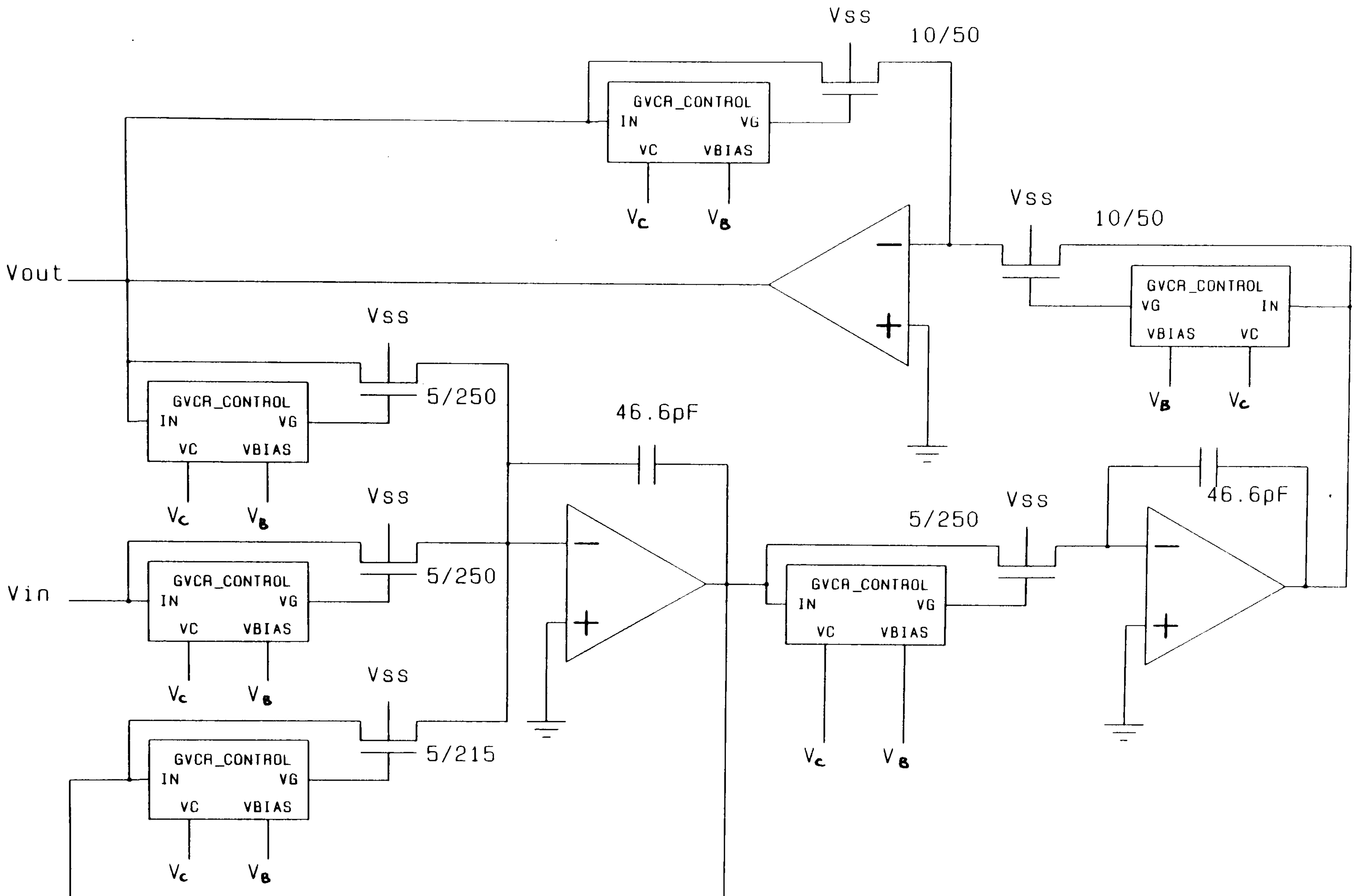


Figure 2.18: GVCR-based Tow-Thomas second-order filter, according to Fig. 2.17

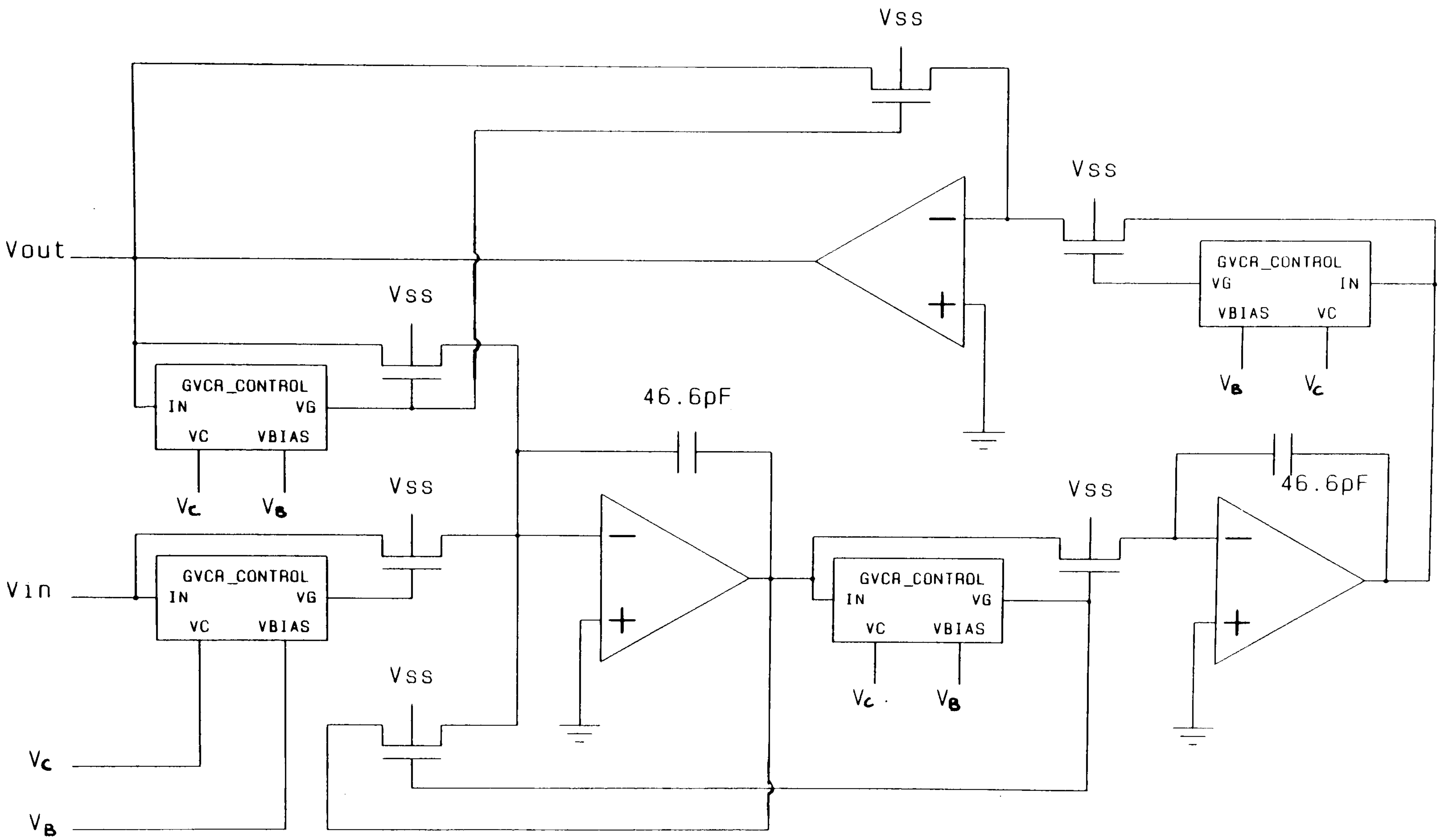


Figure 2.19: Simplified GVCR-based Tow-Thomas second-order filter

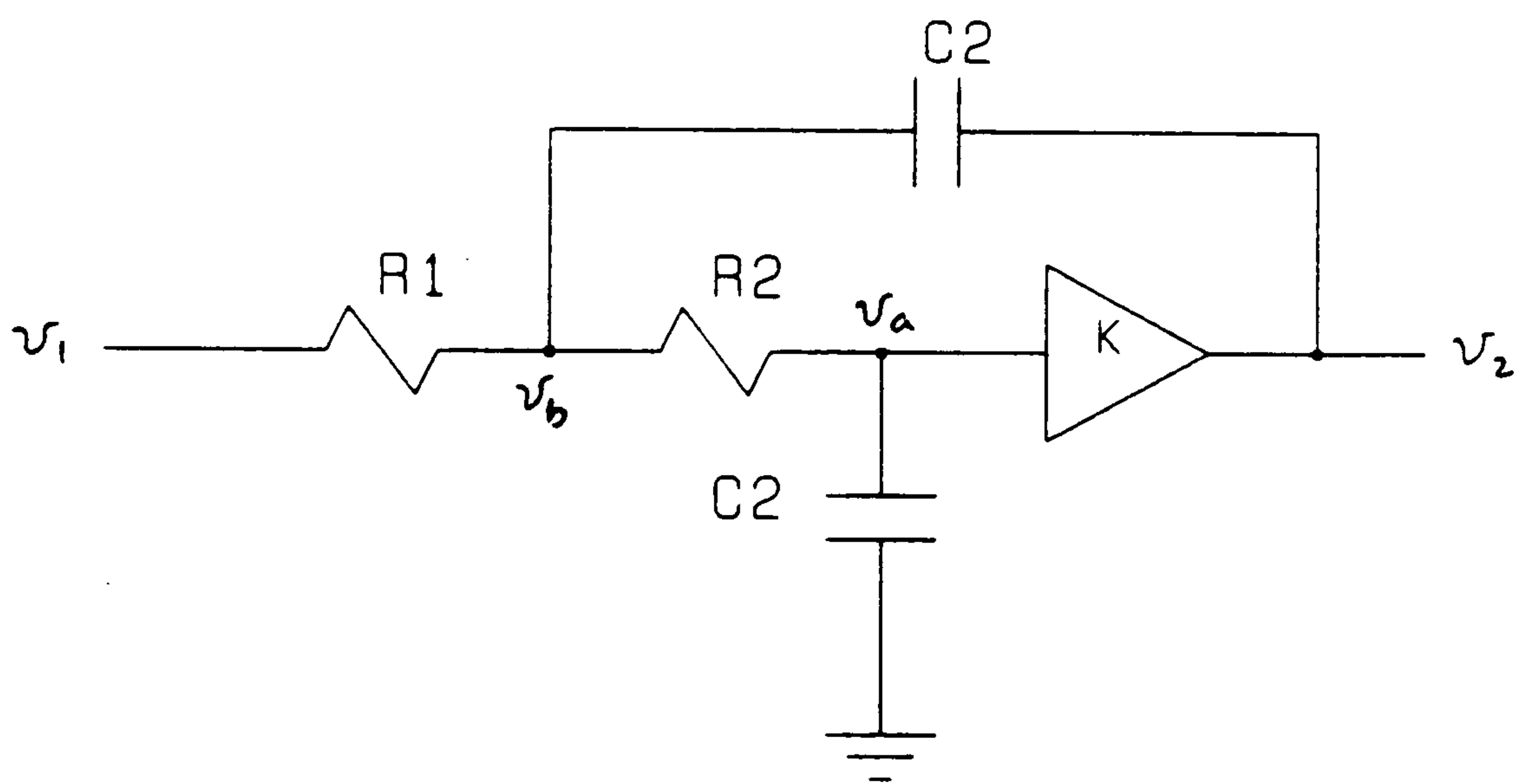


Figure 2.20: Second-order Sallen-Key lowpass filter

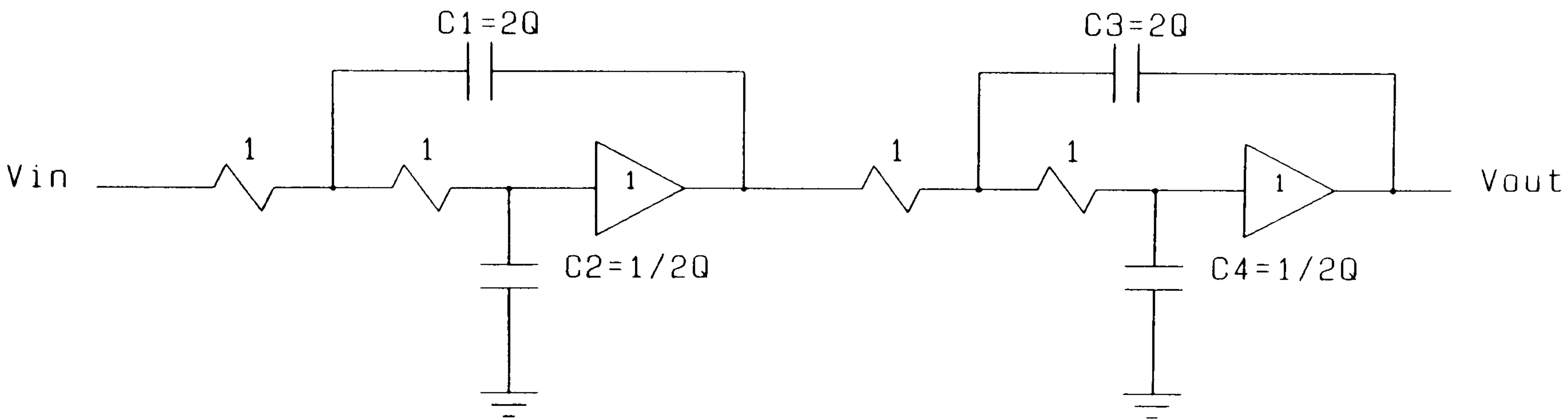


Figure 2.21: Fourth-order lowpass Butterworth

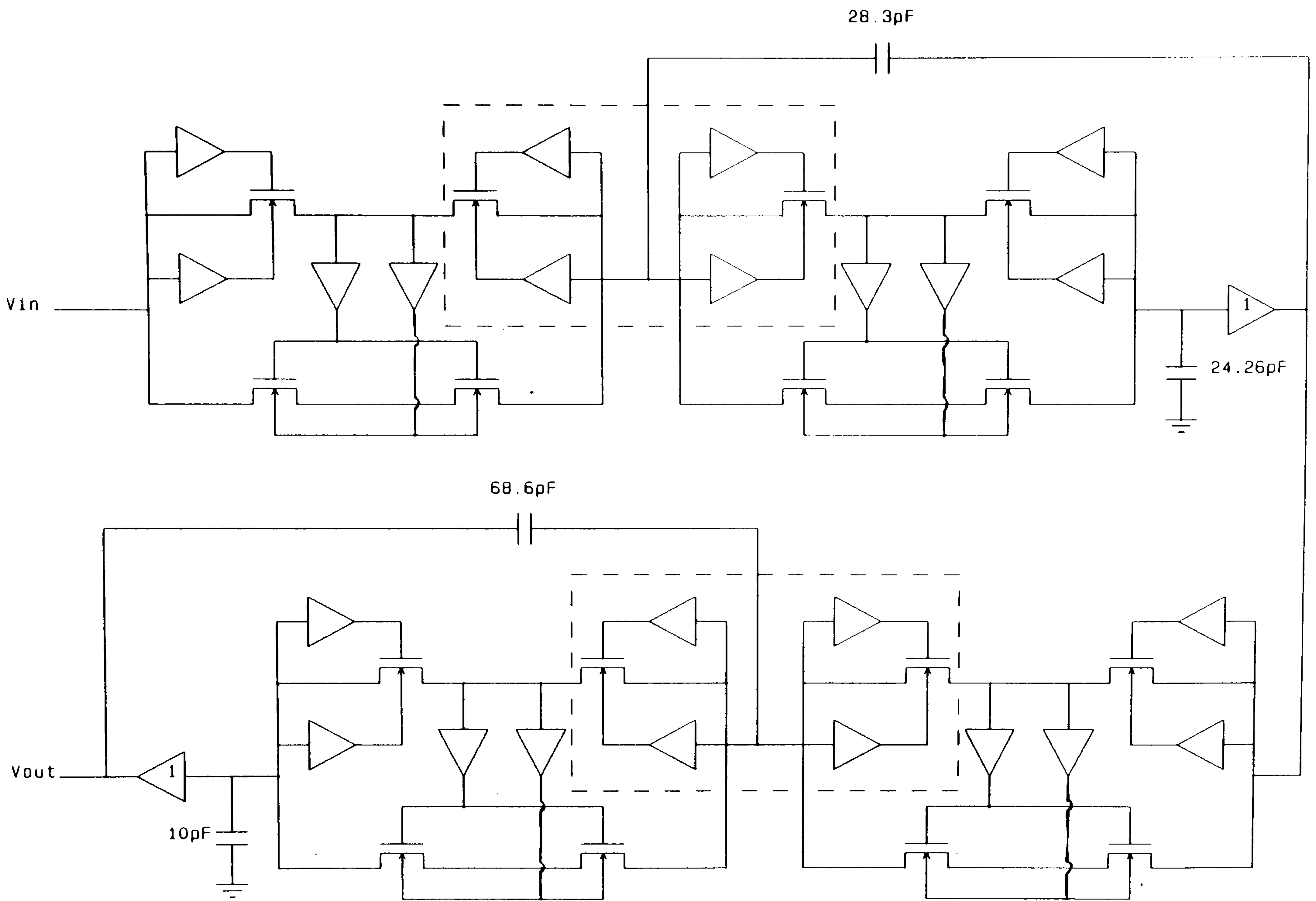


Figure 2.22: Fourth-order SPQR-based Sallen-Key lowpass filter

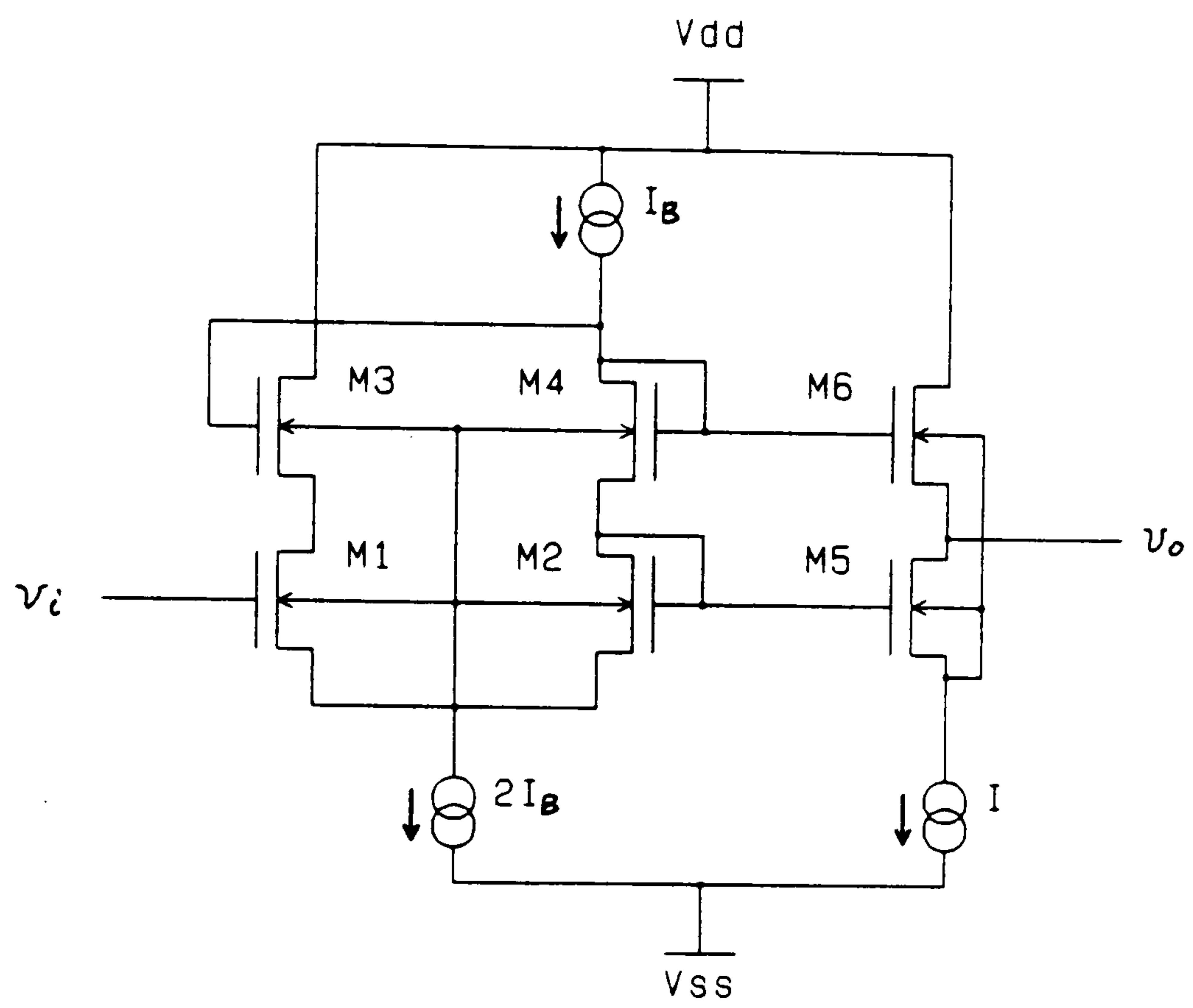


Figure 2.23: Modified VanPeteghem-Rice unity-gain buffer

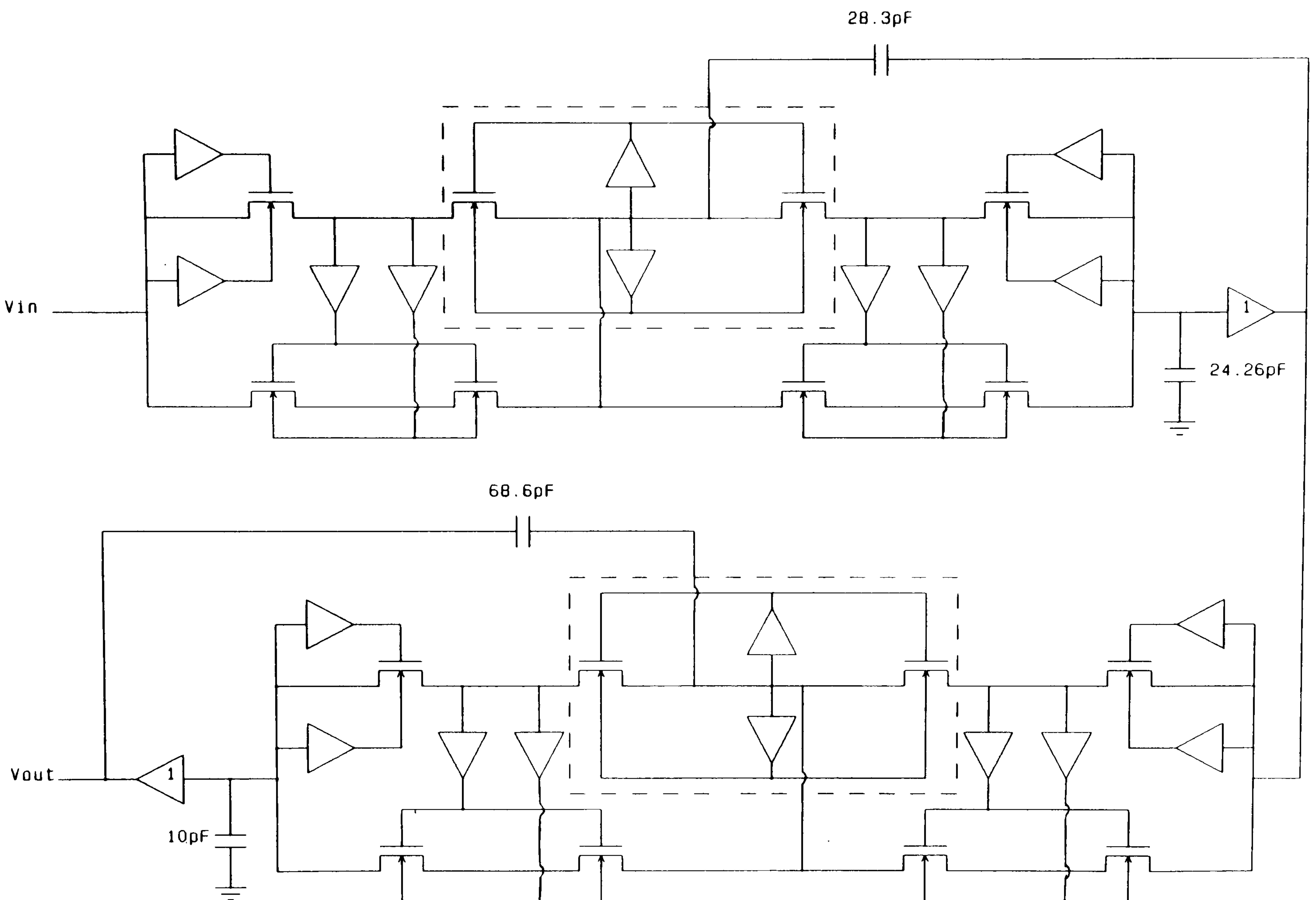


Figure 2.24: Simplified fourth-order Salley-Key lowpass filter

Chapter 3

Performance Comparison of MOS Resistor Circuits

In this chapter, emphasis is placed on evaluating the performance of each resistor in terms of distortion level, signal handling capability, silicon area, power consumption, and bandwidth etc. . The relative advantages and disadvantages are also compared. This invariably suggests a trade-off when attempting to select a particular resistor structure for analogue signal-processing tasks. Simulation and experimental results related to application examples are presented and explained. It is shown that the results agree very well with the theory and observations.

3.1 Simulation Results

3.1.1 Unscaled-Gate Compensation Resistors

SPICE simulations using realistic Level-3 transistor models with gate-voltage-dependent mobility have been performed. Appendix B presents the Plessey $2\mu m$ P-well CMOS process parameters used in these simulation examples. In an at-

tempt to make fair comparisons of the performance of PFR, SPR and SPQR structures, the aspect ratios have been chosen so as to obtain equal resistances. Thus, for a given channel width W, the PFR, SPR and SPQR channel lengths L_s, L_p and L_{sp} are required in a ratio of 4:1:2. In this case, the transistors were n type with $W = 10\mu m$, $L_p = 100\mu m$, $L_s = 25\mu m$ and $L_{sp} = 50\mu m$. The process parameters employed for n-channel transistors were $\theta = 0.15V^{-1}$ and $\gamma = 0.65V^{\frac{1}{2}}$. The respective p-channel source-follower-based buffers, shown in Fig. 2.2, were allocated identical dimensions with transistor aspect ratios of $10\mu m/20\mu m$.

Fig. 3.1→3.3 displays the family of static characteristics for the unscaled-gate-compensated PFR, SPR-III and SPQR-I shown in Fig. 2.3, 2.4(c) and 2.5(a), respectively. It may be seen that the the $I - V$ characteristics in the first and third quadrants are different. The third quadrant typically offers better linearity as well as equal spacing between each individual tuning voltage. The spacing of these curves demonstrates the extent to which the resistors can be tuned via control voltage V_C as defined in Fig. 2.2.

Fig. 3.4 assesses how the distortion varies with the change of resistance value for a $\pm 5V$ supply. The distortion was obtained by Fourier analysis of the signal current. Their simulated transfer characteristics combined with the distortion versus input signal ($1KHz$) at a nominal resistance of $185.2K\Omega$ are plotted in the Fig. 3.5 and Fig. 3.6, respectively. As predicted in Section 2.2, these results confirm that the PFR and SPQR have identical dominant quadratic distortion while the SPR suffers from an additional bias-dependent cubic nonlinearity being a function of both the gate-overdrive bias and signal level.

Table 3.1 summarises the relative performance including the distortion resulting from worst-case mismatches. The mismatch study reveals that even for a $\pm 2\%$

worst-case mismatch, there is no significant change in the total harmonic distortion for each resistor. The unscaled-gate compensation resistors are insensitive to geometrical mismatches because the body-effect quadratic distortion term dominates the overall distortion and masks the effect of mismatching. The influence of mobility degradation has been studied by increasing the mobility degradation factor up to 0.4. It should be noticed that this is an exceptionally high value. The simulation results for this situation are shown in Fig. 3.7→3.8 and Table 3.2, respectively. It is clearly observed that mobility degradation effect slightly offsets the THD performance of PFR amongst others. This is mainly due to the fact that each device in the PFR has the full gate-to-source signal potential applied across it rather than approximately half as in the SPR-III and SPQR-I. Since the increase of THD levels due to the increase of mobility factor in the three resistor cases (Table 3.1 and Table 3.2) is small, it can be deduced that for 'resistors' mobility degradation is not a key factor in the overall distortion.

With reference to Table 3.2, the power consumption (assuming that these resistor structures employ identical buffer structures with equal aspect ratio dimensions) obtained for the PFR, SPR-III and SPQR-I is related in a ratio of 2:1:3. The low power consumption of the SPR-III reflects its simplicity and smaller component count. Furthermore, the SPR-III is silicon-efficient and has better high-frequency characteristics because of the shorter channel length required. The relative bandwidth comparison as shown in Table 3.1 and Fig. 3.9 indicates that the normalised bandwidth for the PFR, SPR-III and SPQR-I is 1:14.9:3.1. This is roughly similar to the single-transistor case [9],[22] where the frequency characteristic is inversely proportional to the square of channel length.

This study illustrates that in practice, residual nonlinearities are largly due

to bulk modulation. The contributions due to mismatches and mobility degradation effect are not critical in this group of resistors. These resistors may be of use in applications where large resistances are desired and linearity is of secondary importance. For fixed resistor implementations, the SPR-III is relatively efficient, particularly in terms of area, power consumption and bandwidth. The total harmonic distortion can be lowered using high gate-overdrive bias ($V_C - V_T$) to minimise the bias-dependent cubic term as described in Eqn (2.11). For tunable resistor applications, the PFR and SPQR-I are the appropriate choices because of the absence of a gate-overdrive bias-dependent cubic nonlinearity. Although the PFR may be acceptable because it is simpler than the SPQR-I and its distortion performance is on par with that of the SPQR-I, its bandwidth is inferior. Therefore, the choice between the PFR and SPQR-I depends on the frequency requirement. The linearity of the PFR and SPQR-I can be improved via the increase of back-gate bias as can be seen in both Eqns (2.8) and (2.15).

3.1.2 Dual Gate-Bulk and Scaled-Gate Compensation Resistors

The results of simulations carried out on both the dual gate-bulk and scaled-gate compensation resistors are now described. These two resistor techniques are aimed at suppressing the bulk modulation, which as noted, is the major source of distortion in the unscaled-gate compensation resistors described earlier. The simulations are performed using identical resistance, common MOS models (Appendix B) and $\pm 5V$ supplies. The channel lengths adopted for the PFR, SPR, SPQR and GVCR were $100\mu m$, $25\mu m$, $50\mu m$, and $50\mu m$, respectively. In all cases the channel width was set to $10\mu m$. The transistors of the LSB (shown in Fig. 2.8)

were assumed to be identical and matched to the corresponding transistor pair in each dual gate-bulk compensation resistor. In the case of the GVCR scaled generator of Fig. 2.12, the transistor dimensions were $5\mu m/60\mu m$, $13\mu m/60\mu m$, $70\mu m/10\mu m$ and $80\mu m/10\mu m$ for M1-M2, M3-M4, M5-M6 and M7-M8 respectively. The bias voltage V_{BIAS} was -3.8V.

The family of static characteristics for the two groups of resistor are detailed in Fig. 3.10→3.16. By comparing the characteristics curves with those of unscaled-gate compensation resistors in Fig. 3.1→3.3, it can be seen that reduction of the gamma-related quadratic term reduces the asymmetry, between the first and third quadrant. The dual gate-bulk compensation resistors are controlled via voltages: V_C' and V_B' which are simultaneously established by the bias current I_B in Fig. 2.8. Similarly, tuning of the GVCR via V_C is depicted in Fig. 2.12.

The linearity for a set of $I - V$ curves can be assessed by examining the total harmonic distortion with variation of resistance for a given input signal level as shown in Fig. 3.17. Prior to discussion of the curves, it should be mentioned that the analytical expressions which are based on the simplified Level-2 equations are established in Appendix G-I and assume that the device is symmetrical. They do not, however, fully explain the trend of the THD curves. The principal reason lies in the fact that simulations are based on actual Level-3 models. The semi-empirical Level-3 models are most often employed because they can be more closely tailored to experimental results. Although Level-2 equations are directly related to device physics and can adequently predict the nonlinearity of the unscaled-gate compensation resistors where the bulk effect is dominant, they are not as accurate as Level 3 for predicting low distortion levels. Appendix J summarises the analytical expressions for the dual gate-bulk compensation resistors

using simplified Level-3 equations. Basically, the cubic terms are approximately the same as those of the Level-2-based expressions (Appendix G-I). The difference is that a small gamma-related quadratic term is generated which subtracts from the mobility-related quadratic term. These two terms it may be noted are bias-dependent. In a typical design where, for example, the gate-overdrive bias is 2V and process parameters are as shown in Appendix B, the mobility-related quadratic term would be larger than the gamma-related quadratic term. Thus, reducing the gate overdrive in the process of tuning a resistor would increase the gamma-related quadratic term and decrease the mobility-related quadratic term, resulting in a reduction in the nonlinearity. With reference to Fig. 3.17, it is interesting to observe that some cancellation of mobility and bulk terms occurs in all structures except the SPR, and results in a distortion minimum. The monotonic increase in the SPR distortion curves is principally due to the increase in the cubic nonlinearity with decreasing bias. By comparing the quadratic coefficients of the simplified Level-3 expressions (Appendix J), it can be seen the magnitude of the dominant quadratic coefficient for the SPQR structures is half of that in the PFR structure. The simulation results agree with the theory that the SPQR networks offer a THD improvement over the PFR network of up to $6dB$.

The GVCR structure should in principle be expected to exhibit a similar distortion level to the SPQR because the mobility degradation level is the same. This is not the case in practice, due to the imperfections in the scaled generator. Factors such as the mobility degradation effect in the differential pairs and imperfect current mirrors etc. would also cause an error on generating a linearising/control signal, resulting in incomplete cancellation of distortion. The similar THD levels confirm that the terminal characteristics of the SPR-I and SPR-III are virtually

identical. This is also the case for the group of SPQR structures.

Having discussed the variation of THD versus tuning of resistance, the signal-handling capability for a given resistance is considered. Fig. 3.18 and 3.19 collectively group the transfer characteristics and THD plots against input signal for nominal resistance $120K\Omega$. With reference to Fig. 3.19, it can be seen that the THD curves for most of the resistor structures exhibit a 'ripple-like' shape rather than a monotonic increasing function. This will be explained by examining the PFR as an example.

Consider the PFR schematic diagram of Fig. 2.9 and assume that the transistor pair is grounded at the 'source' end thus setting the potential $v_s = 0$. For a positive-going signal v_d, the gate-to-source voltage of M1 must be greater than the drain-to-source v_{ds} voltage, thus it is operated in the non-saturation region. The transistor M2, on the other hand, can only be maintained in the non-saturation region when v_{ds} is less than $(V_C' - V_T)$. For a value of $120K\Omega$, simulation data reveals that the dc gate control voltage is $V_C' = 2.22V$ and the threshold voltage of the transistor pair is $V_T = 1.52V$. This suggests that transistor M2 would approach saturation when $v_{ds} = 0.7V$ in peak value. Therefore, the dip of the PFR distortion curve at the first transition $(1.5V_{pp})$ is largely due to the cancellation of the mobility degradation terms and the effective quadratic-related products. The second transition where the THD curve rises rapidly can be attributed to the fact that the current source transistor of the LSB shown in Fig. 2.8 is pushed into the non-saturation region under large signal conditions. Since the mid-point voltage of the SPQR-II and SPQR-III (Fig. 2.11(b) and (c)) is only half of v_{ds}, it thereby doubles the signal level $(3V_{pp})$ for the first transition. Although the SPQR-III in principle should be identical to the SPQR-II, the topological difference in

the buffer arrangement causes it to perform differently under large-signal drive conditions. The SPQR-I distortion curve of Fig. 2.11(a) exhibits similar behaviour but the signal level ($2V_{pp}$) for the first transition is less than for the SPQR-II because the mid-point voltages are not purely common-mode signals. In order to illustrate the overall picture, the SPR-I of Fig. 2.10(a) is examined. Assuming the source terminal of M2 is grounded, the drain-to-source voltage across M1 according to the Eqn (2.35) is $v_{ds}/2-(1+\delta_{Bs})v_{ds}^2/8\sqrt{\frac{I_{Bs}}{K_s}}$ and for M2 is $v_{ds}/2+(1+\delta_{Bs})v_{ds}^2/8\sqrt{\frac{I_{Bs}}{K_s}}$. This is not the case for either the SPQR-II or SPQR-III where the drain-to-source voltage across each device in the upper and lower resistive branch is only $v_{ds}/2$. Since one branch of the SPQR-I is identical to the SPR-I, the operating range of the SPQR-I is lower than that of the SPQR-II and SPQR-III. Compared with the unscaled-gate compensation PFR and SPQR-I in Fig. 3.4, the dominant bulk distortion masks the minor details, resulting in monotonic behaviour. In the SPR case (Fig. 2.10), when either one of the transistors in the resistive branch approaches saturation, the current flowing becomes constant which creates an abrupt change in the distortion level at large signal. Referring to Fig. 3.19, the GVCR structure (Fig. 2.13) offers very good performance in terms of the signal level ($3.5V_{pp}$) for the occurrence of the first transition. This is due to the fact that the gate of the transistor M1 is coupled with a dc control signal plus approximately half of terminal signal (see Eqns (2.46) and (2.48)). Thus very high v_{ds} is required before the transistor moves into saturation.

The operating ranges of individual resistors, assuming that the transistors operate in their valid region, are compared in Table 3.3. These results show that the structures [16]→[19] which distribute v_{ds} across each transistor in the resistive branch increase the operating range compared with that of the parallel

form structures [8]→[15]. This same is true of the single-device-based structures [3]→[5],[7]→[8] with terminal feedback to the gate.

Perfect matching of MOS transistors can never be achieved and mismatches between transistors generally introduce additional distortion. Geometrical mismatch must therefore be regarded as an important factor for design of linear resistors. In practice, the sensitivity of a resistor to mismatches is a function of layout, transistor size, circuit topology and complexity etc. . Table 3.3 together with Fig. 3.20 assesses the worst-case THD curves at ±2% mismatch. The SPQR-III is the most sensitive circuit as two branch currents are simultaneously controlled by the shared buffer. Any mismatch in the shared buffer affects both branch currents, resulting in imperfect cancellation of distortion components. The SPQR-II and SPQR-III architectures are less sensitive in comparison with the SPQR-III. The GVCR structure suffers from the second largest sensitivity figure due to the errors in generating a precise linearising/control signal. The lowest sensitivity to mismatch is obtained for the SPR-III on the basis of its simplicity but the SPR-I is not as insensitive. The PFR, on the other hand, displays a fairly low mismatch sensitivity. However, notwithstanding mismatch considerations, the distortion performance of the SPQR-I and SPQR-II are still better than the PFR, SPR and GVCR by at least $3.6dB$, $13dB$ and $9.71dB$, respectively at $120K\Omega$ for $0.5V_{pp}$.

Table 3.3 also compares the silicon area ratio for each resistor type. The ratios ignore the area associated with bias transistors and any increase due to the routing area. In the design of a dual gate-bulk compensation resistor, the LSB transistors are usually designed to be identical to the respective transistor pair in order to obtain good matching. On this basis, the PFR and SPQR occupy relatively large silicon areas and the SPR the smallest.

As the PFR requires the longest channel length, it needs smaller LSB bias currents to establish equal quiescent bias voltages and achieves low power performance as shown in Table 3.3. In the case of the SPR, the price paid for the shorter channel length and good frequency response is an increase in power consumption. Since the channel length of the SPQR is half of that in the PFR, the power dissipation is therefore higher than in the PFR. The GVCR, on the other hand, demands fairly low power. It is important to note that the power consumption is based on the sharing of a global bias circuit for the corresponding resistor network.

The bandwidth performance is closely related to the channel length and architecture. The simulated frequency responses of the resistors are depicted in Fig. 3.21. With reference to the results in Table 3.3, it can be seen that the bandwidth of the PFR is the lowest whilst that of the SPR is the highest. Although the SPR-III exhibits lower sensitivity and silicon utilization than the SPR-I, the bandwidth is inferior. The SPQR and GVCR structures offer medium bandwidth performance.

To conclude this section, it may be noted that when bulk effects are minimised, mobility degradation and geometrical mismatches are the major factors determining distortion. Unlike the unscaled-gate compensation resistors, these resistors offer reasonably low distortion whilst operating from $\pm 5V$ supplies In addition, the linearity, signal-handling capability, silicon efficiency, power consumption and bandwidth of each resistor is shown to depend on the circuit configuration. Thus, the choice of a resistor to meet a specific application requirement would need to be made with reference to all the relevant advantages and disadvantages.

3.1.3 MOS Filter Examples

The performance of filters based on the proposed resistor structures, GVCR and SPQR-I is now investigated. This includes the signal-handling capability, distortion level and tunability of the filters.

3.1.3.1 Second-Order GVCR-Based Filter

The application of the basic GVCR as the resistive elements in the familiar two-integrator-loop second-order filter has been demonstrated in Section 2.6.1. SPICE simulations of the basic filter have been made based on the transistor dimensions shown in Fig. 2.18. The filter was designed to have a Chebyshev lowpass response with $0.5dB$ passband ripple. The transistor dimensions and bias voltage for the scaled generators were maintained at the values discussed in Section 3.1.2. The models were the Plessey $2\mu m$ process and supply voltages were $\pm 5V$. Auxiliary devices, including capacitors and operational amplifiers, have been assumed to be ideal.

Fig. 3.22 illustrates that the 3dB cut-off frequency can be varied from $3.2KHz$ to $7KHz$ ie, a tuning ratio of 2.2. The amplitude/frequency response simulations show good agreement with the specification at the nominal cut-off frequency $4.7KHz$ given in Fig. 3.23. It can be seen that stopband attenuation is up to $100dB$. Although this figure appears good, in practice, distortion and noise will limit the stopband attenuation.

The distortion performance of the filter has been assessed using an input signal frequency at one-third of the cut-off frequency. With the filter tuned at cut-off frequencies of $3.2KHz$, $4.7KHz$ and $7KHz$, the corresponding THD curves are shown in Fig. 3.24. The lowest frequency curve reveals that when the control

voltage V_C in Fig. 2.12 is low, the grounded transistor (shown in Fig. 2.13) enters into saturation before the large-signal drive violates the saturation requirement of the current mirror transistor M8. This causes the 'ripple-like' phenomenon as described in Section 3.1.2 (see Fig. 3.19). Conversely, when the control voltage V_C is tuned to achieve higher cut-off frequencies, then under large-signal conditions, the mirror transistor no longer operates in the saturation-mode condition; resulting in a rapid rise in distortion. With reference to Fig. 3.24, the filter can support input signals up to $4V_{pp}$. These curves measured over a tuning ratio of 2.2 suggest that even under a ±38% variation in process parameters, a signal swing of at least $3V_{pp}$ can be maintained for a 1% distortion. A wider tuning range can be achieved but only at the expense of reducing the signal-handling capability of the filter.

It should be appreciated that these reasonably low distortion figures are obtained without employing differential circuit topology. The filter uses regular single-ended operational amplifiers and the design process is straightforward. It can provide an economic alternative to the balanced arrangements previously advocated [20]→[25] for use in fully integrated continuous-time MOSFET-C filters.

3.1.3.2 SPQR-Based Sallen-Key Lowpass Filter

Realisation of a 4th order Sallen-Key lowpass filter based on the the SPQR-I structure was described in Section 2.6.2. Simulation results for the proposed filter structure in Fig. 2.24 are now presented. As in the previous simulation example, the models and supplies were assumed to be identical. The aspect ratios for each of the LSBs and resistive transistor were $5\mu m/50\mu m$, whilst those for the M1-M4, M5-M6 combination in the driving buffer (Fig. 2.23) were $135\mu m/3\mu m$ and $675\mu m/3\mu m$, respectively. The bias current I_B was set to $I/5$ and equal to $17\mu A$

in the driving buffer.

Unlike the conventional operational-amplifier-based buffer in which the output impedance is reduced by negative feedback, the finite output impedance of the buffer as shown in Fig. 2.23 would impose a limit on the stopband attenuation. In order to minimise this drawback, extra capacitors of $5pF$ were added to the output nodes of the individual driving buffer. Fig. 3.25 compares the simulated filter response with the ideal case at nominal $37KHz$ $3dB$ cut-off frequency. It is important to note that the filter response remains unchanged following this modification. Control tuning of the frequency response to cut-off frequencies of $25KHz$ and $50KHz$ is also illustrated in Fig. 3.26 and demonstrates the tunability of the resistor. It can be seen that a worst-case minimum stopband attenuation of $75dB$ should be achievable over a tuning ratio of 2:1. The individual THD at one-third of cut-off frequency is plotted in Fig. 3.27, indicating that the maximum stays below 1% distortion for input signal swing up to $5V_{pp}$. This result is even better than the figure obtained in the GVCR case because, at an input frequency of one-third of the cut-off frequency, the nodal potentials v_a and v_b as indicated in Fig. 2.20 are not actually at ground. The distortion is reduced due to the relatively smaller v_{ds} drop across each resistive transistor network and enhances the input signal capability. However, at higher cut-off frequencies where a high gate bias is required, higher input signal will push the current-source transistor in the LSB out of saturation and produces a sharp increase in distortion.

The application of the proposed SPQR-I to the design of a fourth-order Butterworth lowpass filter shows that good results can be obtained using identical floating resistors together with capacitors and simple buffers. The results compare favourably with those reported in [20] and [30]. As noted, the use of a buffer

in place of operational amplifiers does, however, require additional capacitors in order to compensate for the higher output impedance and ensure adequate stop-band attenuation.

3.2 Experimental Results

3.2.1 Layout Techniques

Based on the simulation studies presented earlier, a group of unscaled-gate compensation resistors have been fabricated using the Plessey twin-well CMOS technology with one μm minimum geometry (Appendix C). A microphotograh of the CMOS resistors is given in Fig. 3.28. In all cases, the resistive transistor pairs are p-channel. The channel length and width of the PFR, SPR-III and SPQR-I were those in Section 3.1.1. In addition, the n-channel-based source followers are arranged physically close to the corresponding resistor network. The aspect ratio for transistors in the source followers are $40\mu m/10\mu m$. The biases for the buffers were globally adjusted via a common control pin. The layout of the voltage-controlled resistors was implemented using Mentor Graphics CHIPGRAPH (a graphical layout editor) using Plessey Q rules. The estimated silicon area (including routing area) for the PFR, SPR-III and SPQR-I are $6.1\times10^4\mu m^2$, $2.8\times10^4\mu m^2$ and $7.2\times10^4\mu m^2$, respectively.

In laying out the unscaled-gate compensation resistors, several considerations were taken into account. Firstly, all the transistor pairs of individual resistors were placed close together and arranged with the same orientation so as to obtain a high degree of matching. Secondly, large transistor dimensions were employed in order to minimise second-order effects such as channel-length modulation and

geometrical mismatches.

All the inputs/outputs of the complete chip were protected electrically by Plessey ESD (Electrostatic Discharge) cells. The cell was modified by stripping off the input resistance, leaving only a diode to bypass static electric charges. The influence of the normal-input protect resistor on the $I - V$ characteristic measurement is therefore eliminated. However, a large capacitance is associated with the bonding-pad diode. All the measurements are therefore restricted to low frequencies.

3.2.2 Unscaled-Gate Compensation Resistors and Filter Example

Measurements were conducted for the representative circuits; PFR, SPR-III and SPQR-I. Since the maximum allowable supply voltage for the chip was $7V$, an unbalanced supply of $+2V/-5V$ was used. The experimental set-up for the measurement of total harmonic distortion is shown in Fig. 3.29. The total harmonic distortion was measured with a Hewlett-Packard distortion analyser HP339A. The DUT (Device Under Test) refers to the active resistor to be tested. This active resistor combined with a feedback passive resistor R ($120K\Omega$) and an operational amplifier ($TL072$) constitute an inverting amplifier. The amplifier distortion, as measured by replacing the DUT with a passive resistor, was below $80dB$. This ensured that the measured THD is mainly that contributed by the MOS resistor.

Fig. 3.30 presents the plots of THD against variation of resistance value for each resistor with the signal amplitude set to $0.5V_{pp}$. It should be noted that the resistance is a function of gate bias established via the control bias of the source follower. The higher the gate bias, the lower is the resistance. The result shows the

improvement in THD achieved with low resistance value (implying a large control bias is applied for the circuits). With reference to the technological parameters in Appendix C, the mobility factor is 0.1. As low supply voltage and large transistor dimensions were employed in the design, the distortion due to the mobility degradation effect and geometrical mismatches could be expected to be small. It is also evident from Fig. 3.30 that the PFR and SPQR-I have similar distortion levels because the bulk modulation effects are virtually identical. The SPR-III, on the other hand, is more sensitive to the bias owing to the additional bias-dependent nonlinearity. These experimental results show excellent correlation with the theoretical predictions and the simulation results of Fig. 3.4.

The results for static $I - V$ measurements performed on these circuits at a nominal $37K\Omega$ resistance is depicted in Fig. 3.31. It may be seen that the bulk effect produces asymmetrical $I - V$ characteristics which is particularly pronounced at larger signal drives. As expected, good linearity requires that the input signal swing be restricted. Fig. 3.32 further compares the corresponding THD curve against input signal at the same nominal resistance value. The distortion components in all cases are below the $-39dB$ level for input amplitudes lower than $0.5V_{pp}$. The bias-dependent cubic nonlinearity increases rapidly with signal level. This experimental evidence confirms the predicted linearization.

The tunability of the SPQR-I is examined in Fig. 3.33. These voltage transfer characteristics were obtained by measuring both the input and output voltage of the test circuit in Fig 3.29. With the feedback resistance R chosen to be $120K\Omega$, the settings for the oscilloscope were 0.2V/div in X mode and 2V/div in Y mode. Three curves for resistances of $25K\Omega$, $37K\Omega$ and $55.6K\Omega$ were obtained by tuning the respective control voltages.

A second-order filter based on the SPQR-I structure and with the circuit schematic shown in Fig. 2.15 was constructed using external capacitors and operational amplifiers. The filter components were designed to give a Butterworth filter response by setting the quality factor Q to be 0.707. The operational amplifiers were $TL072$ and the measured capacitors were $C_1 = C_2 = 830pF$. For a nominal resistance of $37K\Omega$ and Q control resistance tuned to $26.16K\Omega$, the calculated and measured nominal $3dB$ frequency were $5.18KHz$. Fig. 3.34 illustrates the signal-handling capability of the filter with the input signal frequencies set at one-third of the cut-off frequencies. As indicated by the curves, the THD increases with the input signal amplitude and decreases with increasing cut-off frequency. The linearity of the filter closely follows that of the resistors up to a frequency limit of the amplifier. For a tuning ratio of 2.2, the worst-case maximum input swing for distortion below $-36dB$ is $0.5V_{pp}$. Although this figure could be expected to be higher for the dual gate-bulk counterpart, the effective linearity can be extended by means of input attenuation and post amplification at the cost of reducing the dynamic range of the filter [20],[22]. As the resistor is simple and the design process is straightforward, the additional circuitry does not cause too much silicon overhead or design burden. Based on these results, the SPQR, PFR and SPR should find useful application for analogue signal-processing tasks in the MHz range.

$R = 185.2K\Omega$	PFR	SPR-III	SPQR-I
THD(dB) at $0.5V_{pp}$, no mismatch	-35.09	-33.76	-35.19
THD(dB) at $0.5V_{pp}$, 2% mismatch	-34.07	-32.74	-34.33
Power Consumption (mW)	0.2	0.1	0.3
Bandwidth (MHz)	1.35	20.14	4.21

Table 3.1: Performance comparison of unscaled-gate compensation resistors with $\theta = 0.15V^{-1}$ at nominal resistance ($185.2K\Omega$)

$R = 185.2K\Omega$	PFR	SPR-III	SPQR-I
THD(dB) at $0.5V_{pp}$, no mismatch	-34.47	-37.46	-39.49
THD(dB) at $0.5V_{pp}$, 2% mismatch	-34.26	-37.02	-39.16

Table 3.2: THD comparison of unscaled-gate compensation resistors with $\theta = 0.4V^{-1}$ at nominal resistance ($185.2K\Omega$)

$R = 120K\Omega$	PFR	SPR-I	SPR-III	SPQR-I	SPQR-II	SPQR-III	GVCR
THD(dB) at $0.5V_{pp}$, no mismatch	-56.25	-45.97	-45.93	-62.97	-62.85	-62.85	-55.14
THD(dB) at $0.5V_{pp}$, 2% mismatch	-53.81	-41.43	-44.38	-57.79	-57.43	-50.93	-47.72
Increase of THD(dB) at 2% mismatch	2.44	4.54	1.55	5.18	5.42	11.92	7.42
Operating Range (V)	±0.75	±1	±1	±1	±1.5	±1.25	±1.75
Relative Silicon Ratio	20	5	3	16	20	16	-
Power Consumption (mW)	0.082	0.333	0.22	0.22	0.276	0.22	0.175
Bandwidth (MHz)	3.2	38	28.1	8.6	11.2	8.6	5.4

Table 3.3: Performance comparison of dual gate-bulk and scaled-gate compensation resistors with $\theta = 0.15V^{-1}$ and $\pm5V$ supply voltage at norminal resistance ($120K\Omega$)

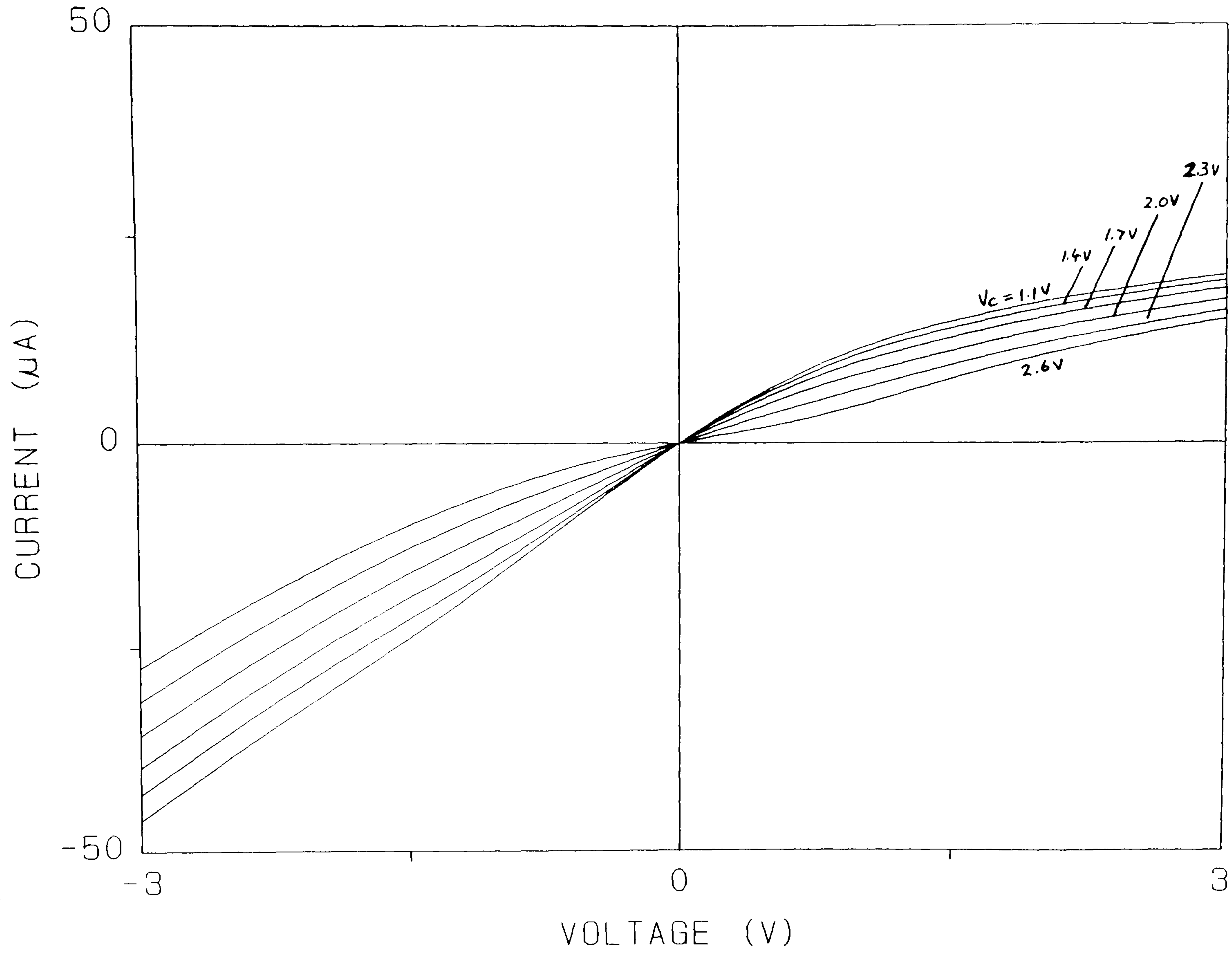


Figure 3.1: Control voltage tuning of static characteristics for unscaled-gate compensation PFR

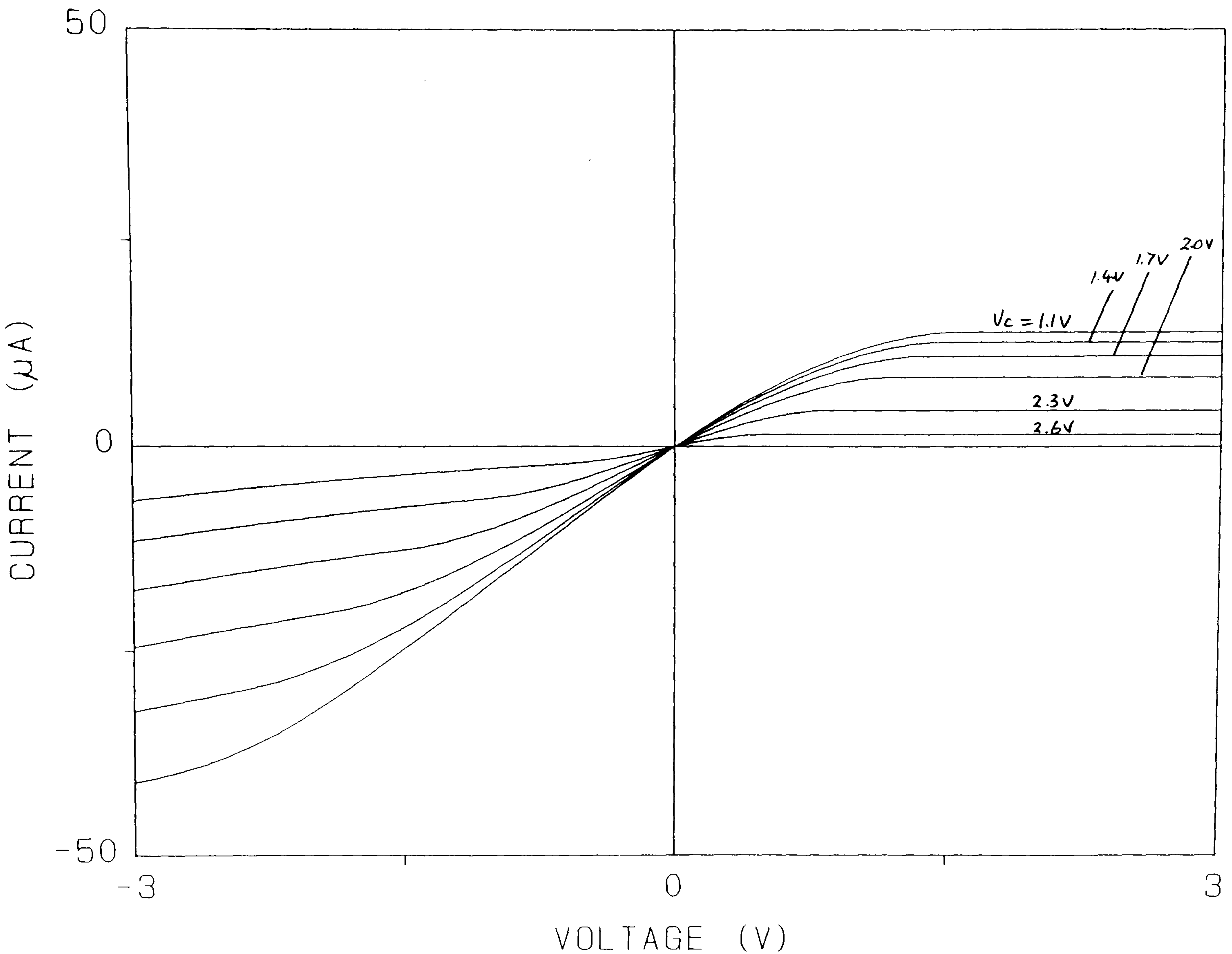


Figure 3.2: Control voltage tuning of static characteristics for unscaled-gate compensation SPR-III

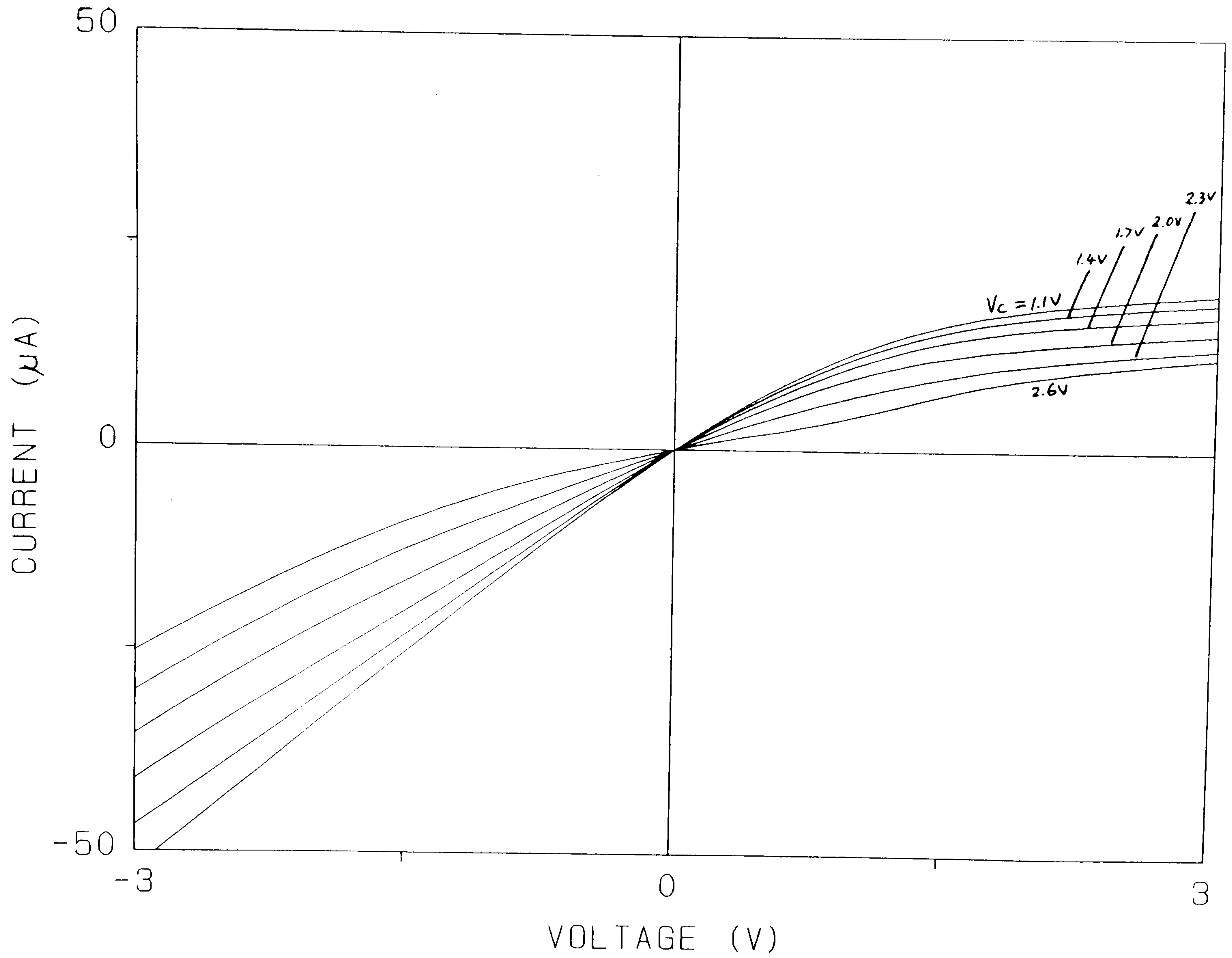


Figure 3.3: Control voltage tuning of static characteristics for unscaled-gate compensation SPQR-I

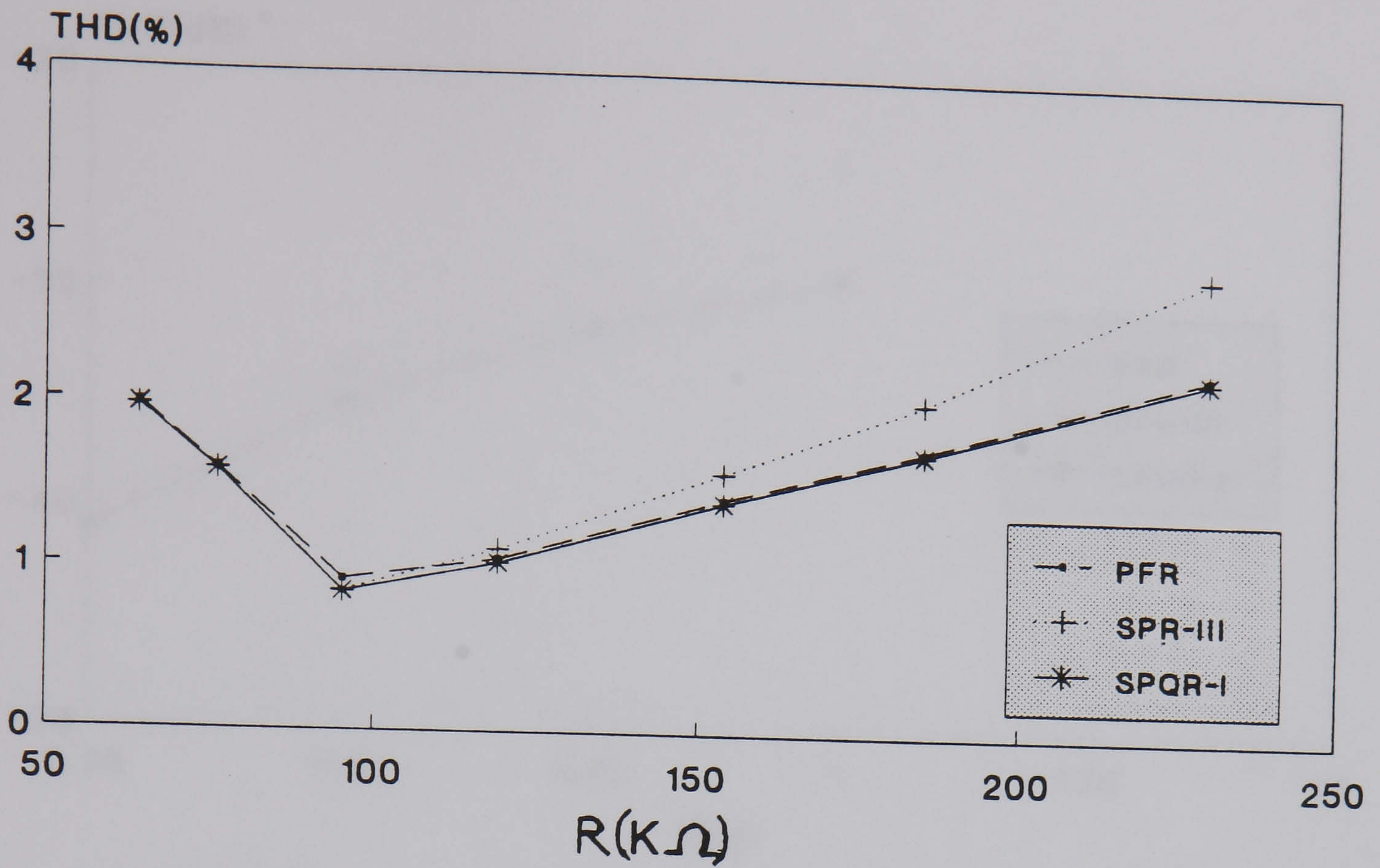


Figure 3.4: THD of unscaled-gate compensation PFR, SPR-III and SPQR-I with different resistance values at $0.5V_{pp}$, $\theta = 0.15V^{-1}$

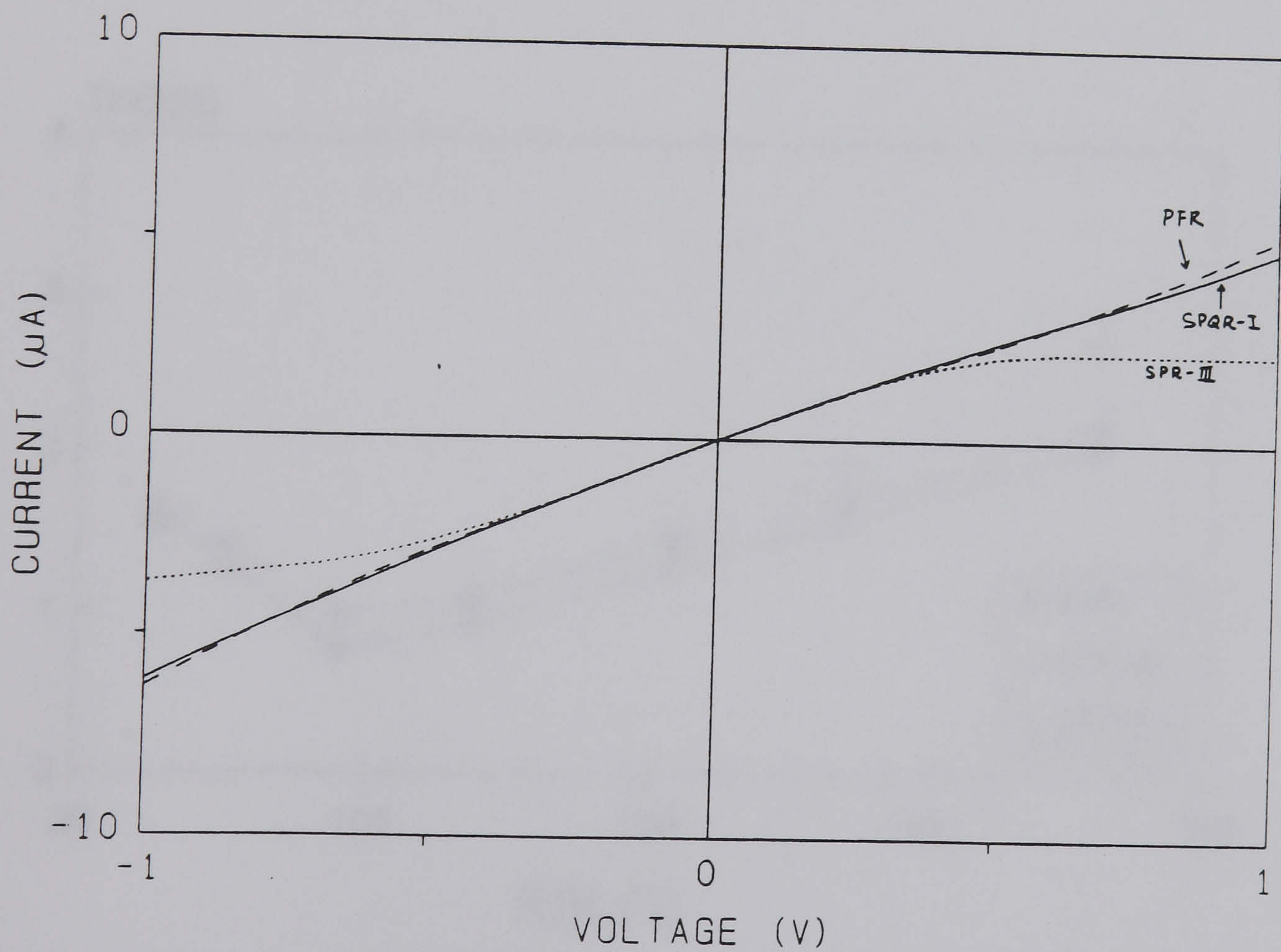


Figure 3.5: Static characteristic of PFR, SPR-III and SPQR-I for nominal resistance $(185.2K\Omega)$

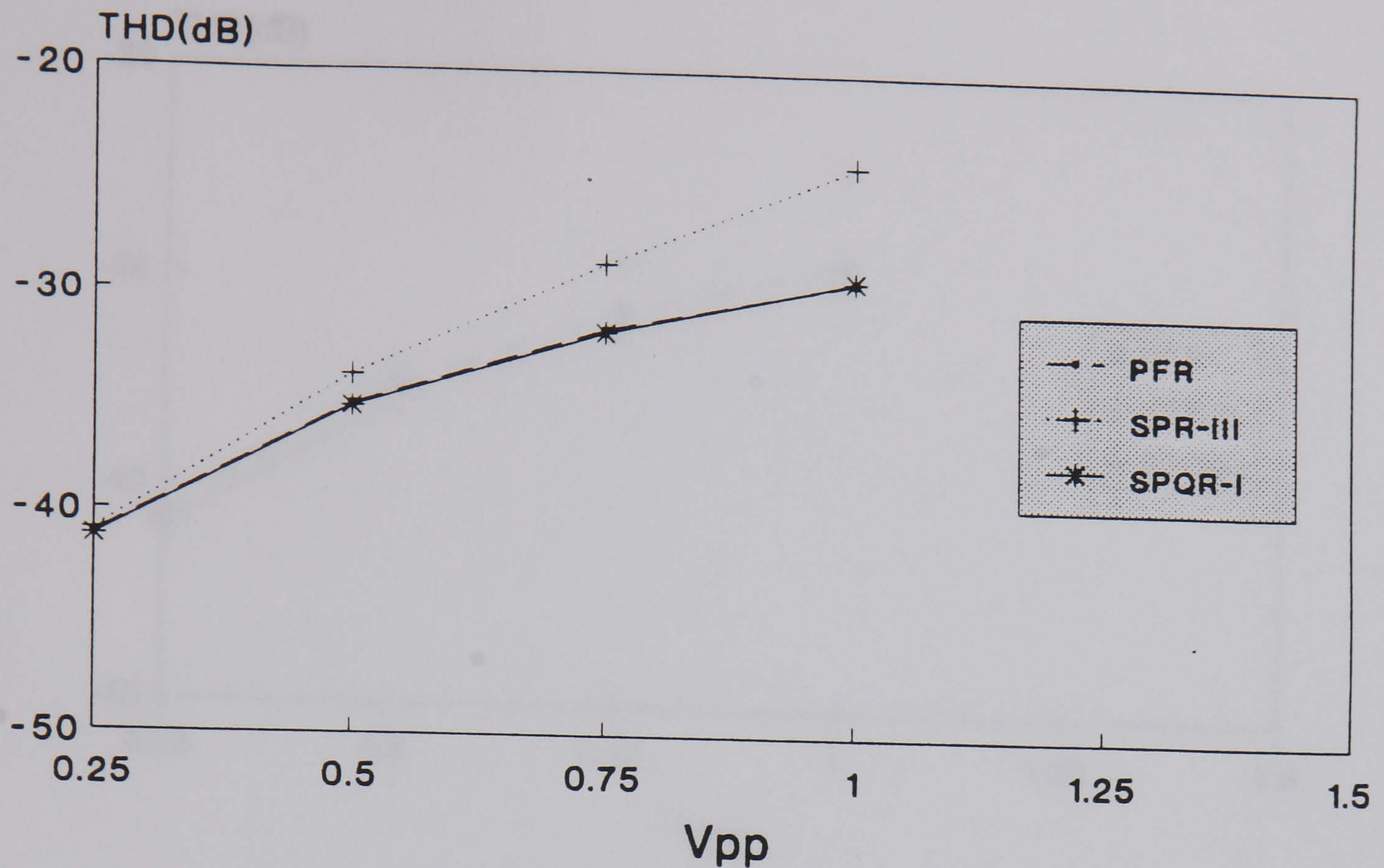


Figure 3.6: THD of unscaled-gate compensation PFR, SPR-III and SPQR-I against signal level at nominal resistance ($185.2K\Omega$) for $\theta = 0.15V^{-1}$

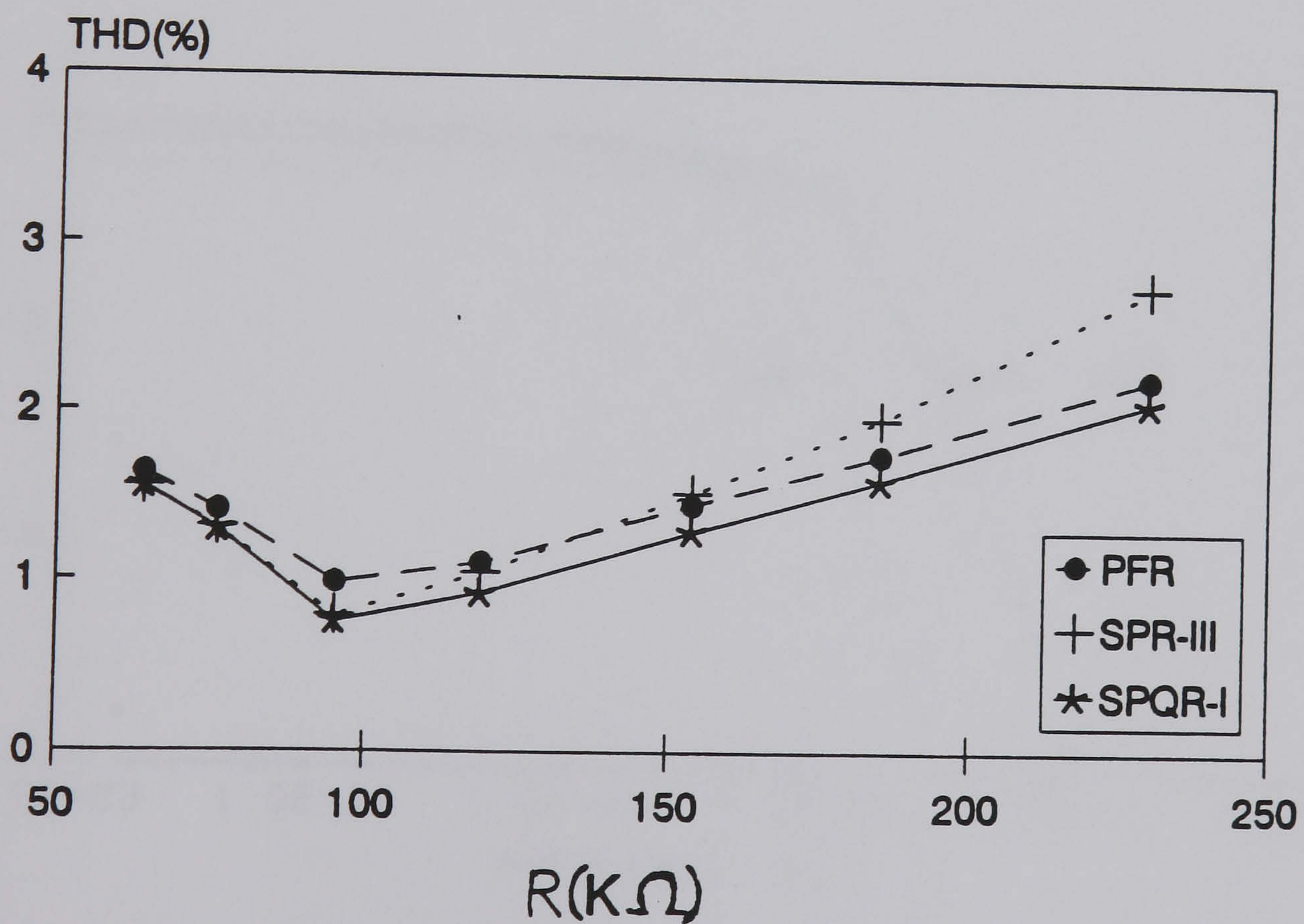


Figure 3.7: THD of unscaled-gate compensation PFR, SPR-III and SPQR-I with different resistance values at $0.5V_{pp}$, $\theta = 0.4V^{-1}$

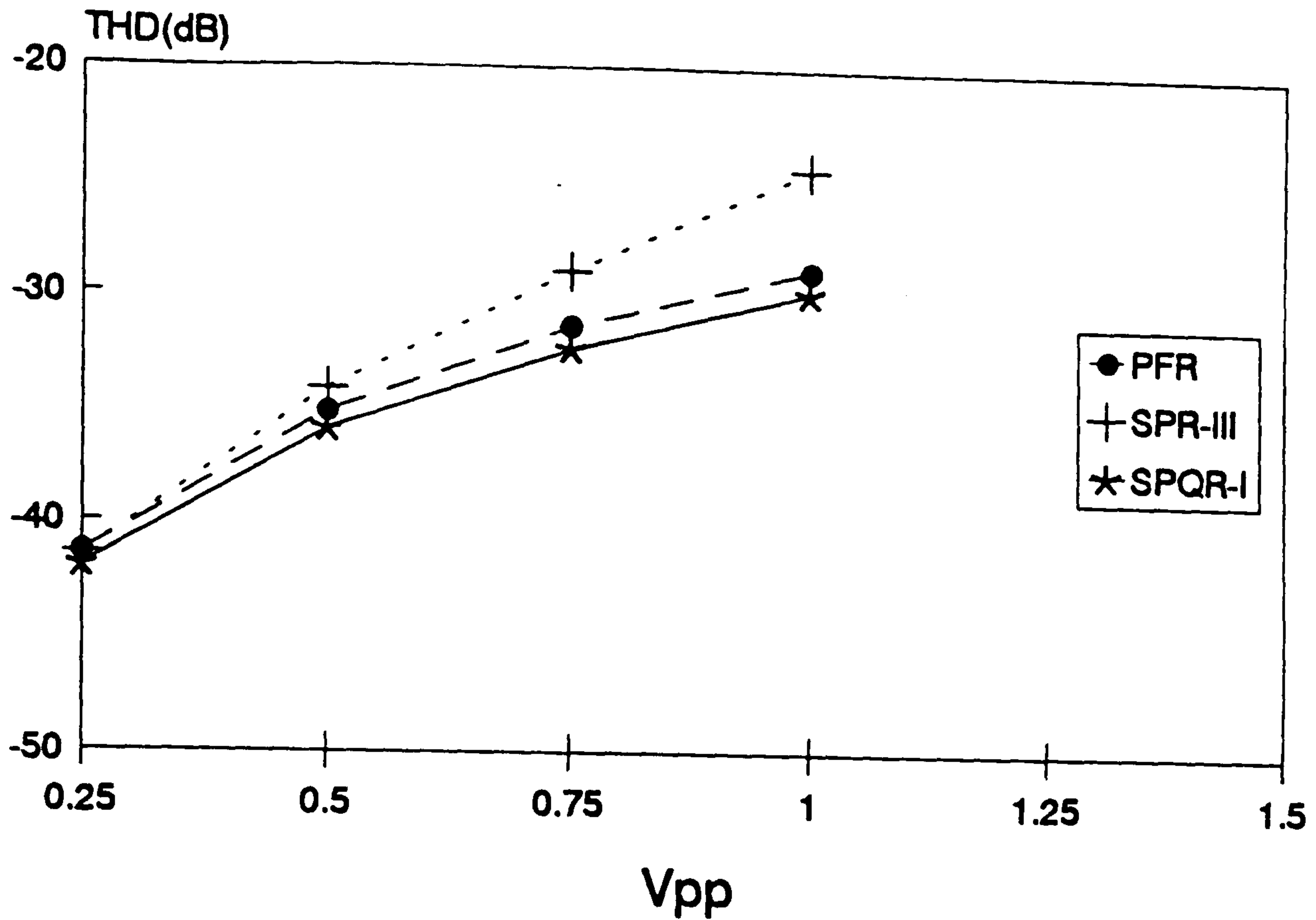


Figure 3.8: THD of unscaled-gate compensation PFR, SPR-III and SPQR-I against signal level at nominal resistance ($185.2K\Omega$) for $\theta = 0.4V^{-1}$

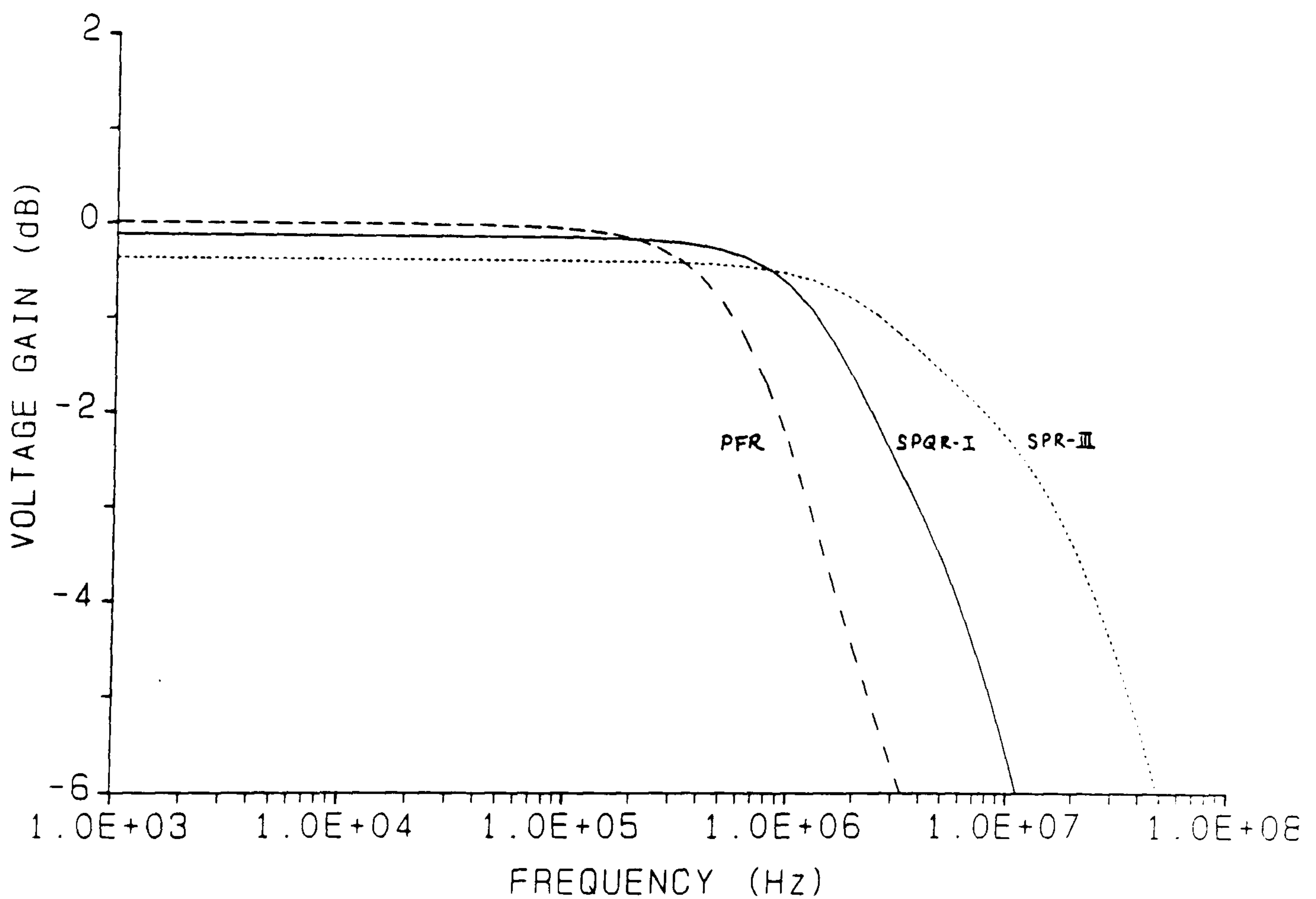


Figure 3.9: Bandwidth of unscaled-gate compensation resistors at nominal resistance ($185.2K\Omega$)

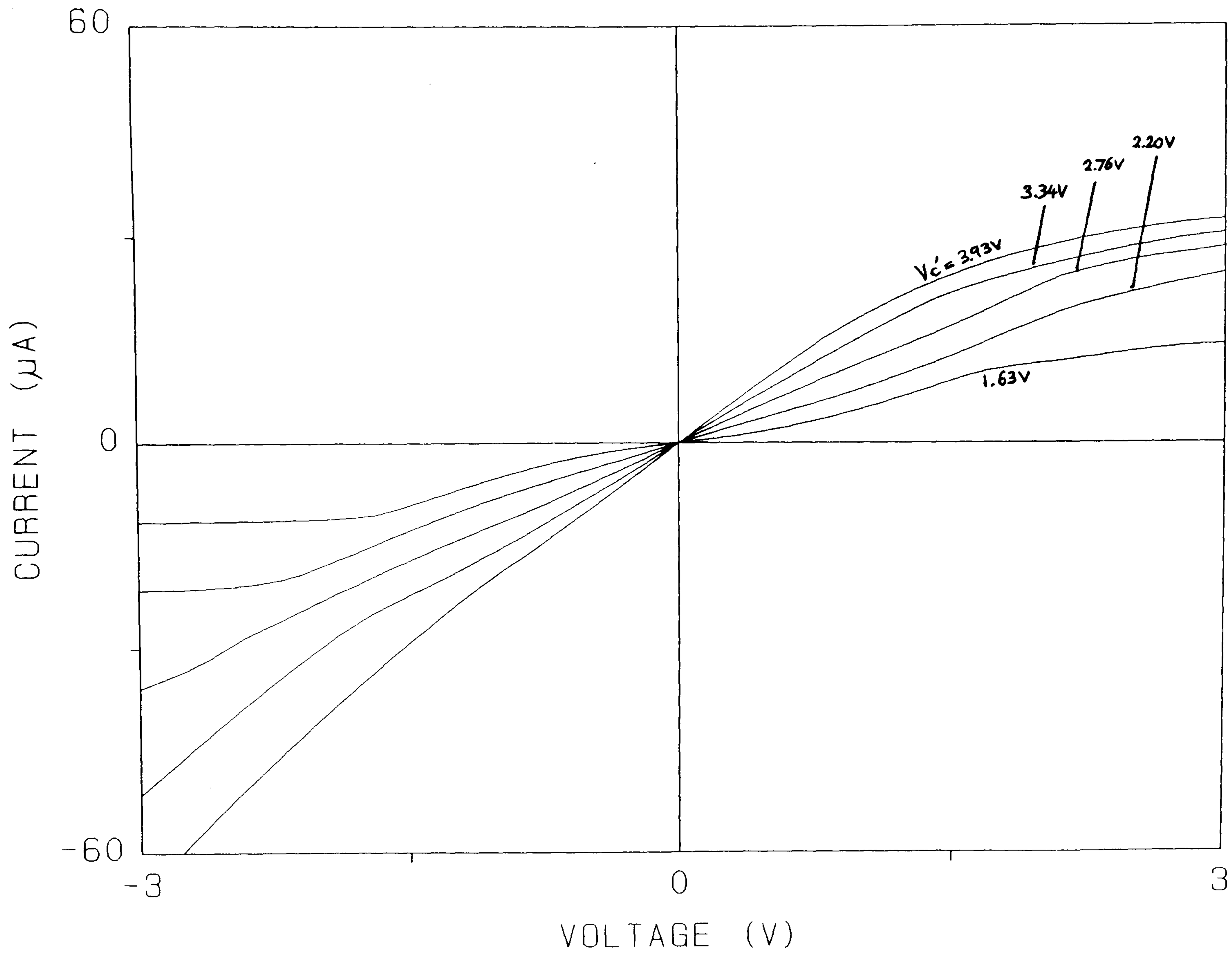


Figure 3.10: Control voltage tuning of static characteristics for dual gate-bulk compensation PFR

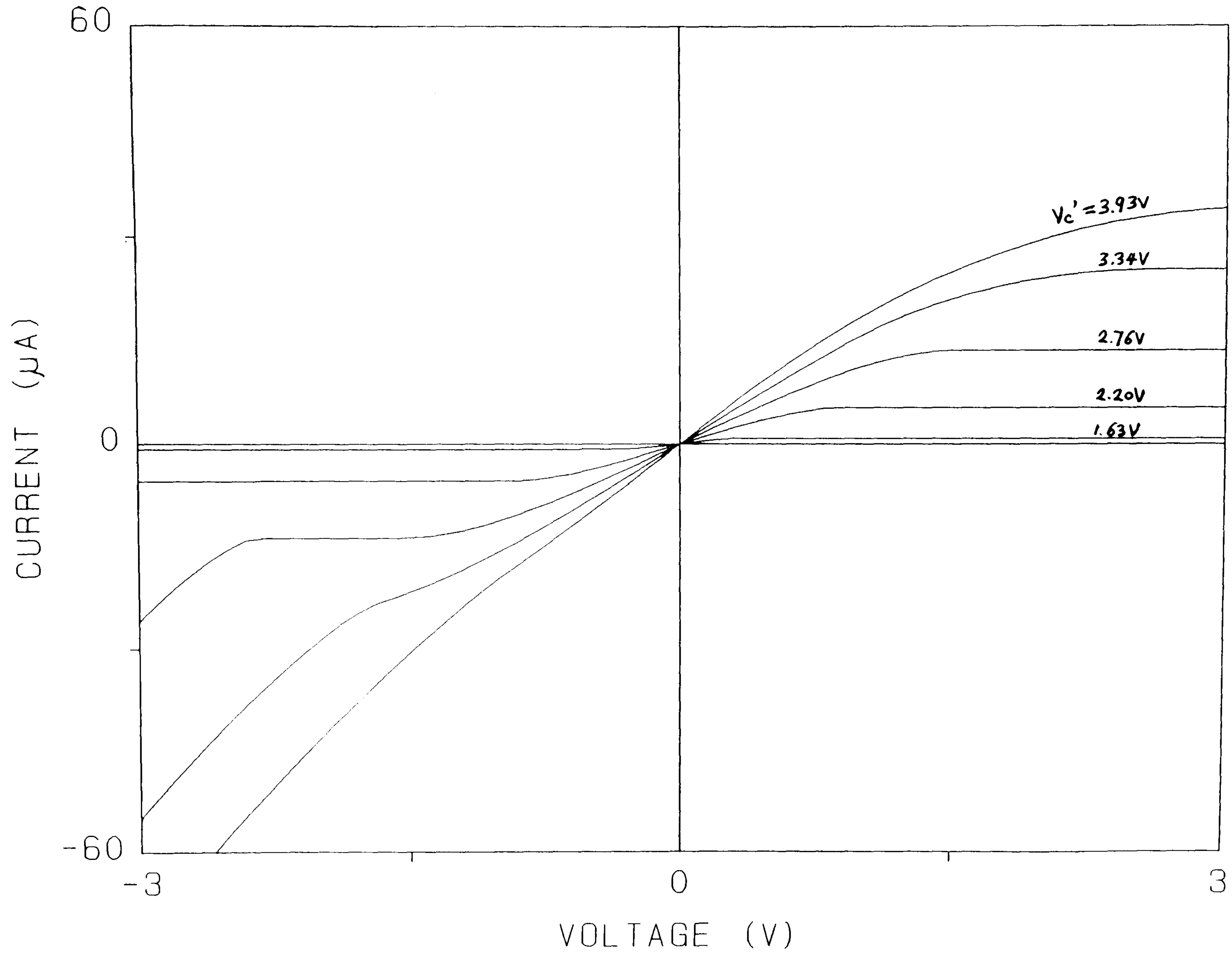


Figure 3.11: Control voltage tuning of static characteristics for dual gate-bulk compensation SPR-I

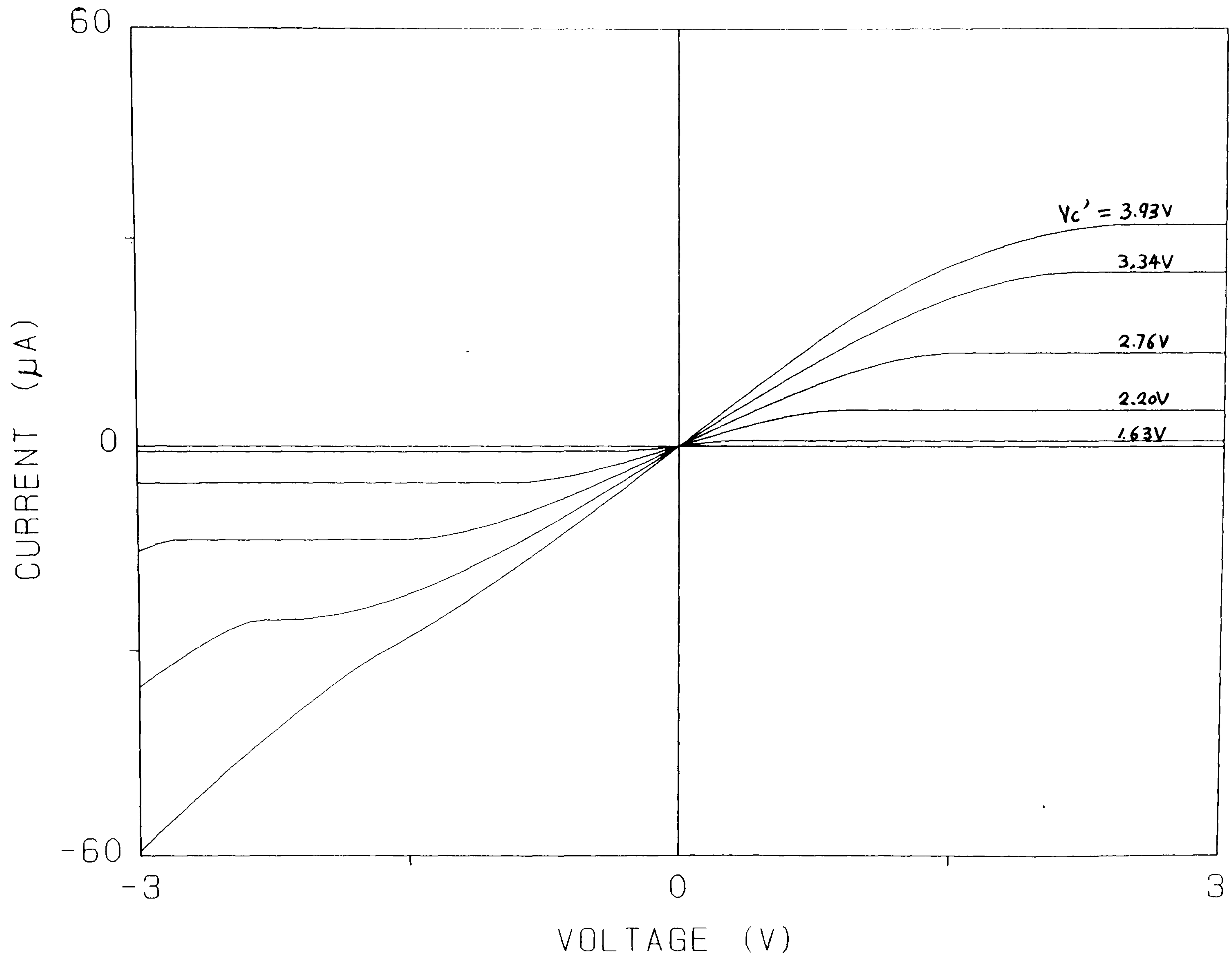


Figure 3.12: Control voltage tuning of static characteristics for dual gate-bulk compensation SPR-III

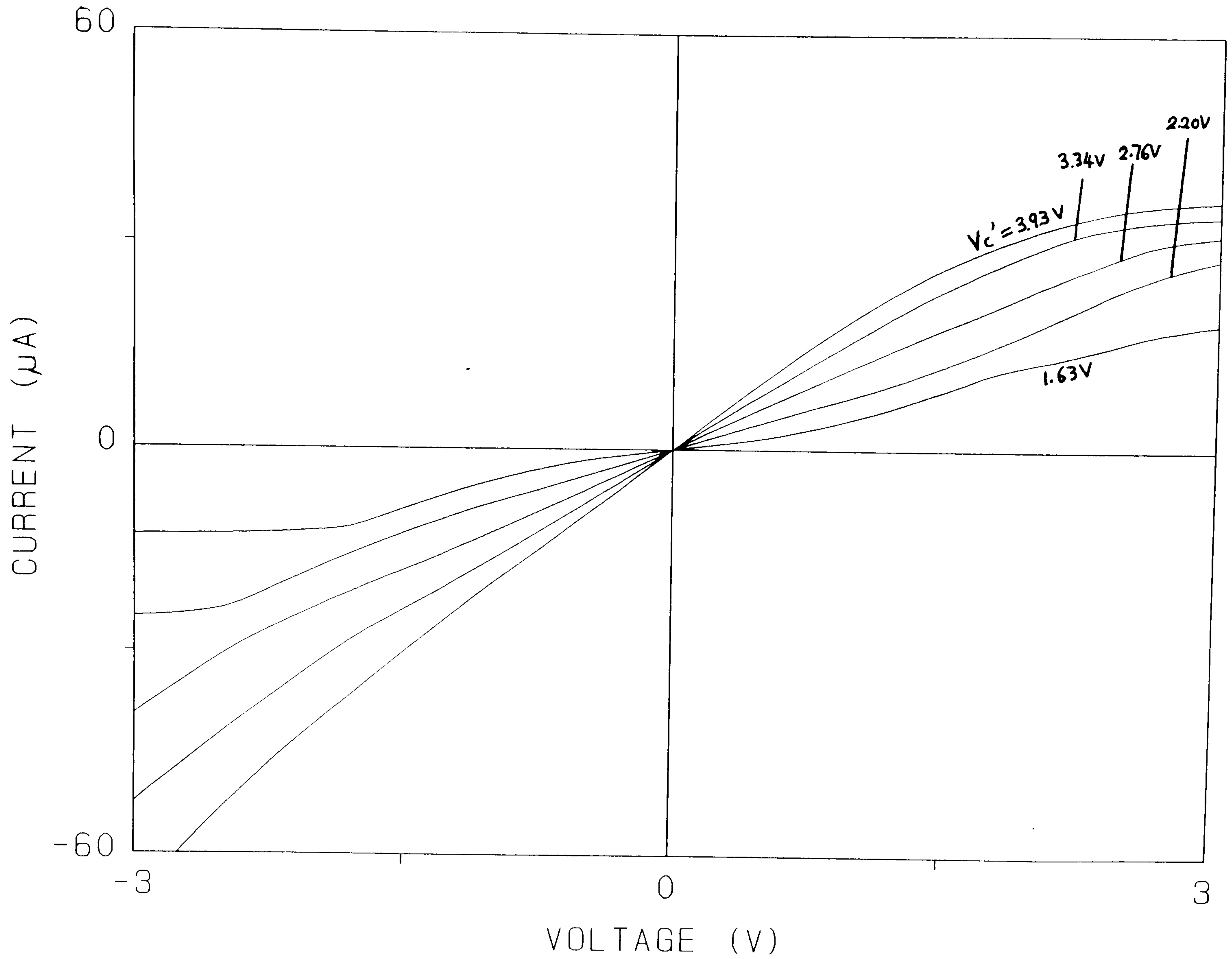


Figure 3.13: Control voltage tuning of static characteristics for dual gate-bulk compensation SPQR-I

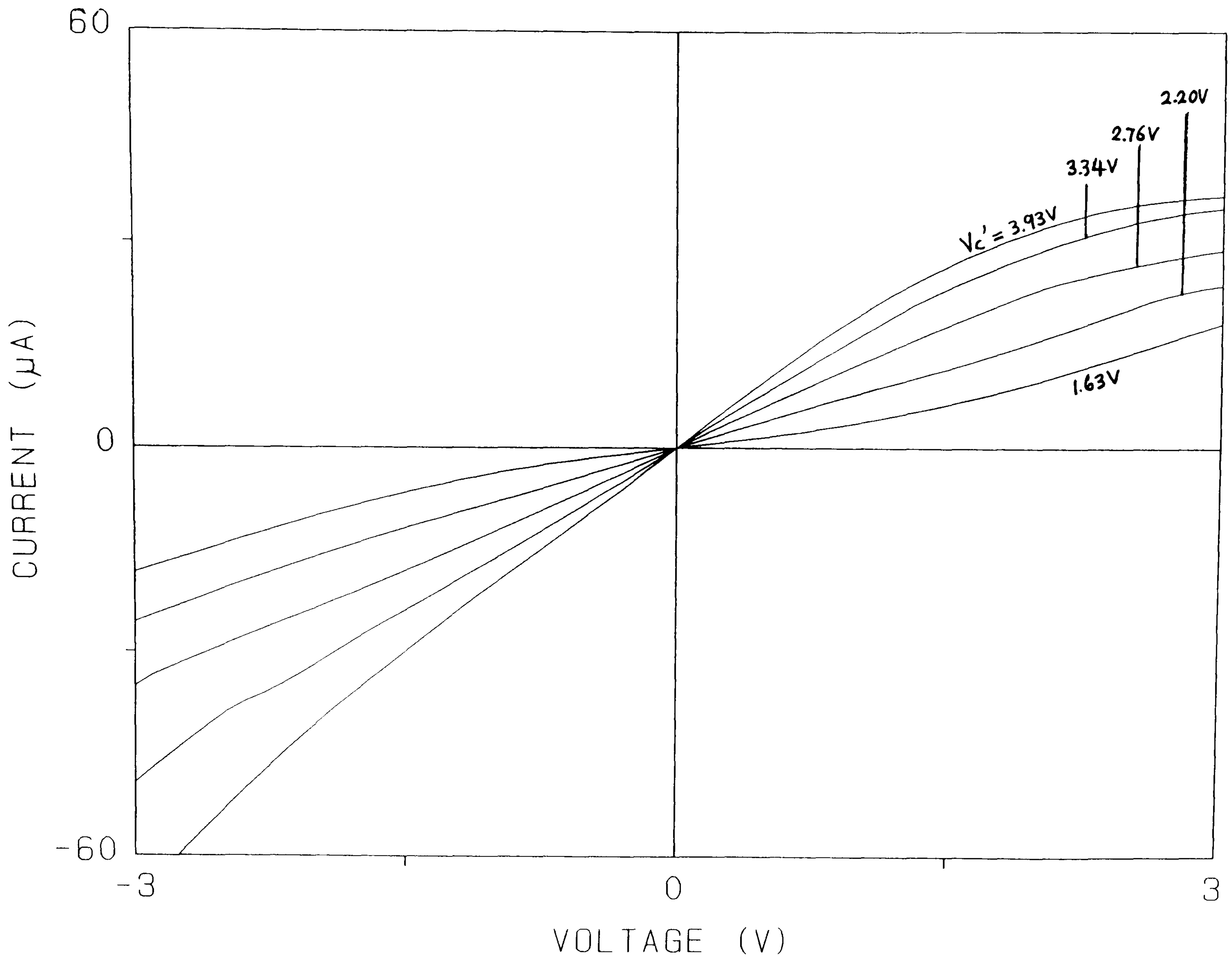


Figure 3.14: Control voltage tuning of static characteristics for dual gate-bulk compensation SPQR-II

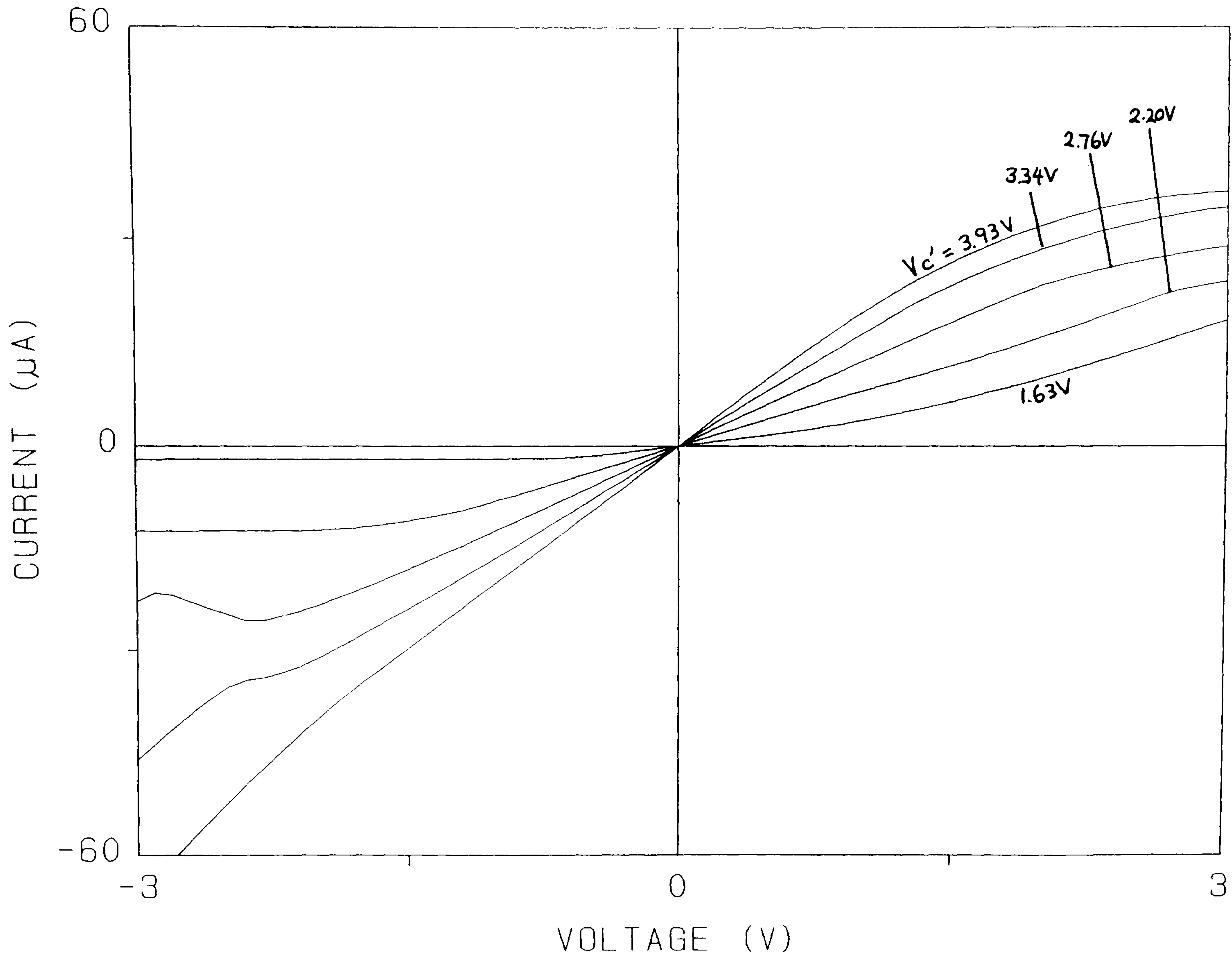


Figure 3.15: Control voltage tuning of static characteristics for dual gate-bulk compensation SPQR-III

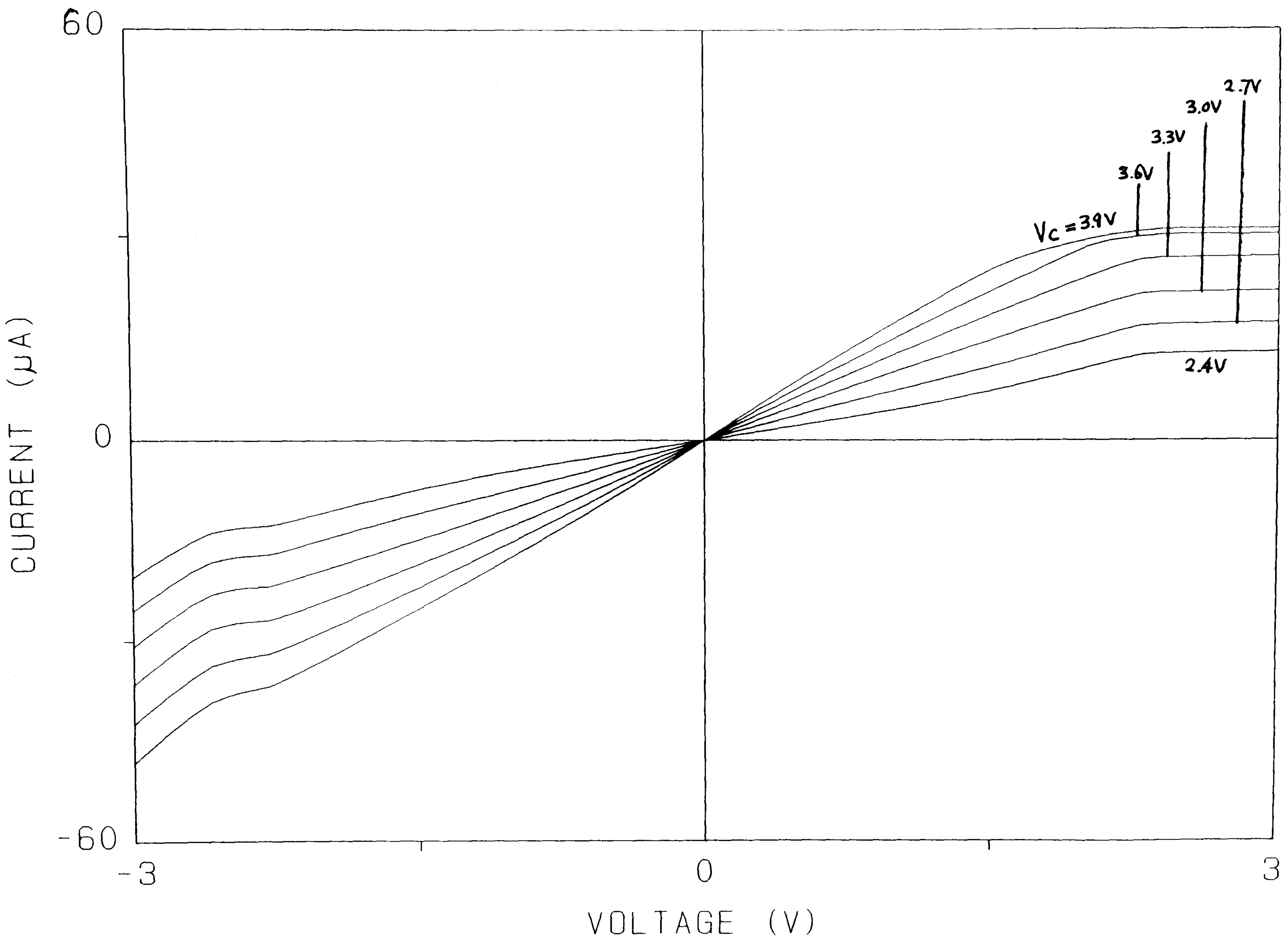


Figure 3.16: Control voltage tuning of static characteristics for scaled-gate compensation GVCR

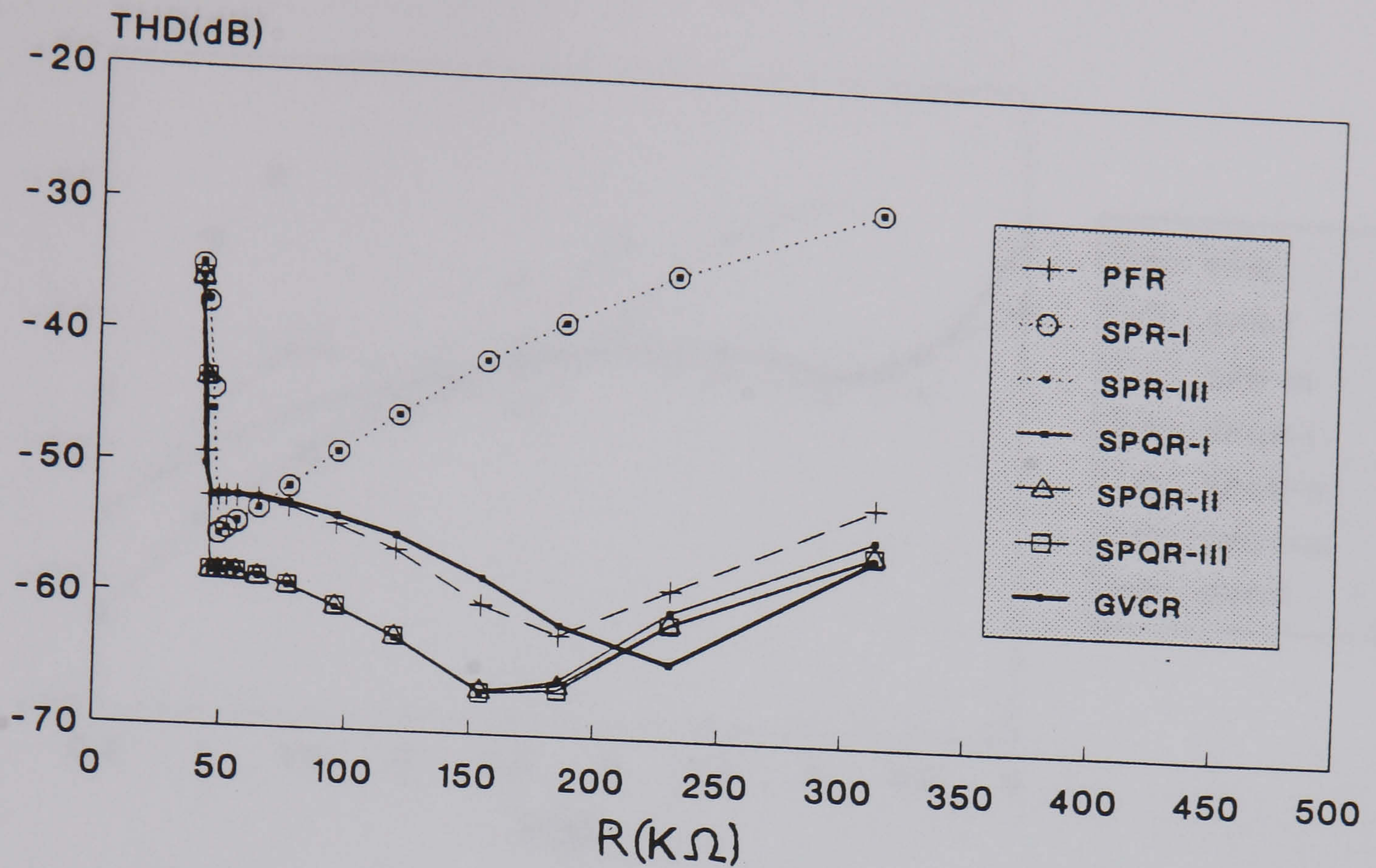


Figure 3.17: THD of dual gate-bulk and scaled-gate compensation resistors with different resistance values at $0.5V_{pp}$, $\theta = 0.15V^{-1}$ and $\pm 5V$ supply

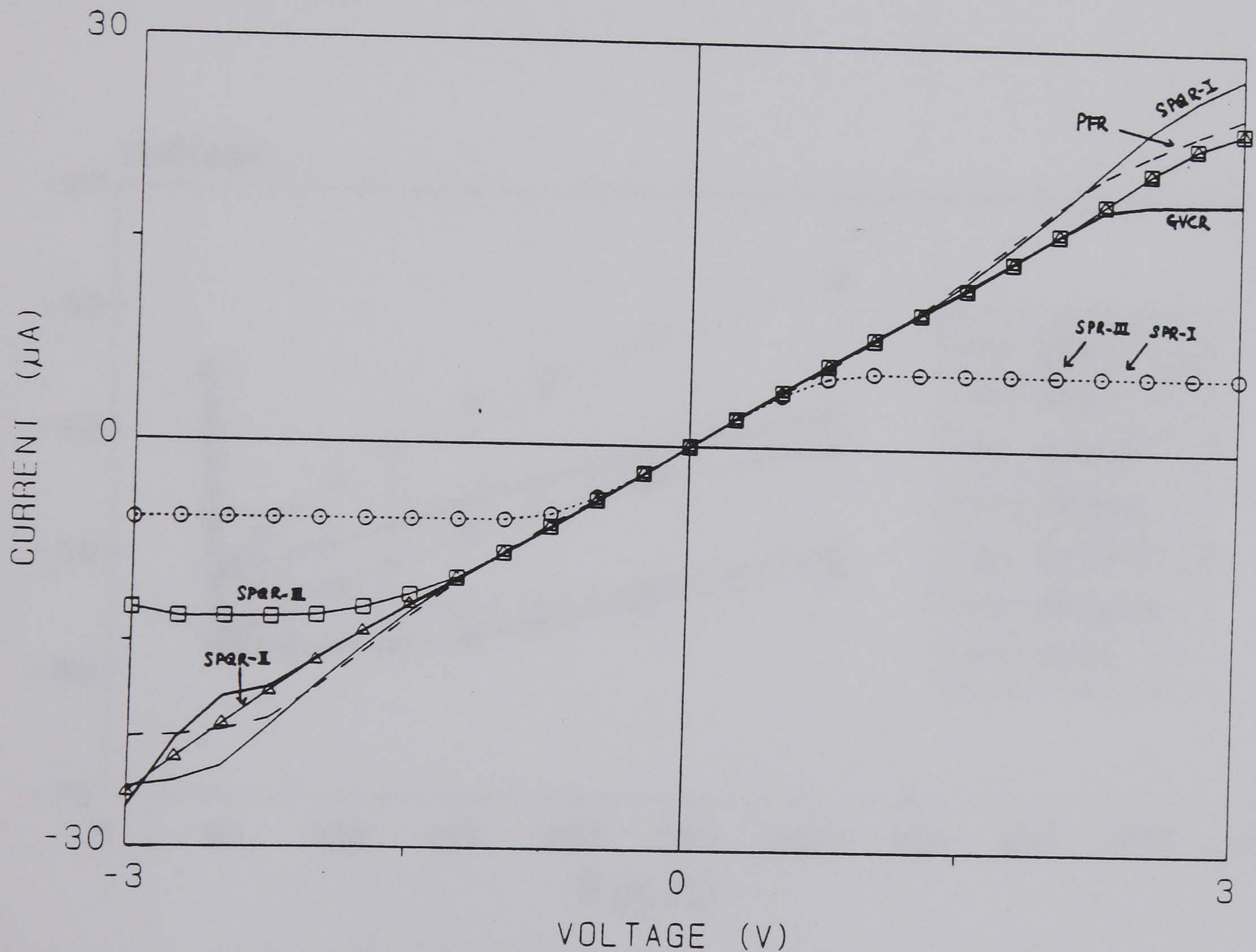


Figure 3.18: Static characteristics of dual gate-bulk and scaled-gate compensation resistors for nominal resistance ($120K\Omega$)

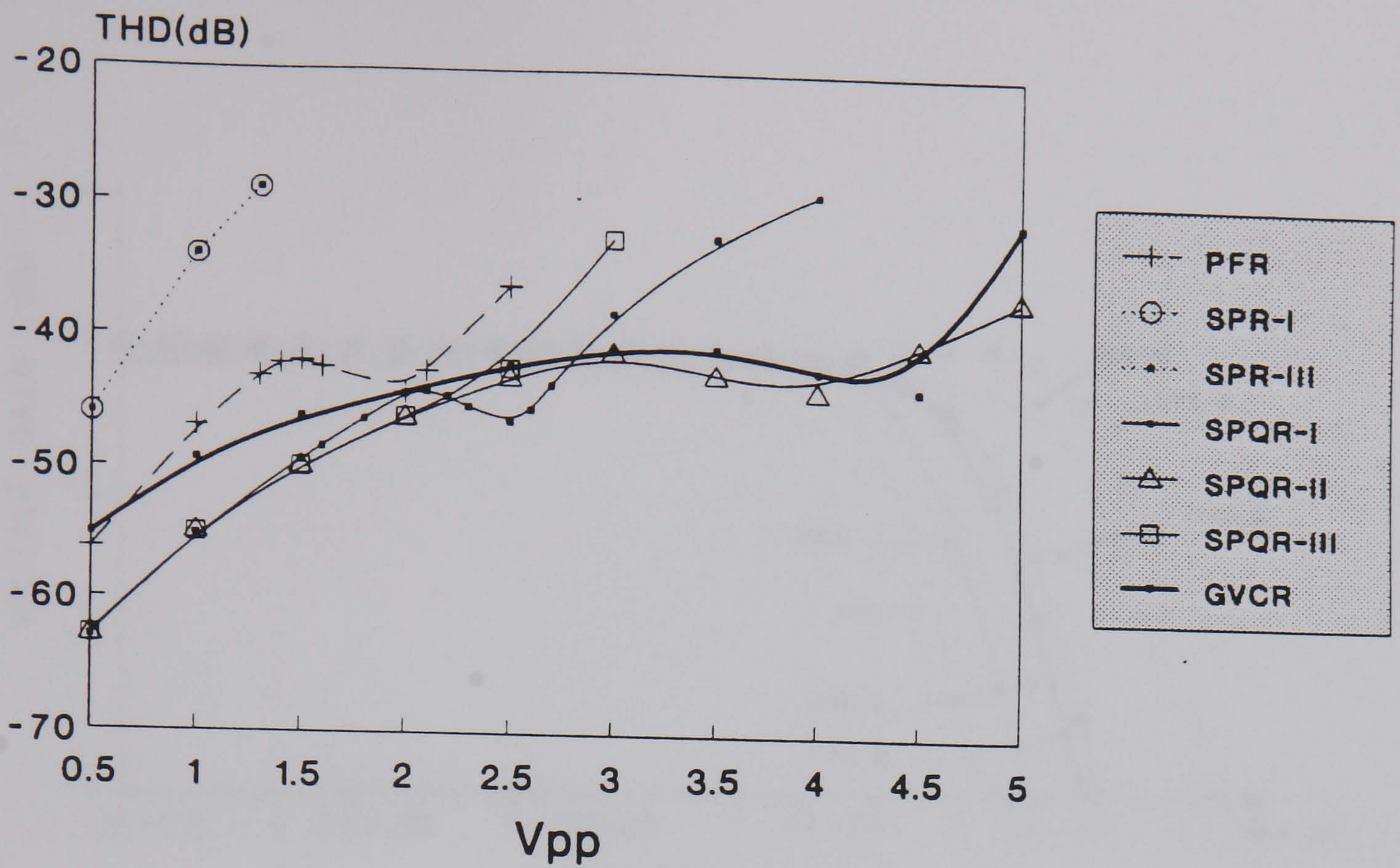


Figure 3.19: THD of dual gate-bulk and scaled-gate compensation resistors against input signal for nominal resistance ($120K\Omega$)

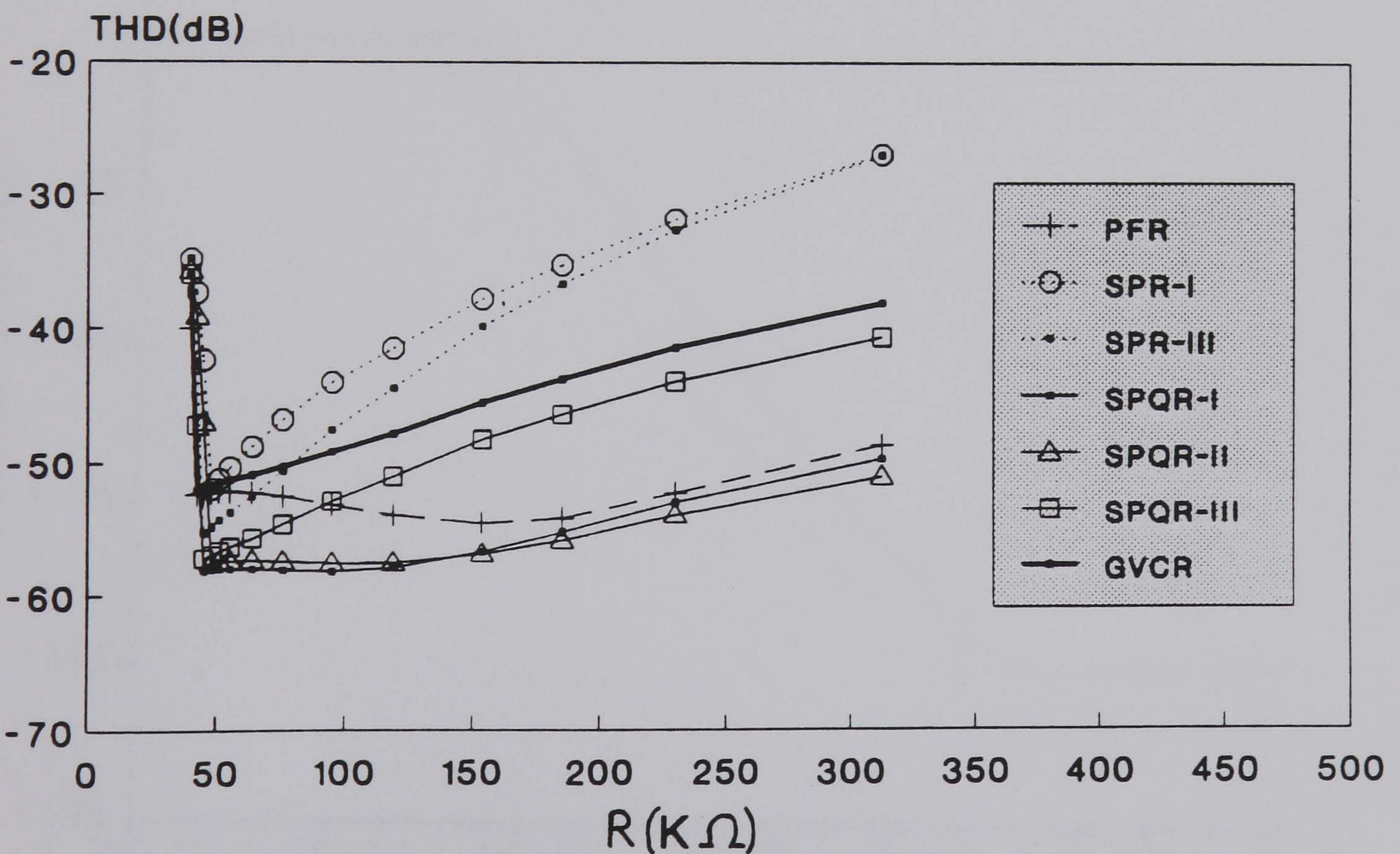


Figure 3.20: THD of dual gate-bulk and scaled-gate compensation resistor with different resistance values at $0.5V_{pp}$ for $\pm 2\%$ mismatches

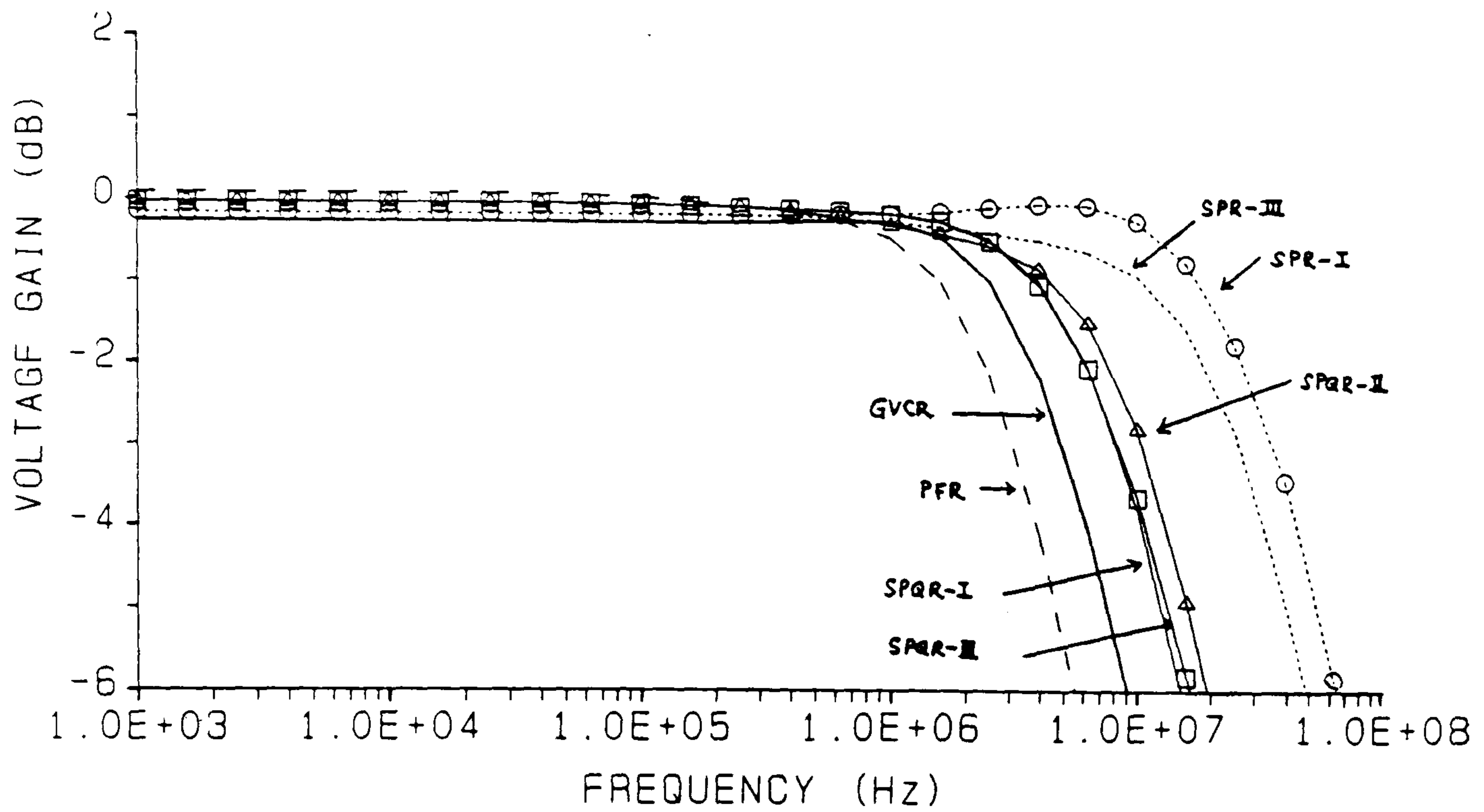


Figure 3.21: Bandwidth of dual gate-bulk and scaled-gate compensation resistors at nominal resistance ($120K\Omega$)

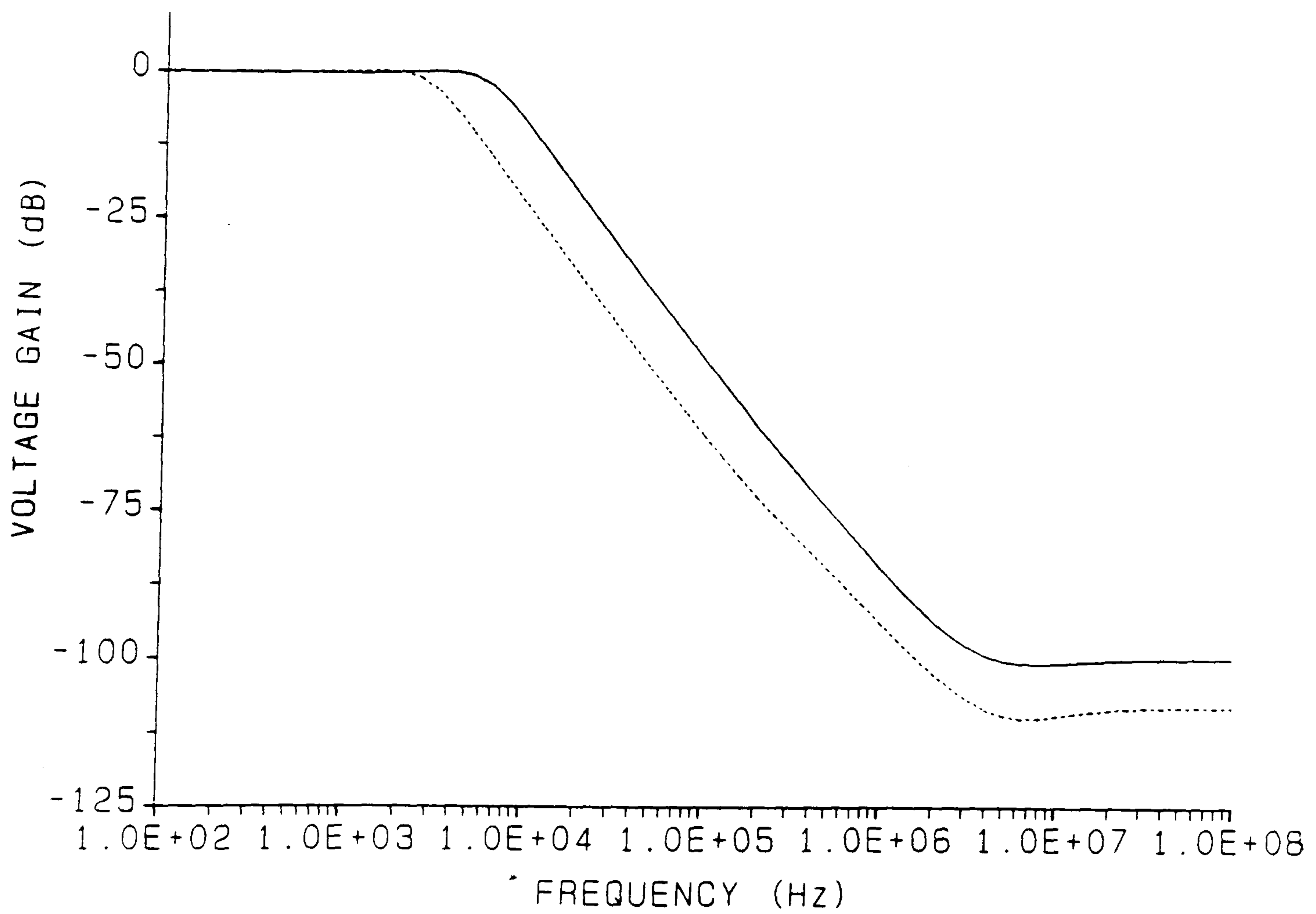


Figure 3.22: Tuning of lowpass cut-off frequency in the GVCR-based filter

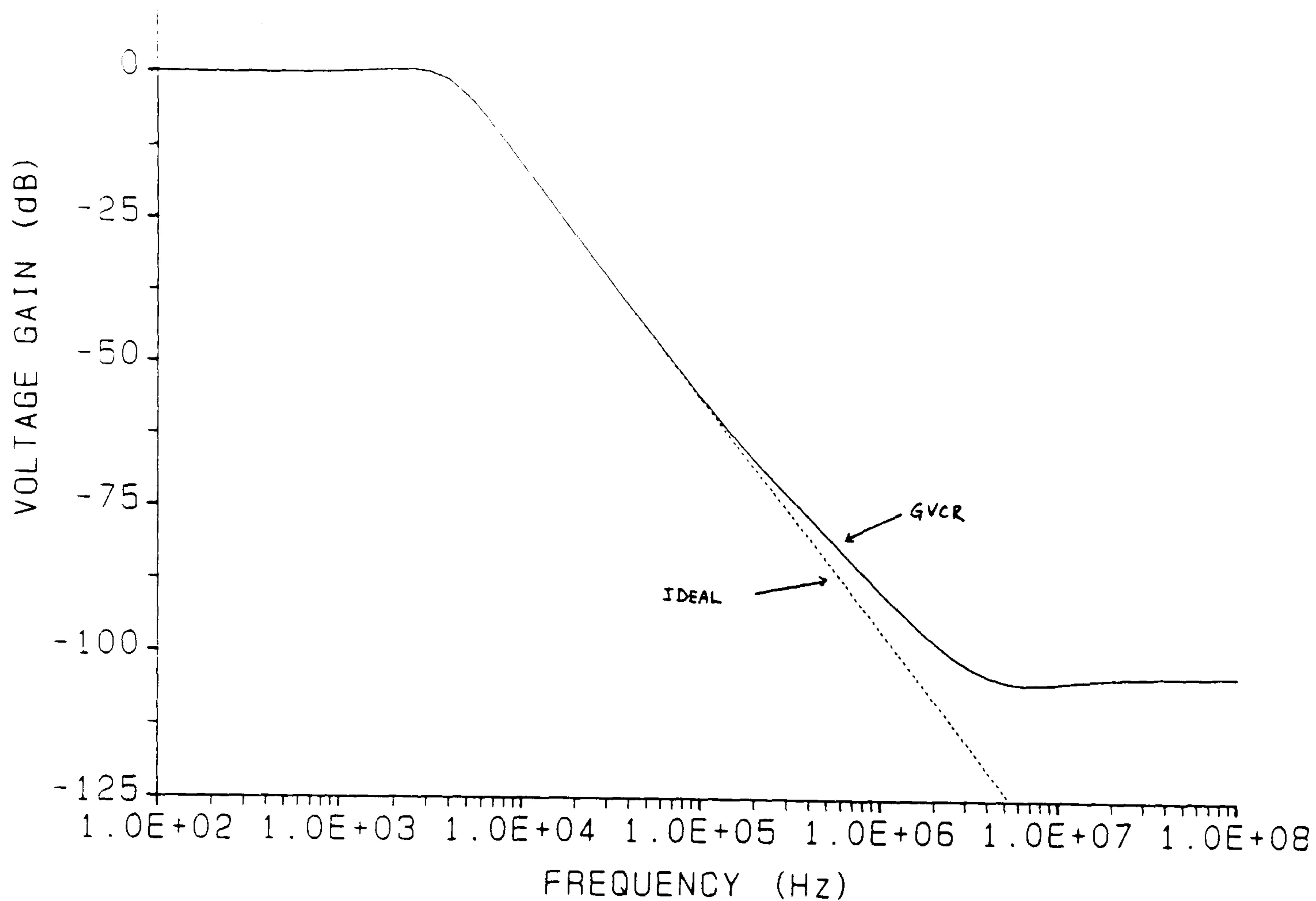


Figure 3.23: Comparison of simulated and ideal frequency characteristic at nominal $4.7KHz$ cut-off frequency

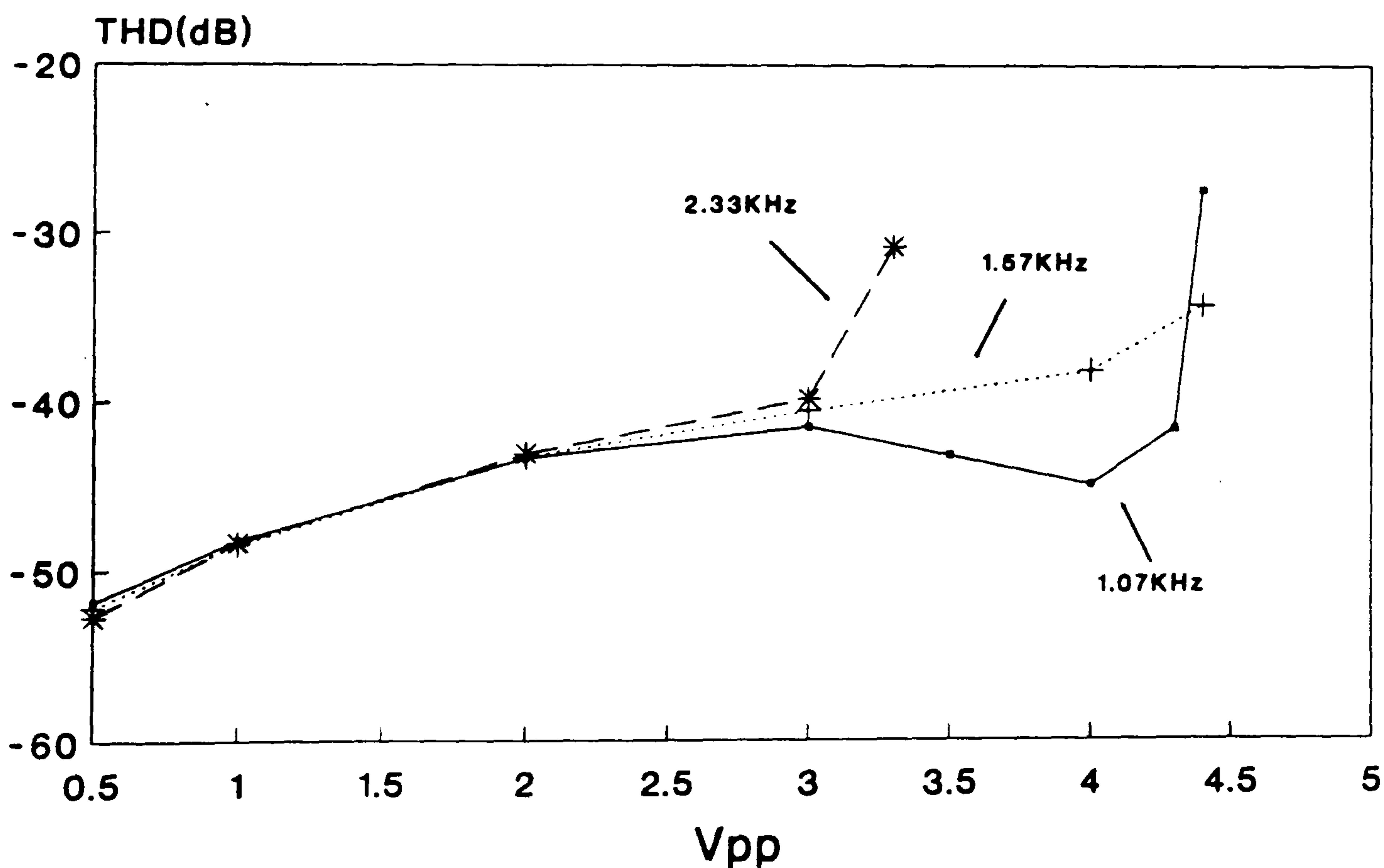


Figure 3.24: THD with variation of input signal at different frequencies (1/3 of cut-off frequencies) for GVCR-based filter

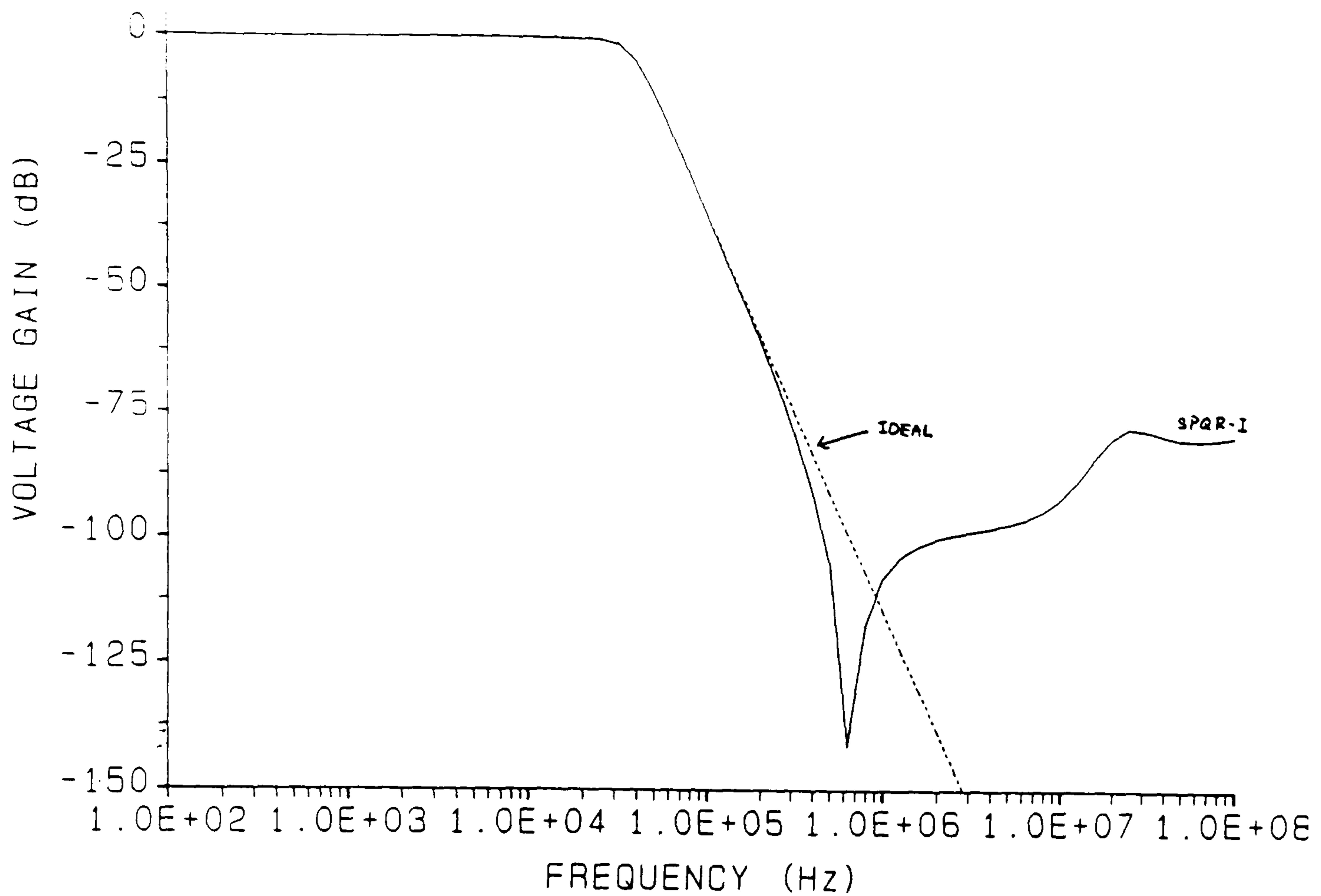


Figure 3.25: Comparison of simulated and ideal frequency characteristic at nominal $37KHz$ cut-off frequency for SPQR-based filter

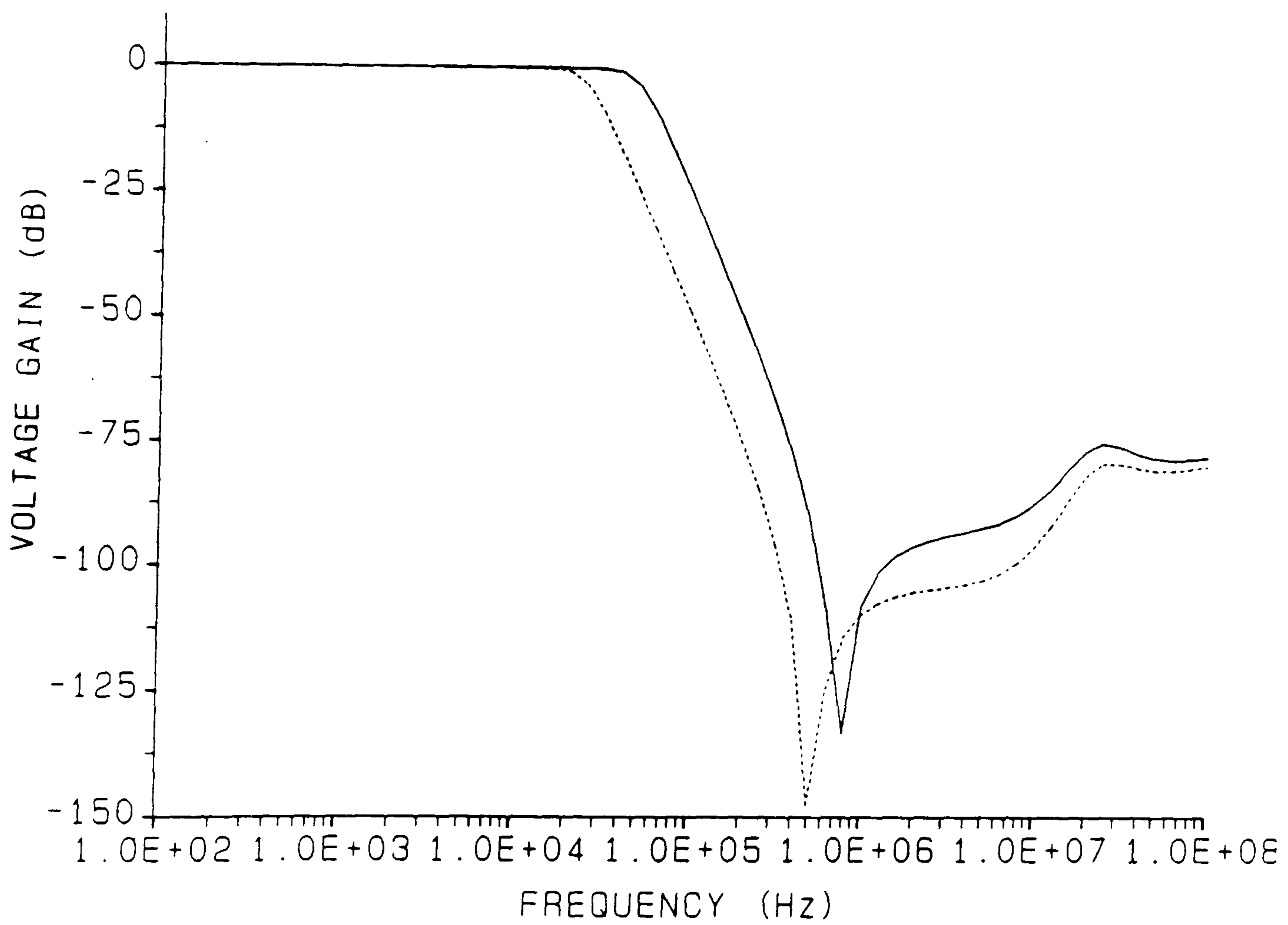


Figure 3.26: Tuning of lowpass cut-off frequency in the SPQR-based filter

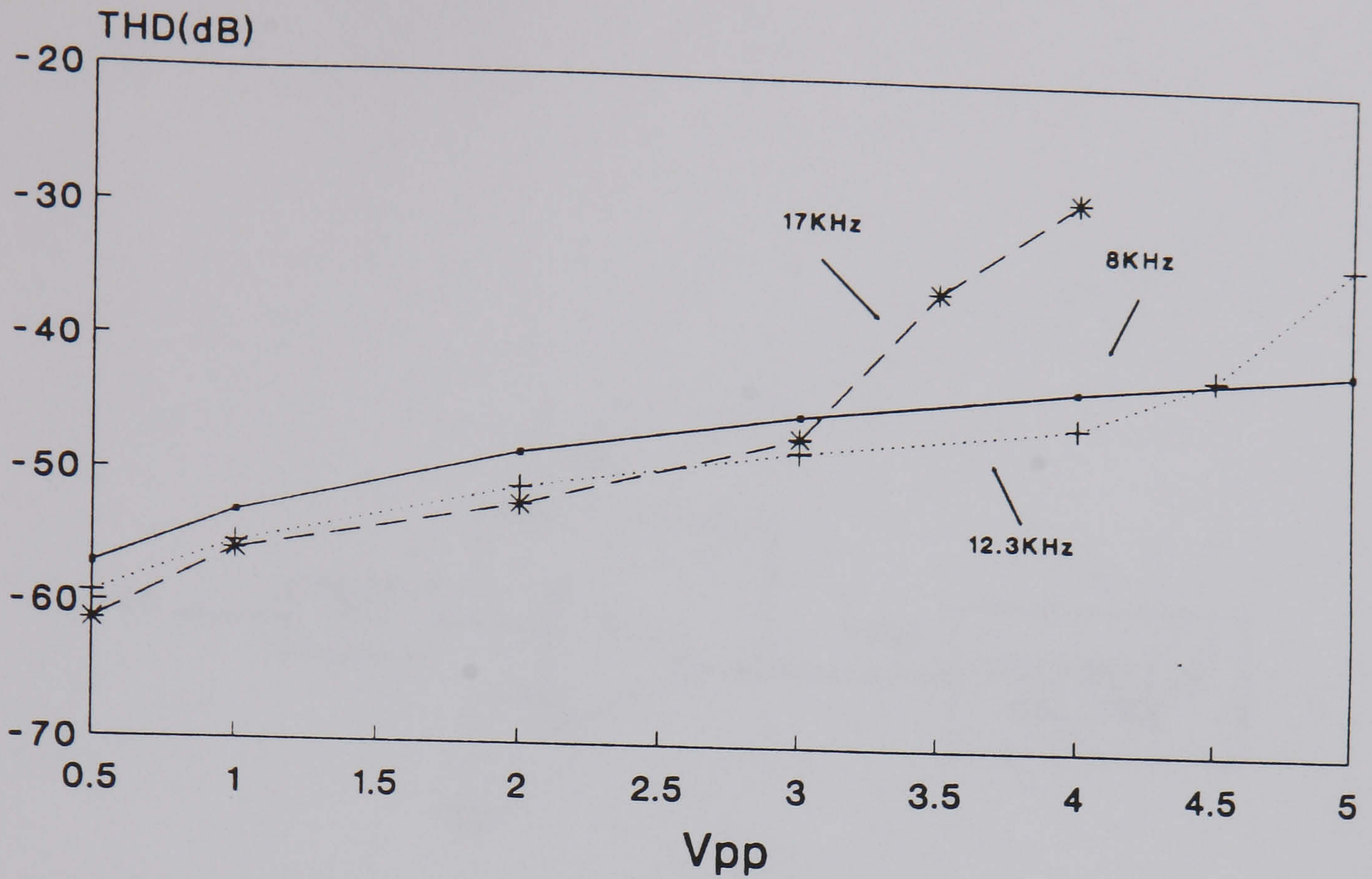


Figure 3.27: THD with variation of input signal at different frequencies (1/3 of cut-off frequencies) for SPQR-based filter

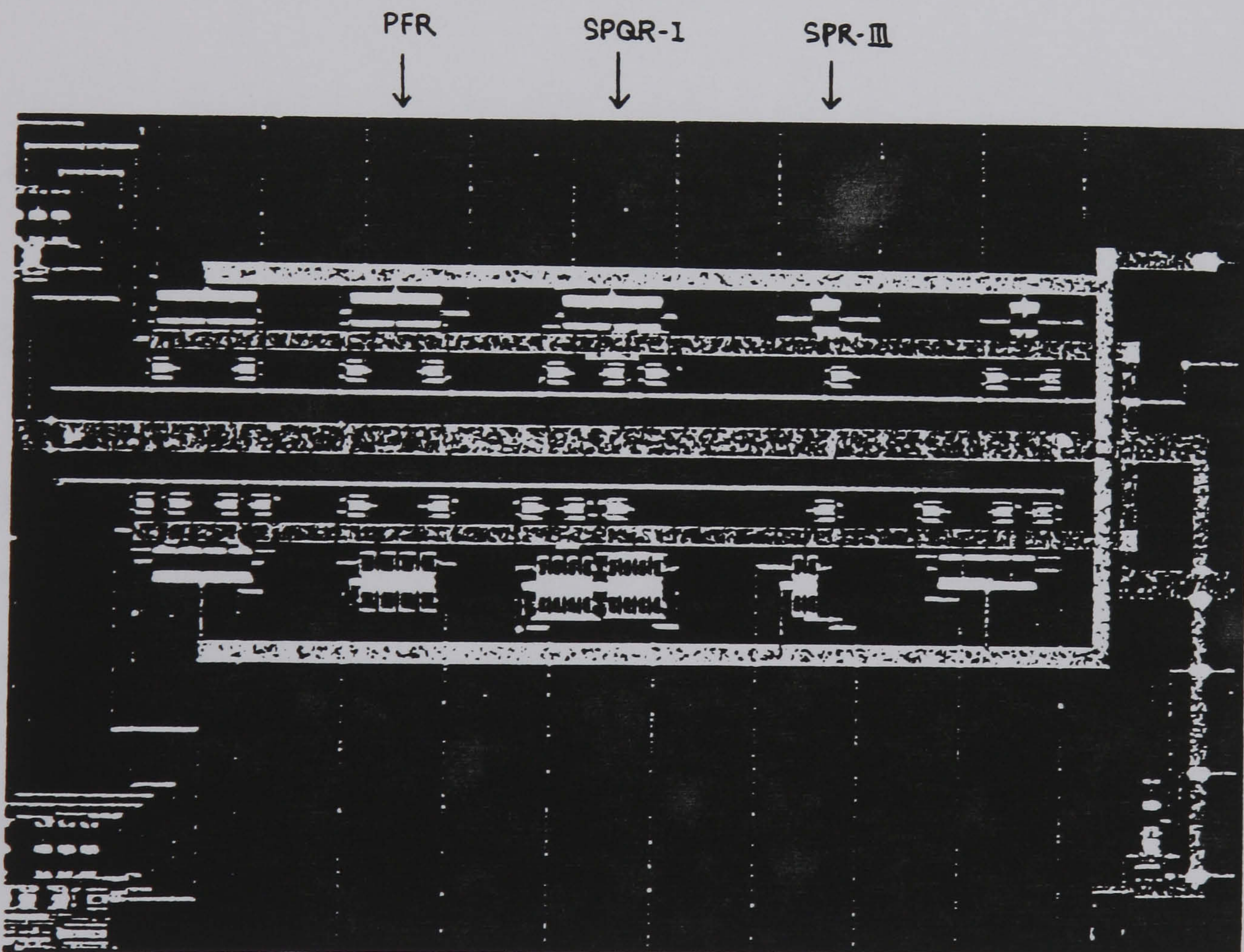


Figure 3.28: A microphotograh of unscaled-gate compensation CMOS resistors

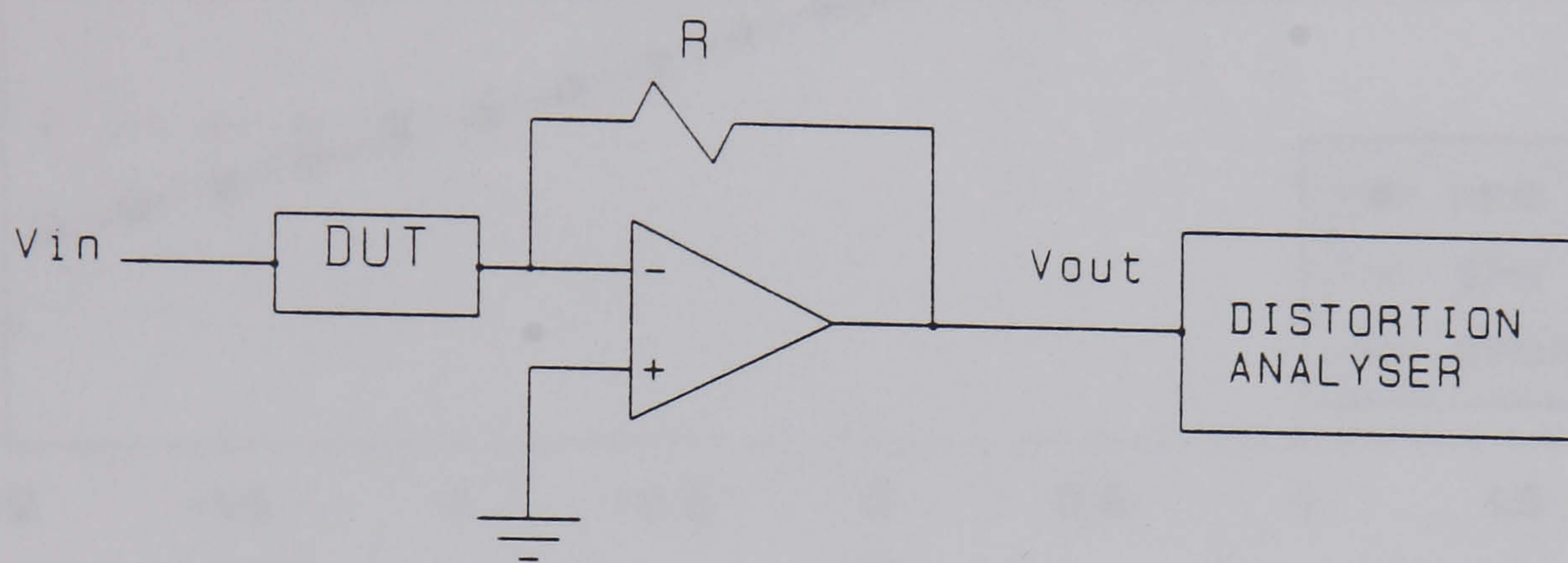


Figure 3.29: Experimental set-up for measuring total harmonic distortion of test resistor

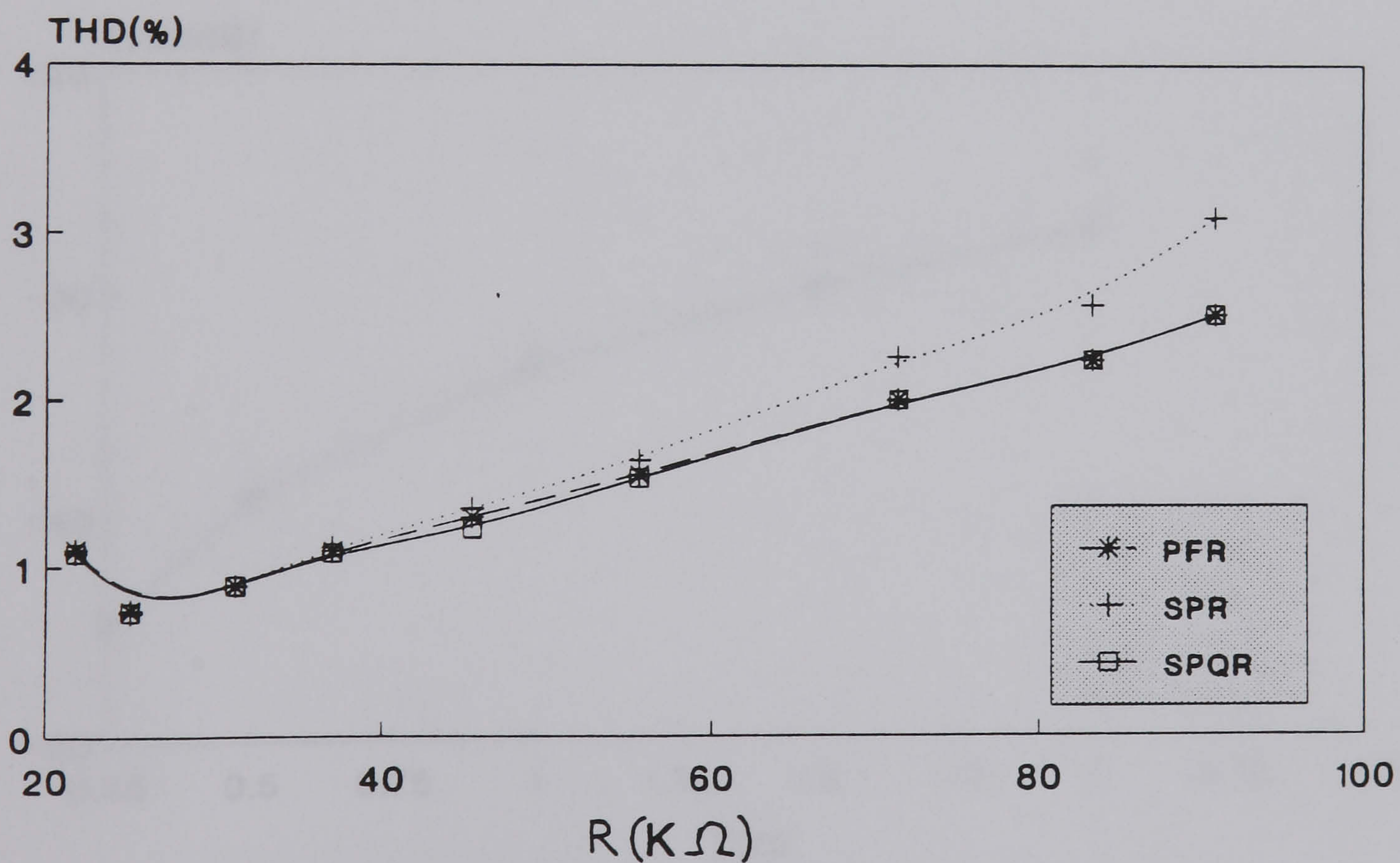


Figure 3.30: Experimental THD comparison of PFR, SPR-III and SPQR-I with variation of resistance values at $0.5V_{pp}$

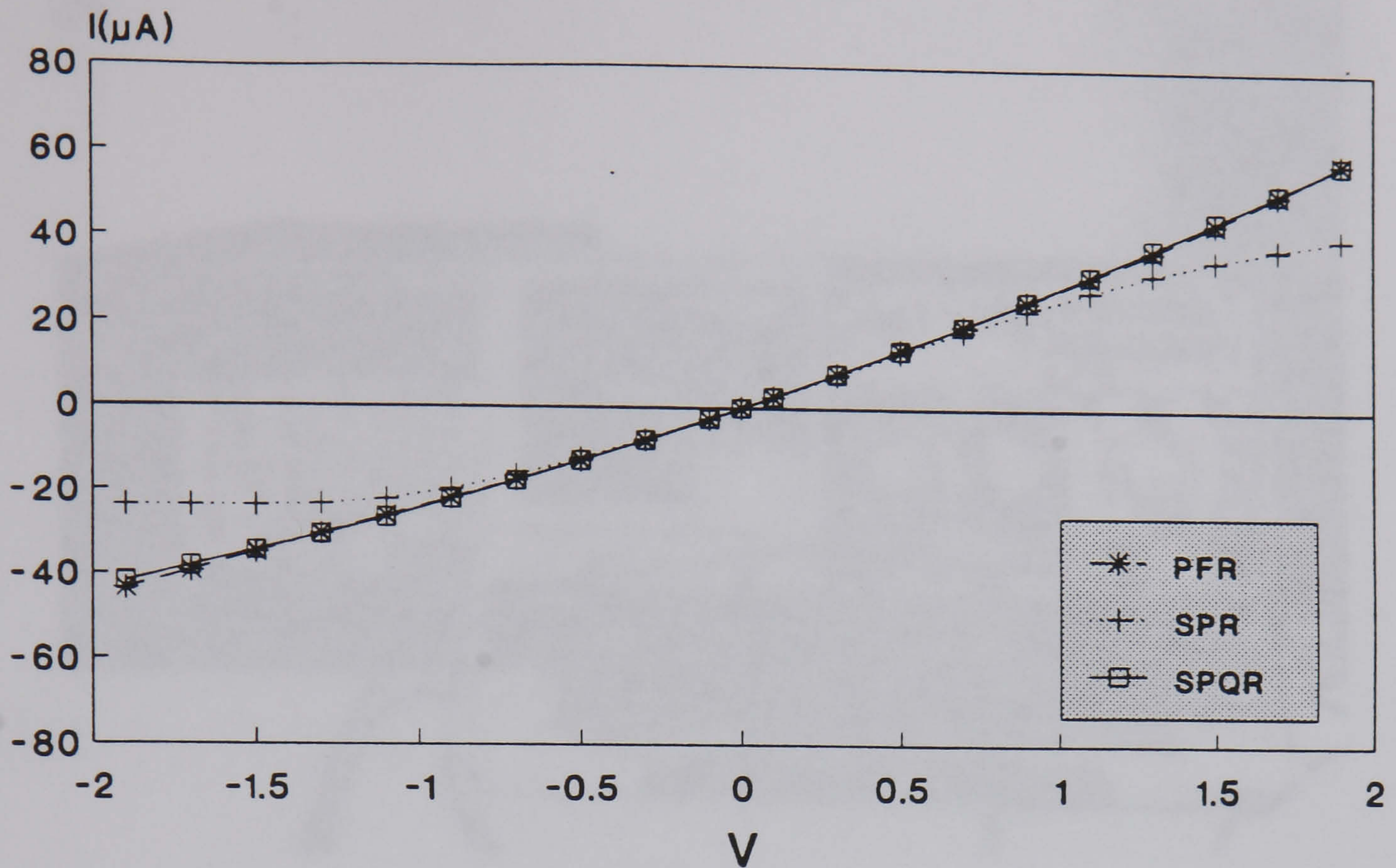


Figure 3.31: Experimental comparison of static characteristics for PFR, SPR-III and SPQR-I at the nominal resistance of $37K\Omega$

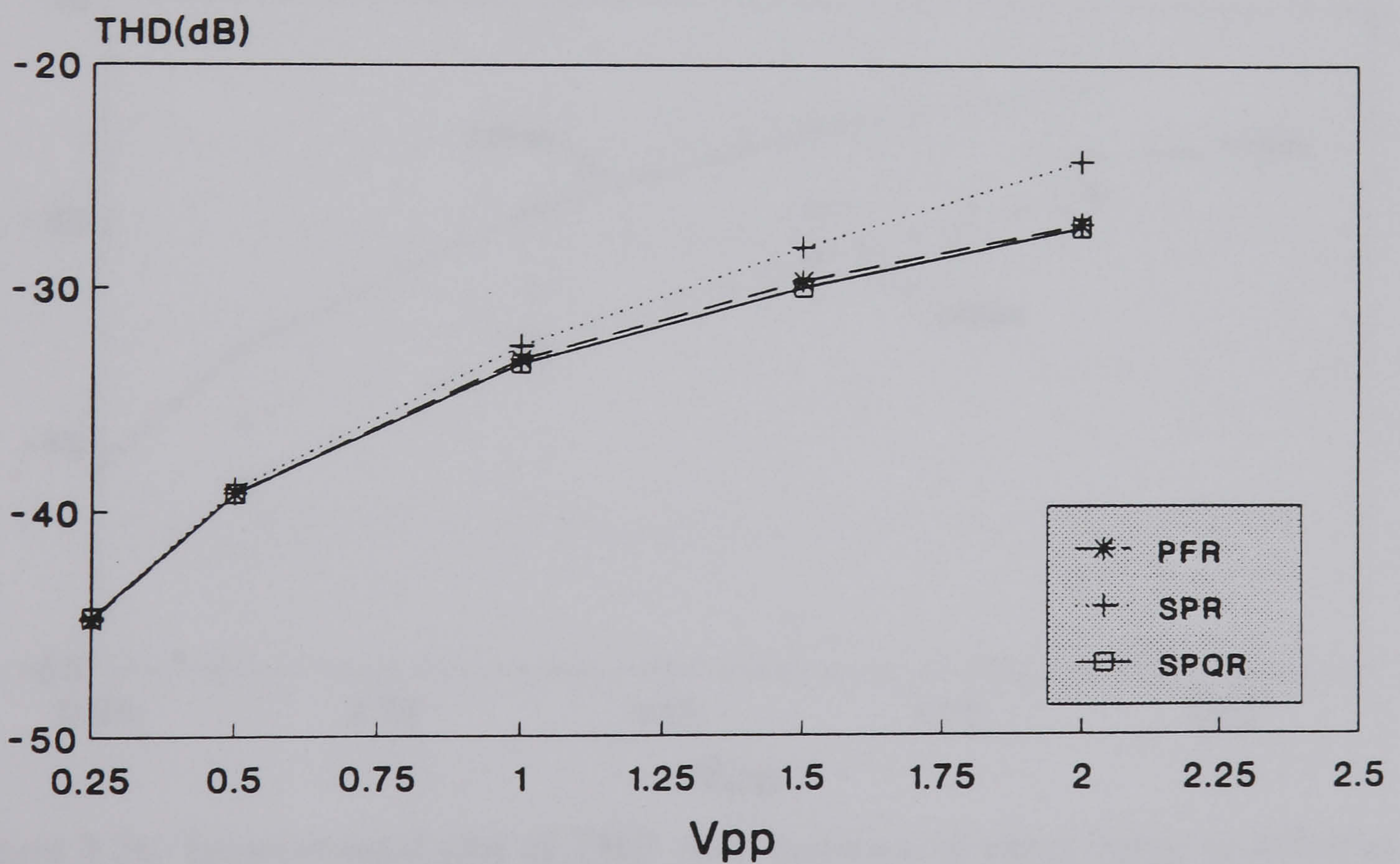


Figure 3.32: Experimental THD comparion of PFR, SPR-III and SPQR-I against input signal at the nominal resistance of $37K\Omega$

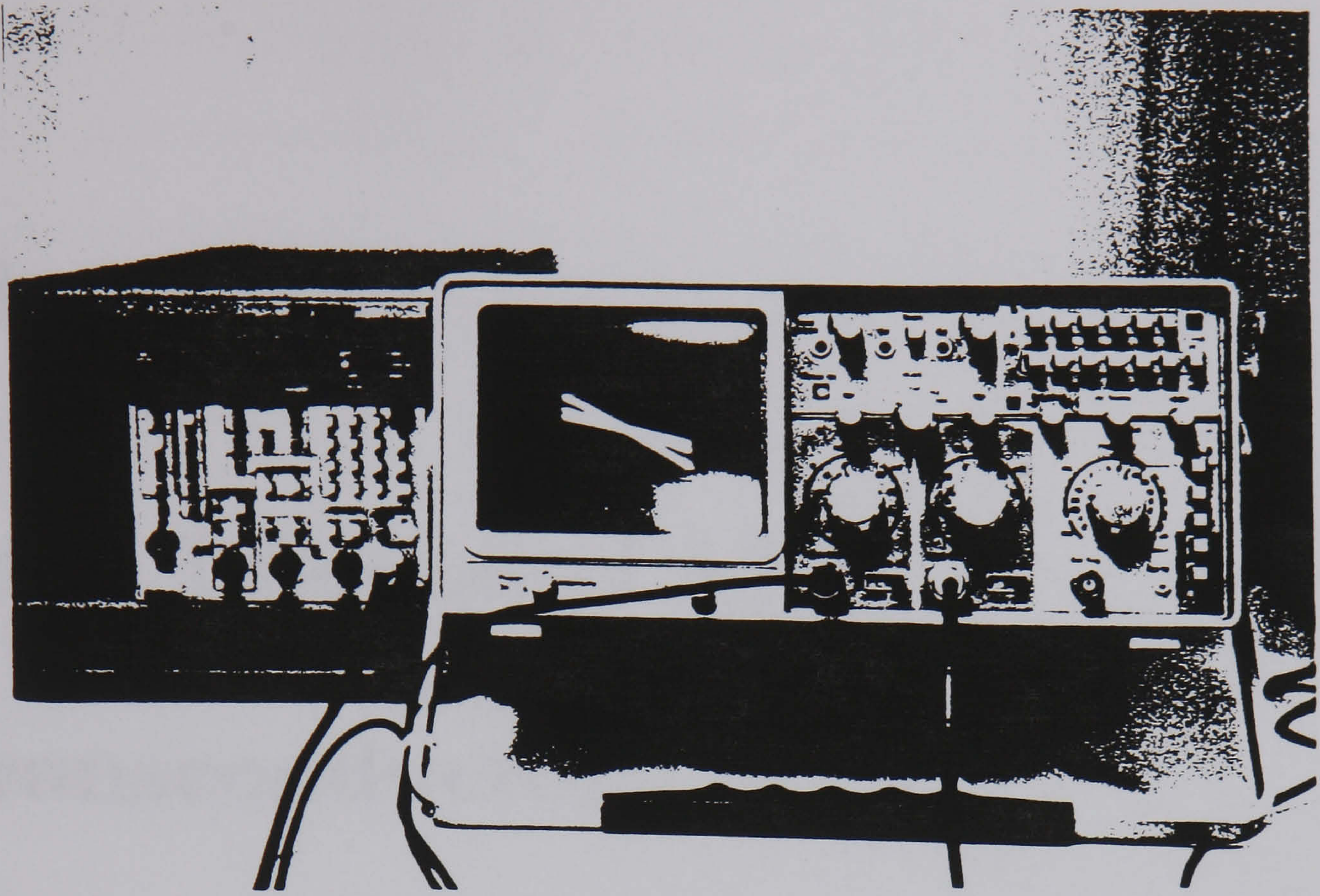


Figure 3.33: Experimental family static characteristics of the SPQR-I

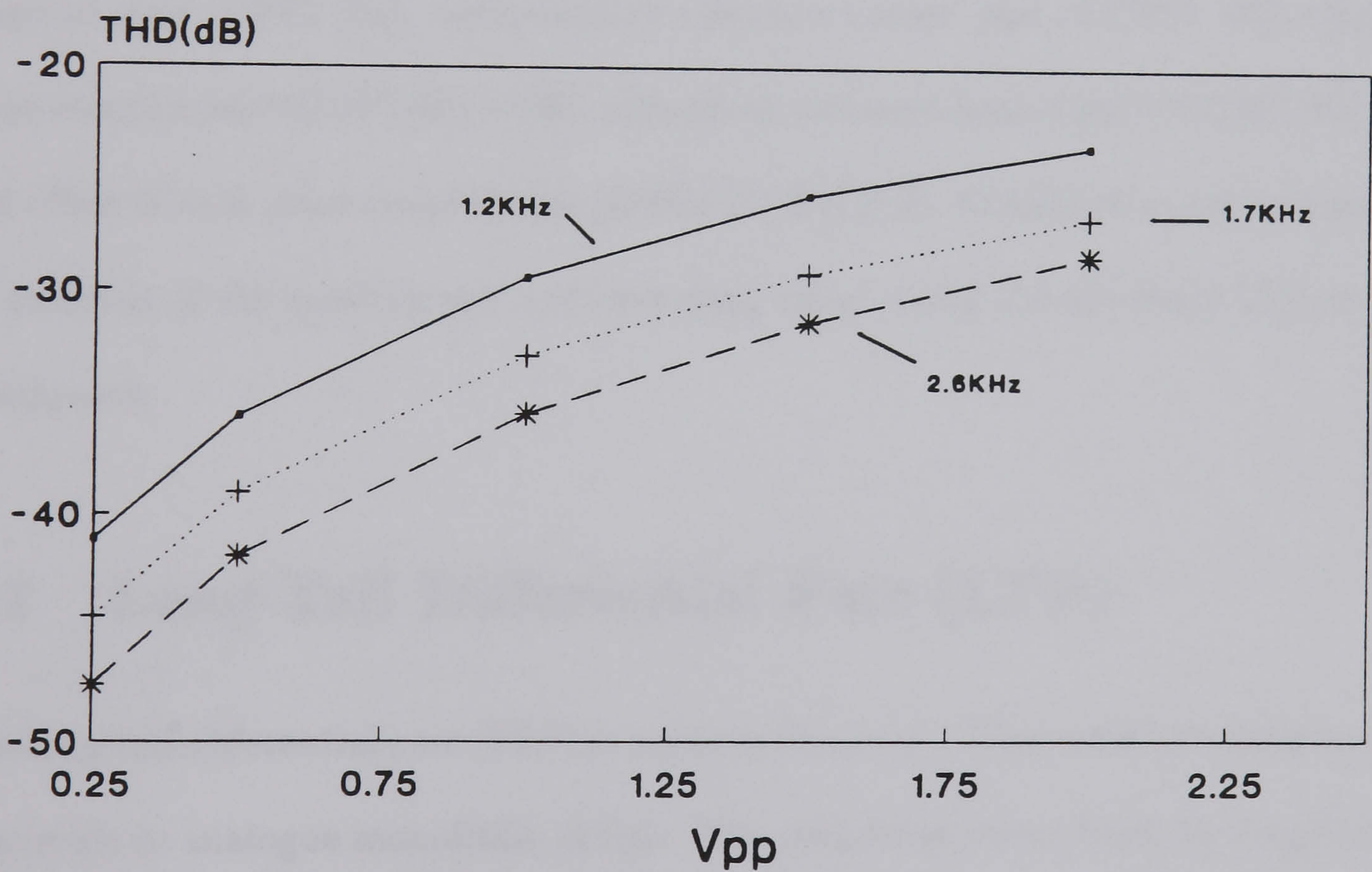


Figure 3.34: Experimental plot of THD with variation of input signal at different frequencies (1/3 of cut-off frequencies) for second-order Sallen-Key lowpass based on the SPQR-I

Chapter 4

Fully Integrated MOS Transconductors

Linearisation techniques and circuit configurations for saturation-mode transconductors are discussed in this chapter. These transconductors are designated as long-tail pair (LTP) [54], compensated common-source pair (CCSP) [60]→[62], cross-coupled pair (CCP) [65]→[68], anti-phase common-source pair (ACSP) [63],[64] and offset-biased cross-coupled pair (OBCCP) [69],[70]. Attention is concentrated on analyses of the nonlinearity and operating range using the standard LTP as a benchmark.

4.1 Long-Tail Differential Pair (LTP)

The long-tail differential pair (LTP) is perhaps the most widely used two-transistor subcircuit in analogue monolithic design. The usefulness stems from its simplicity and versatility as basic building block. Thus, the LTP transconductor is not only attractive but also serve a useful benchmark role. Unfortunately, as has been shown, the nonlinearity generated by the constant-current operation limits the

signal-handling capability, and some form of linearisation is normally be required.

Consider the matched differential pair with constant current-sink shown in Fig 4.1. In the following analysis, it will be assumed that the output current subtraction circuit (current mirror not shown in the figure) is ideal, and effects such as channel-length modulation, bulk modulation and velocity saturation, etc. are negligible. With the additional assumption that the devices operate in saturation, the adoption of a simple square-law model given by Eqn (E.17) (which also assumes constant mobility) leads to simplified analytical expressions for the purpose of illustrating operating principles.

The constant-current biasing can be represented by the equivalent voltage-source-based representation shown in Fig. 4.2. The dc source V_Q models the quiescent bias of the differential pair, while the pair of ac voltage sources defines the complex signal $f(v)$ appearing at node M consisting of the common-mode ac component $v_c = (v_1 + v_2)/2$ and a nonlinear generator v_n. The common-mode component results from the symmetry and source-follower-like structure of the differential pair, whereas the nonlinearity is required in order to account for the absence of even-order distortion terms in the drain currents. Expressions for V_Q and v_n can be developed as follows.

For the matched differential pair shown in Fig. 4.1, the voltage v_M generated at the common-source node generally consists of a dc bias component V_Q and an ac component f(v) to be determined. Hence,

$$v_M = V_Q + f(v) \tag{4.1}$$

The drain currents for MA1 and MA2 are

$$I_1 = I + i = K[v_1 - V_Q - f(v) - V_{TO}]^2 \tag{4.2}$$

and

$$I_2 = I - i = K[v_2 - V_Q - f(v) - V_{TO}]^2 \tag{4.3}$$

where the gate overdrive

$$V_Q + V_{TO} = -\sqrt{\frac{I}{K}} \tag{4.4}$$

defines the quiescent current I, V_{TO} is the threshold voltage at zero source-to-bulk voltage and $K = \mu C_{ox} W/2L$ is the transconductance parameter. μ is the carrier mobility (assumed equal to μ_o), C_{ox} is the capacitance per unit gate area, W is the channel width, and L is the channel length.

The transfer characterisic is obtained as a special case of the SDP in Chapter 1 (see also [47],[60]) as

$$I_o = I_1 - I_2 = 2i = GV_{in}\sqrt{1 - \frac{KV_{in}^2}{4I}} \tag{4.5}$$

where the ideal ac transconductance parameter G is defined as

$$G = 2\sqrt{KI} \tag{4.6}$$

and $V_{in} = v_1 - v_2$ is the differential input voltage.

Although the symmetry of the long-tailed pair normally ensures sufficient rejection of even-order distortion terms, it can be seen from Eqn (4.5) that a dominant bias-dependent cubic term is generated. It follows from Eqn (4.5) that for a given transconductance, cubic distortion can be reduced either by increasing the bias current or reducing the aspect ratio (W/L).

Subtracting Eqn (4.3) from (4.2) and equating to (4.5) yields

$$f(v) = \frac{v_1 + v_2}{2} + \sqrt{\frac{I}{K}}(1 - \sqrt{1 - \frac{KV_{in}^2}{4I}}) \tag{4.7}$$

which identifies $f(v)$ as the sum of an ac common-mode signal and a nonlinear signal, which it may be noted, is a direct consequence of the constant current biasing.

Substituting Eqns (4.5) and (4.6) into (4.2), (4.3), gives

$$I_1 = K(\frac{V_{in}}{2} + \sqrt{\frac{I}{K}}\sqrt{1 - \frac{KV_{in}^2}{4I}})^2 \tag{4.8}$$

and

$$I_2 = K(-\frac{V_{in}}{2} + \sqrt{\frac{I}{K}}\sqrt{1 - \frac{KV_{in}^2}{4I}})^2 \tag{4.9}$$

from which an upper and lower limit to the operating range can be found by setting $I_1, I_2 = 0$. Thus

$$-\sqrt{2}\sqrt{\frac{I}{K}} < V_{in} < \sqrt{2}\sqrt{\frac{I}{K}} \tag{4.10}$$

as a result of the constant current operation, when the differential input signal exceeds the values defined above, the drain currents saturate at $2I$ and 0 as appropriate.

With the accurate square-law model of Eqn (E.13), where mobility degradation effect is taken into account, the output current in Appendix K can be expressed as

$$I_o = I_1 - I_2 = G_1 V_{in} + G_3 V_{in}^3 \tag{4.11}$$

where

$$G_1 = \frac{(2 + \theta V_b)}{(1 + \theta V_b)^2} K_{oc} V_b \tag{4.12}$$

and

$$G_3 = -\frac{1 + (1 + \theta V_b)^2}{(2 + \theta V_b)(1 + \theta V_b)^4} \frac{K_{oc}}{4V_b} \tag{4.13}$$

Note that K_{oc} and V_b are defined in Apendix A and K, respectively.

It can be seen that the mobility degradation effect causes reduction of the linear transconductance G_1 and has a pronounced effect on the relative magnitude of the nonlinear term G_3. With increasing θ, the denominator increases much faster than the numerator in G_3, consequently reducing the coefficent G_3. The linear

term G_1, on the other hand, does not change as rapidly as G_3. The linearity of the LTP can therefore be enhanced by using processes with higher mobility factor.

4.2 Compensated Common-Source Pair (CCSP)

The limited signal swing of the LTP has generated a group of linearisation techniques for CMOS transconductors. Perhaps the best known $V - I$ converter [60],[61] is shown in Fig. 4.3. The schematic diagram of the CCSP transconductor has already been outlined in Fig. 1.13(b). Referring to Fig. 4.3, the linearisation process consists of generating a compensating tail current I_t as a function of the differential-input voltage from auxiliary cross-coupled pairs formed by MB3→MB6, which is subsequently passed to the source-coupled pair MB1-MB2 via a level-shifter transistor MB7.

With Eqn (4.5) rewritten as

$$I_o = V_{in}\sqrt{K(4I_t - KV_{in}^2)}, \tag{4.14}$$

it can be seen that, in principle, the output current can be linearised by setting the tail current to

$$I_t = I + \frac{KV_{in}^2}{4} \tag{4.15}$$

in which case,

$$I_o = GV_{in} \tag{4.16}$$

Other authors [62] implement a similar type of transconductor by means of a current-squaring circuit and a mirror-copy circuit to generate the tail current function. Unfortunately, the current-squaring circuit increases the transistor stack level, thus decreasing both the signal-handling capability and tunability.

It will be useful to examine the potential generated at the common source node under these conditions. Consider Fig. 4.3, and let v_N be expressed as

$$v_N = V_Q + g(v) \tag{4.17}$$

The currents flowing through transistors MB1 and MB2 are

$$I_1 = K[v_1 - V_Q - g(v) - V_{TO}]^2 \tag{4.18}$$

and

$$I_2 = K[v_2 - V_Q - g(v) - V_{TO}]^2 \tag{4.19}$$

which with Eqns (4.14) and (4.15) yield

$$g(v) = \frac{v_1 + v_2}{2} \tag{4.20}$$

Alternatively, $g(v)$ can also be identified by setting $I_1 + I_2 = I_t$. Both approaches give the same result. Thus $g(v)$ is a purely common-mode signal and results in each input transistor being driven in an antiphase mode by the difference signal $V_{in}/2$.

From Eqns (4.18) and (4.19), the operating range can be obtained as

$$-2\sqrt{\frac{I}{K}} < V_{in} < 2\sqrt{\frac{I}{K}} \tag{4.21}$$

and is a factor of $\sqrt{2}$ wider than that for the long-tailed pair due to the reduction of signal swing in the common-source node N.

Consider the ac signals v_X and v_Y for the the auxiliary differential pair employing transistors of different aspect ratios. The aspect ratio for MB3 and MB6 is related to MB4 and MB5 by a factor of n. Thus the current relationship is obtained as

$$I_3 + I_4 = I_4 + I_5 = (n + 1)I \tag{4.22}$$

The source node potentials can be solved as

$$v_X = \frac{nv_1 + v_2}{n+1} - \frac{(nv_1 + v_2)^2}{2\sqrt{\frac{I}{K}}(n+1)^2} + \frac{nv_1^2 + v_2^2}{2\sqrt{\frac{I}{K}}(n+1)} + V_Q \tag{4.23}$$

and

$$v_Y = \frac{nv_2 + v_1}{n+1} - \frac{(nv_2 + v_1)^2}{2\sqrt{\frac{I}{K}}(n+1)^2} + \frac{nv_2^2 + v_1^2}{2\sqrt{\frac{I}{K}}(n+1)} + V_Q \tag{4.24}$$

where V_Q is defined in Eqn (4.4).

The amplitude of v_X and v_Y depends on the choice of n. For $n = 1$, the differential-pair transistors have identical aspect ratios. Under this condition, $v_X = v_Y = v_N$. In order to compensate the LTP nonlinearity [60], n is required to be 2.155.

The ideal transconductance predicted by these relationships is not achieved in practice since unavoidable second-order effects, amongst which mobility degradation [62],[66] has a dominant role, results in some degree of nonlinearity.

Using the mobility model in Eqn (E.13), it has been shown in Appendix L that the current difference expression is

$$I_o = I_1 - I_2 = G_1 V_{in} + G_3 V_{in}^3 \tag{4.25}$$

where

$$G_1 = \frac{(2 + \theta V_b)}{(1 + \theta V_b)^2} K_{oc} V_b \tag{4.26}$$

and

$$G_3 = -\frac{\theta K_{oc}}{4(1 + \theta V_b)^4} \tag{4.27}$$

In this case, mobility degradation reduces the transconductance as for the LTP, but the contribution to odd-order distortion is significantly different. Eqn (4.27) reveals that lowering mobility factor can improve linearity. This is, in sharp contrast with the LTP where the linearity is enhanced by increasing the mobility

degradation factor. In practice, the odd-order distortion in the CCSP could be expected to be smaller than that in the LTP.

4.3 Cross-Coupled Pair (CCP)

A cross-coupled linearisation technique has been proposed by Viswanathan [65]. The schematic diagram for this transconductor is given in Fig. 4.4. For the cross-coupled pair, the inputs v_1 and v_2 are directly coupled to the respective gates and together with an appropriate dc offset V_Q' are buffered onto the opposite source terminals. This arrangement results in an antiphase drive to each device equal to the full differential input $(v_1 - v_2)$ with the sources offset by V_Q' volts relative to signal ground.

The implementation shown in Fig. 4.5 employs two shunt-feedback buffers to establish cross coupling and dc biasing for the two-transistor cell MC1-MC2 and in principle offers an ideal linear $v{\sim}i$ conversion. Other authors have offered different circuit configurations such as the compound p-n complementary pair [66],[69] and current feedback voltage source [67],[68] to achieve the same linearisation effect.

Assume that the quiescent current I' flowing via the transistors MC1-MC2 establishes a direct potential V_Q' at their source nodes as shown in Fig. 4.5. If the transistor pairs MC1-MC2 and MC3-MC4 are matched and have transconductance K', the drain currents are

$$I_1 = K'[V_{in} - (V_Q' + V_{TO})]^2 \tag{4.28}$$

and

$$I_2 = K'[-V_{in} - (V_Q' + V_{TO})]^2 \tag{4.29}$$

where $V_Q' + V_{TO} = -\sqrt{\frac{I'}{K'}}$. Thus, the difference current output is

$$I_o = I_1 - I_2 = 4\sqrt{K'I'}V_{in} = G'V_{in} \tag{4.30}$$

In order to provide a proper basis for identical transconductance comparison, K' and I' are selected to set $G' = G$, and $V_Q' = V_Q$ which can only be satisfied when $K' = K/2$ and $I' = I/2$.

From Eqns (4.25) and (4.26), the operating range becomes

$$-\sqrt{\frac{I}{K}} < V_{in} < \sqrt{\frac{I}{K}} \tag{4.31}$$

and can be seen to be $\sqrt{2}$ times lower than that for the LTP.

In this case, an analysis of the mobility effect on distortion gives (Appendix M)

$$I_o = I_1 - I_2 = G_1 V_{in} + G_3 V_{in}^3 \tag{4.32}$$

where

$$G_1 = \frac{(2 + \theta V_b)}{(1 + \theta V_b)^2} K_{oc} V_b \tag{4.33}$$

and

$$G_3 = -\frac{\theta K_{oc}}{(1 + \theta V_b)^4} \tag{4.34}$$

from which it may be noted that the distortion coefficient G_3 is four times larger than that for the CCSP. This result reveals that higher signal swing not only increases the extent to which the devices are driven into cut-off but also leads to an increase in mobility-dependent distortion.

4.4 Anti-Phase Common-Source Pair (ACSP)

As previously noted, the LTP nonlinearity is a result of the constant current drive. It has also been noted that the current-mode compensation in the CCSP structure

results in a purely differential drive to the input transistors. This can, however, be achieved directly [63] by replacing the current drive with a common-mode voltage source v_c as depicted in Fig. 4.6 The implementation is shown in Fig. 4.7, and comprises an ac common-mode signal generator [47], a shunt-feedback buffer [65], together with a pair of common-source transistors MD1-MD2. The generator is configured as two series-connected differential pairs MD3-MD4, MD5-MD6 with tail currents equal to $2I_t$. The ac common-mode signal generated is coupled to the input pair via a source follower. The output of the source follower includes a quiescent drop V_Q formed by conducting MD7 with a bias current I. The buffer current I_B is chosen so as to ensure that MD1-MD2 operate in the desired input voltage range and has been set at $8I_t\mu A$.

The linearisation scheme can be alternatively achieved [64] by means of an additional operational amplifier together with a common-mode signal generator incorporating passive resistors. However, this increases the complexity and moreover requires passive integrated resistors.

Refer to Fig. 4.5, assuming the bias current I and transconductance K are identical to that for the LTP and CCSP, the drain currents are

$$I_1 = K[\frac{V_{in}}{2} - (V_Q + V_{TO})]^2 \quad (4.35)$$

and

$$I_2 = K[-\frac{V_{in}}{2} - (V_Q + V_{TO})]^2 \quad (4.36)$$

giving a difference output current $I_o = GV_{in}$. The input signal range is again given by Eqn (4.21). With mobility taken into account, the output current is as given by the CCSP transconductor result of Eqns (4.25) to (4.27).

4.5 Offset-Biased Cross-Coupled Pair (OBCCP)

It is typically the case that adjusting the quiescent drain current of devices in saturation-mode transconductors significantly reduces the signal handling capability. With stacked structures [55],[56],[62], [66],[71]→[73], the problem can be particularly pronounced. The major reason is that the operating range of the gate-overdrive bias is limited by the requirement that the constant-current sources remain in saturation and also by the cut-off behaviour of the transistor pair. Although the ACSP [63] and OBDP [74] transconductors address this problem by means of incorporating a shunt-feedback buffer and eliminating the current source respectively, the class-A buffer in the former case and the high gate-overdrive bias voltage establishing across the transistor pair in the latter case inevitably demand high power consumption. These drawbacks can be overcome in the case of the proposed offset-biased cross-coupled pair transconductor [70]. Since bipolar tuning gate voltages are employed, the range of gate-overdrive bias is extended and the tunability of transconductor for given input signal amplitude is enhanced. In addition, the current feedback technique [67] for sourcing the respective drain current of the transistor pair is class-AB, the power consumption is lowered. This offset-biased tuning approach has also been recently exploited by other authors in a cross-coupled structure [69].

The general arrangement of the OBCCP transconductor is illustrated in Fig. 4.8. It may be seen that this network differs in the way the controlled transistors ME1-ME2 are coupled to the input signals (v_1, v_2) and in the biasing arrangement by comparison with the CCP structure of Fig. 4.4. The inputs are preprocessed to form the weighted-sum functions as shown. This results in only half of the antiphase differential-input signal being applied to the respective controlled tran-

sistors. Linearisation is subsequently achieved by the subtraction of their drain currents.

The transconductor can be implemented as shown in Fig. 4.9. It consists of a controlled pair ME1-ME2, two series-connected differential pairs ME3-ME4, ME5-ME6, and two p-channel buffers ME7-ME8, ME9-ME10 together with associated mirror pairs. The signals generated at the source nodes of the differential pairs are cross coupled by the buffers to the gates of the controlled pair. The resulting antiphase gate-to-source voltages produce drain currents I_1 and I_2 which are also drawn from the source nodes by means of a current feedback technique. The output current is obtained by subtracting these two currents.

With reference to Fig. 4.9, assume that the controlled transistor pair has transconductance K whilst that for the transistors of the series-connected differential pair is K_t. Using Eqn (4.7), the weighted sums at the source nodes of the series-connected differential pairs are

$$v_a = \frac{3}{4}v_1 + \frac{1}{4}v_2 + v_n \qquad (4.37)$$

and

$$v_b = \frac{1}{4}v_1 + \frac{3}{4}v_2 + v_n \qquad (4.38)$$

where

$$v_n = \sqrt{\frac{I_t}{K_t}}(1 - \sqrt{1 - \frac{K_t V_{in}^2}{8I_t}}) \qquad (4.39)$$

and I_t is the quiescent level of the diffferential pair bias currents and also serves to define the dc offset:

$$V_Q'' = -(\sqrt{\frac{I_t}{K_t}} + V_{TO}) \qquad (4.40)$$

With v_a and v_b cross coupled to ME1 and ME2 as shown, the drain currents are

independent of v_n and can be written as

$$I_1 = K[v_a - v_b + V_B - V_Q'' - V_{TO}]^2 \tag{4.41}$$

and

$$I_2 = K[v_b - v_a + V_B - V_Q'' - V_{TO}]^2 \tag{4.42}$$

where V_B is the dc bias of the p-channel buffers. The difference-current expression

$$I_o = I_1 - I_2 = 2K(V_B + \sqrt{\frac{I_t}{K_t}})(v_1 - v_2) \tag{4.43}$$

is in principle, a purely linear function of the differential input and illustrates the dual tuning capability. The transconductance can be tuned by two parameters I_t and V_B. In practice, I_t would be fixed in conjunction with the appropriate choice of the aspect ratio of the differential pairs so as to maximise the signal-handling capability. The second tuning parameter V_B, can be dynamically modulated by adjusting the bias current through the buffers with an external control voltage V_C. The use of p-n complementary DC coupling provides a bipolar range for V_B and significantly enhances the tuning characteristics. The operating range is thus obtained as

$$-(V_B + \sqrt{\frac{I_t}{K_t}}) < V_{in} < (V_B + \sqrt{\frac{I_t}{K_t}}) \tag{4.44}$$

where $(V_B + \sqrt{\frac{I_t}{K_t}})$ is controlled by an appropriate combination of gate and source dc offsets chosen as as to maximise the tuning range. The allowable tuning voltage range (without imposing saturation constraints on the current sources) is usually greater than the $\sqrt{\frac{I}{K}}$ as defined for previous transconductors. For a comparison, using identical transconductance, $V_B + \sqrt{\frac{I_t}{K_t}} = \sqrt{\frac{I}{K}}$. The signal swings required to drive the LTP, CCSP, CCP, ACSP and OBCCP are in the ratio $\sqrt{2}$:2:1:2:2. Furthermore, since both junctions are driven in antiphase by $V_{in}/2$ rather than the full difference signal, the signal range over which the currents maintain a specified

linearity is significantly better than the structure in [69] (assuming identical supply voltages).

Mobility modulation effects will inevitably result in finite distortion levels. The mobility analysis given in Appendix N shows that

$$I_o = I_1 - I_2 = G_1 V_{in} + G_3 V_{in}^3 \tag{4.45}$$

where

$$G_1 = \frac{(2 + \theta V_b'')}{(1 + \theta V_b'')^2} K_{oc} V_b'' \tag{4.46}$$

and

$$G_3 = -\frac{\theta K_{oc}}{4(1 + \theta V_b'')^4} \tag{4.47}$$

The K_{oc} and V_b'' are defined in Apendix A and N, respectively. For $V_b'' = V_b$, the OBCCP exhibits similar mobility degradation effect to that of the CCSP and ACSP for a given transconductance.

4.6 Second-Order Effects

Mobility degradation effect plays an important role in the linearity performance of transconductors. It suppresses the third-harmonic distortion in the LTP but is a fundamental cause of odd-order distortion in the CCSP, ACSP, CCP, OBCCP and other saturation-mode or non-saturation-mode transconductors. It also results in a reduction of transconductance for all transconductors. In addition, other second-order effects may be considered, e.g. channel-length modulation, body effect, velocity saturation and device mismatching. In this study, the channel length of the input devices have been chosen to be greater than $10\mu m$, and channel-length modulation can therefore be neglected. The body effect it may be noted, can be suppressed by tying the body terminal of the transistor to the source terminal.

Velocity saturation, associated with the influence of lateral field on mobility has a pronounced effect when the channel length is short and is modelled by the term α as defined in Eqn (E.12). One can therefore predict the influence of velocity-saturation effect on linearity by replacing the gate-field-dependent mobility factor θ with $(\theta + \alpha)$ in all previous current expressions. In practice, for long-channel devices, θ is much greater than α. The inclusion of θ would normally be sufficient to predict the linearity of a transconductor based on a long-channel device. Although the symmetrical structures of converters suppress even-order nonlinearities, device mismatching does give rise to additional even-order distortion. Of course, the mismatching is related to circuit configuration and complexity. It can, however, be minimised through careful layout and employing transistors of large dimension at the cost of reducing high-frequency performance.

4.7 Transconductor-C Filter Example

Although the majority of active MOSFET-C filters are based around the voltage-controlled voltage source (operational amplifier), it has become increasingly apparent [21]→[23],[30] that such filters are limited by the complexity and finite gain-bandwidth of operational amplifiers. Operational transconductance amplifiers (OTAs), on the other hand, have significantly higher bandwidths than operational amplifiers. They also generally provide simpler circuitry for monolithic integration and allow for electronic tuning by changing bias currents. The following illustrative example shows how transconductance elements can be applied to the transconductor-C or OTA-C filter.

Fig. 4.10 presents a lowpass filter structure [41] using the ACSP transconductance elements. Assuming the transconductors have identical gain g_m, the transfer

function would be

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m^2}{C_1 C_2}}{s^2 + \frac{g_m}{C_2}s + \frac{g_m^2}{C_1 C_2}} \tag{4.48}$$

where the radian cut-off frequency is defined as

$$w_o = \frac{g_m}{\sqrt{C_1 C_2}} \tag{4.49}$$

and the quality factor obtained as

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{4.50}$$

It can be seen that the frequency can be controlled by tuning the transconductance gains simultaneously. Since the Q factor is defined by the ratio of the capacitance values, it is independent of the frequency tuning in this example. Setting $Q = 0.86$, $g_m = 20\mu A/V^2$, $C_1 = 925.3pF$ and $C_2 = 684.4pF$, the filter output would exhibit $0.5dB$ passband ripple and a $4.7KHz$ $3dB$ cut-off frequency. The simulation results are to be presented in Chapter 5.

This simple example of a second-order transconductance-C filter configuration uses only three OTAs and two capacitors. Due to simplicity and electronically controlled tuning feature, OTAs are likely to play an increasingly important role in analogue filter design and other signal-processing applications [92]→[96].

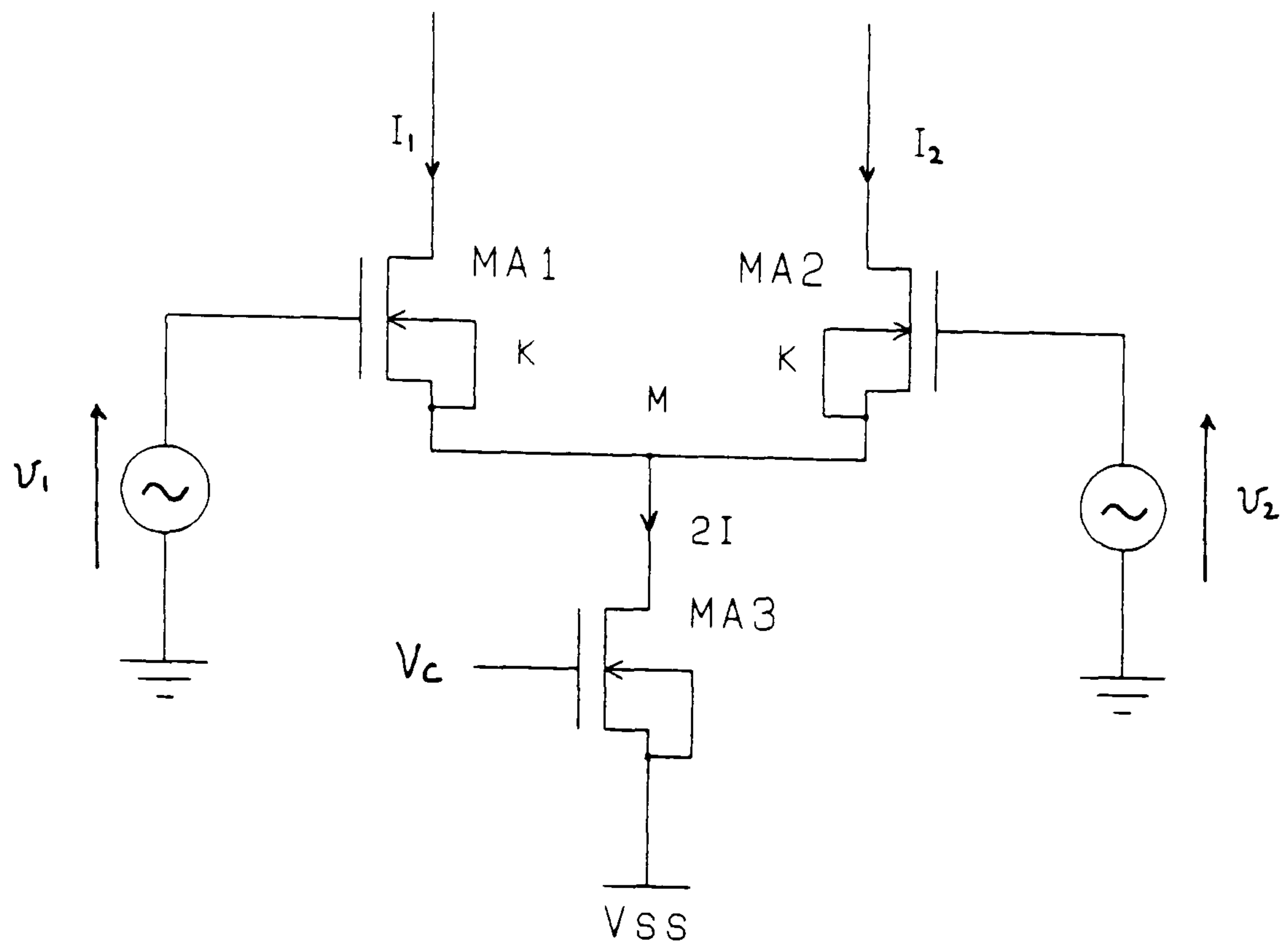


Figure 4.1: The differential-pair transconductor with constant-current biasing

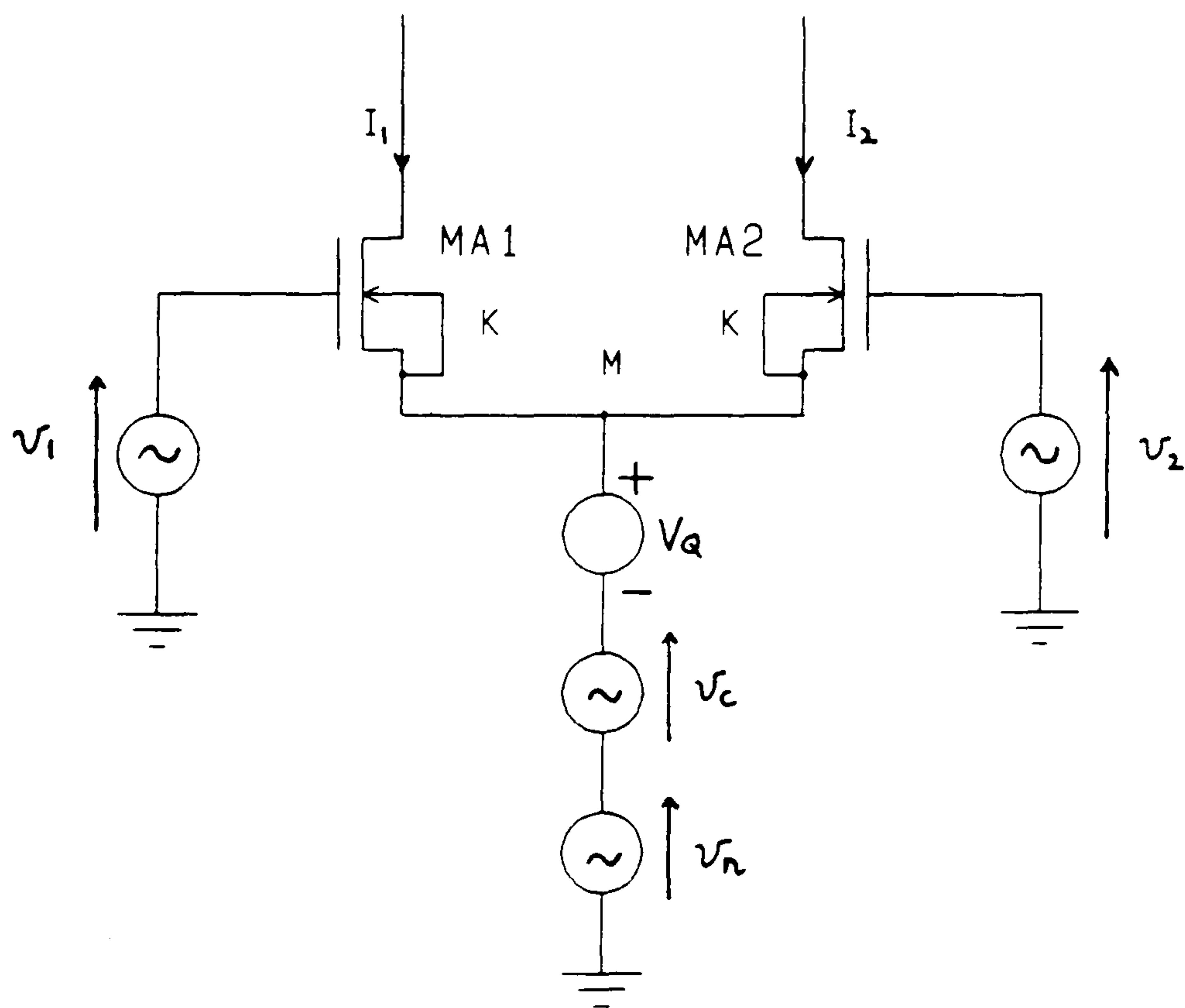


Figure 4.2: The differential pair under equivalent voltage-source excitation

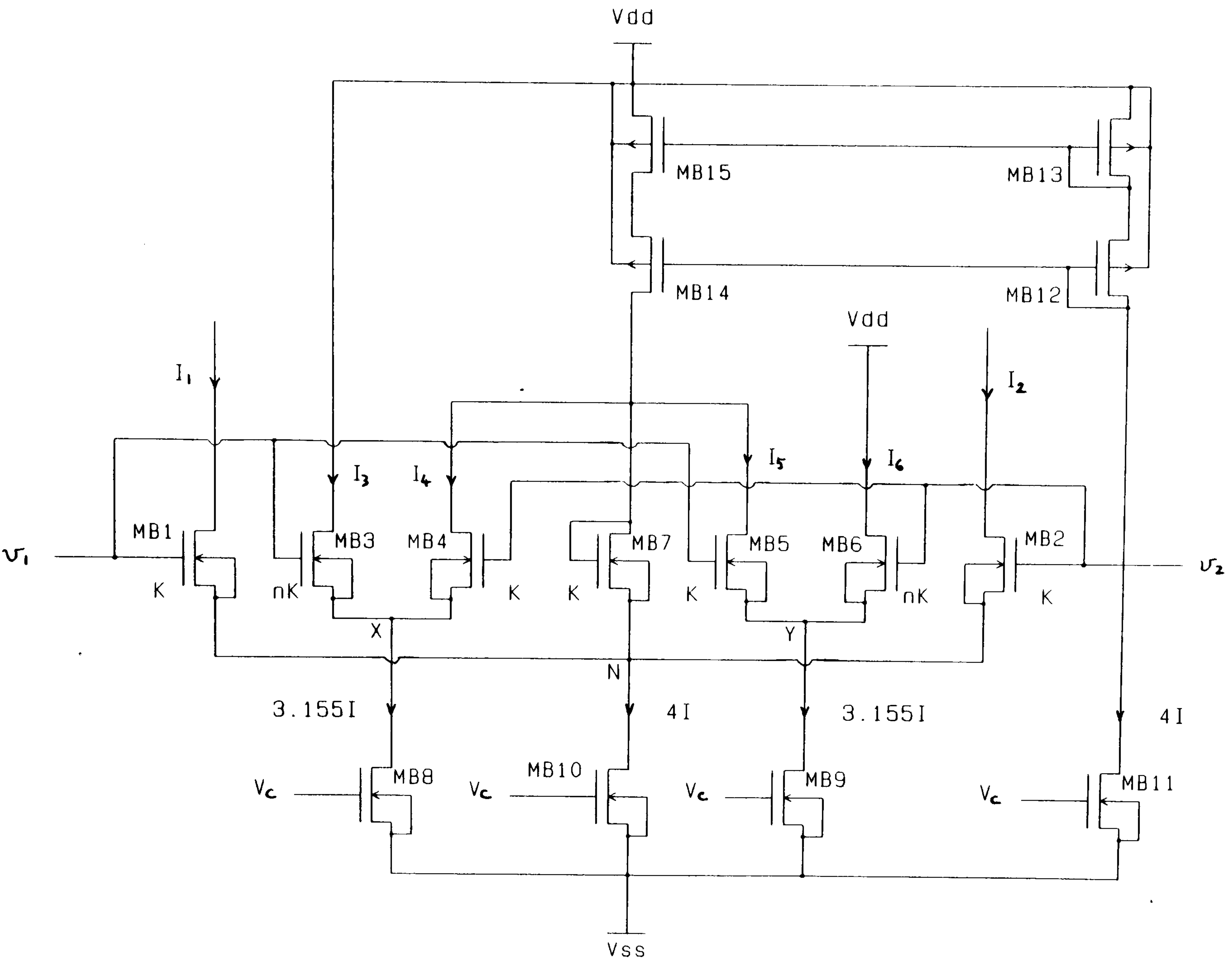


Figure 4.3: Compensated common-source pair transconductor

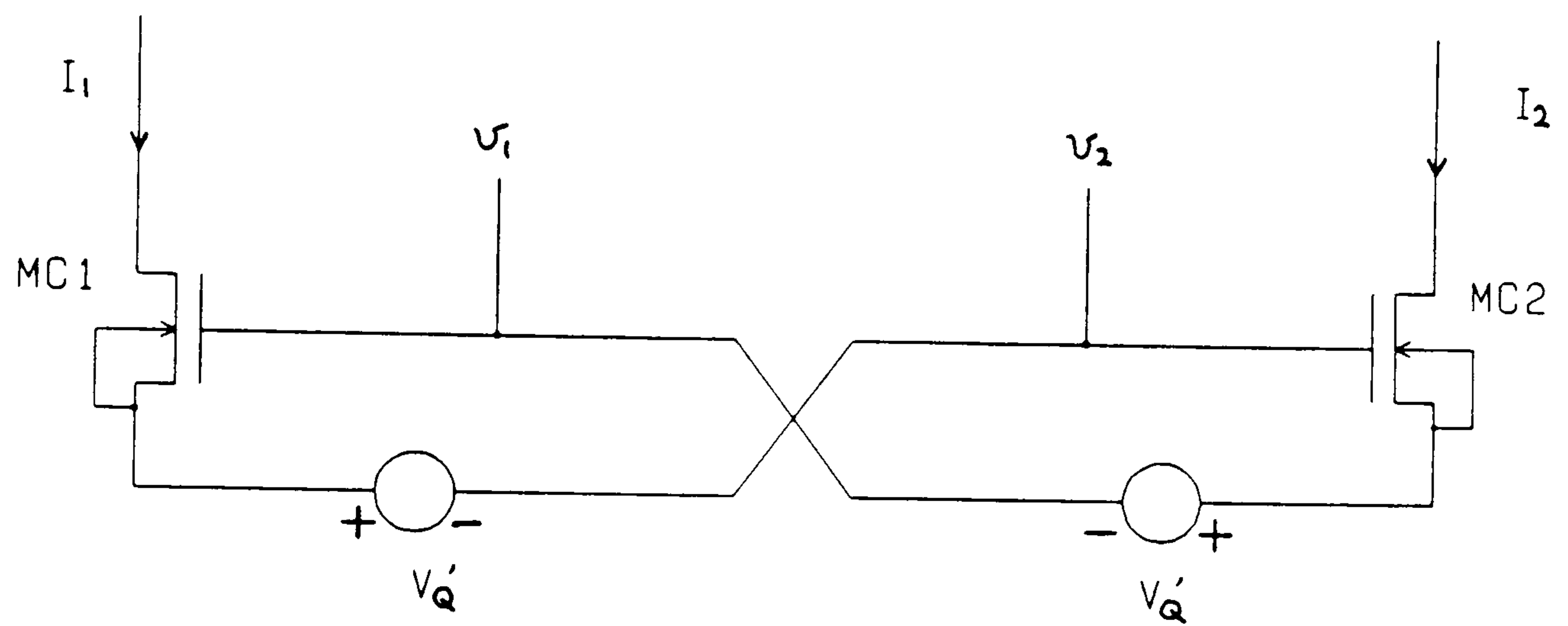


Figure 4.4: Cross-coupled pair scheme

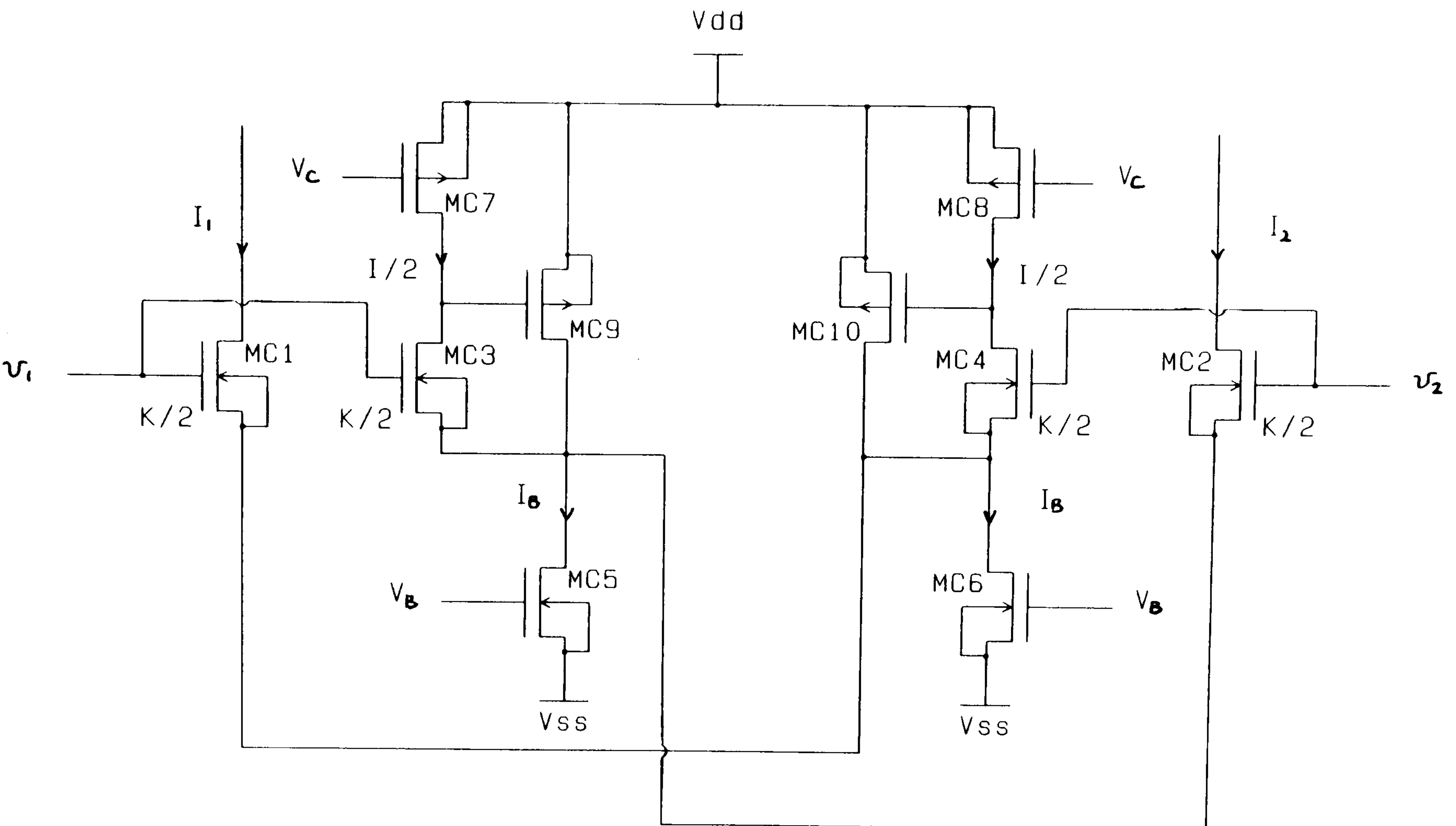


Figure 4.5: Cross-coupled pair transconductor

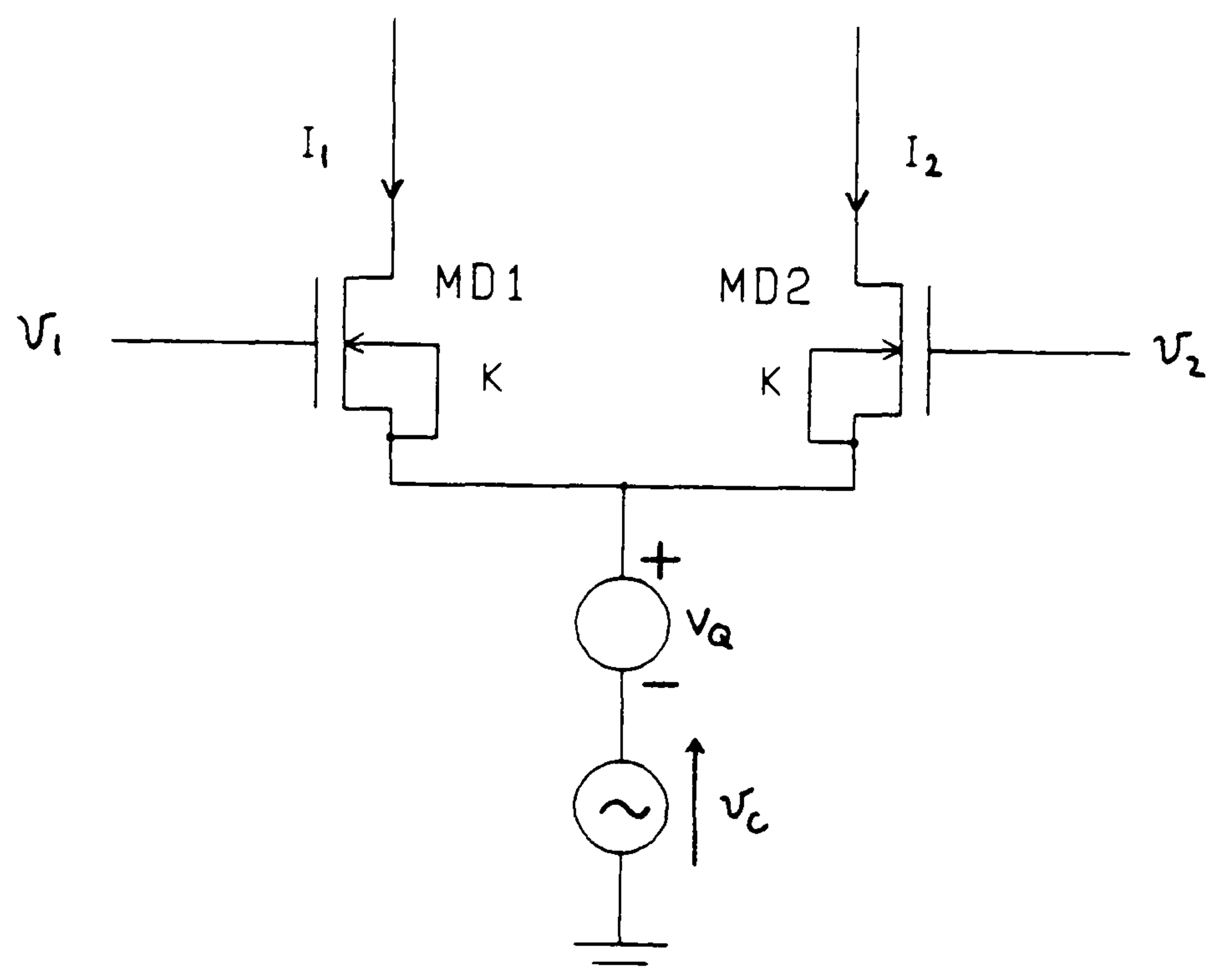


Figure 4.6: Proposed anti-phase common-source pair scheme

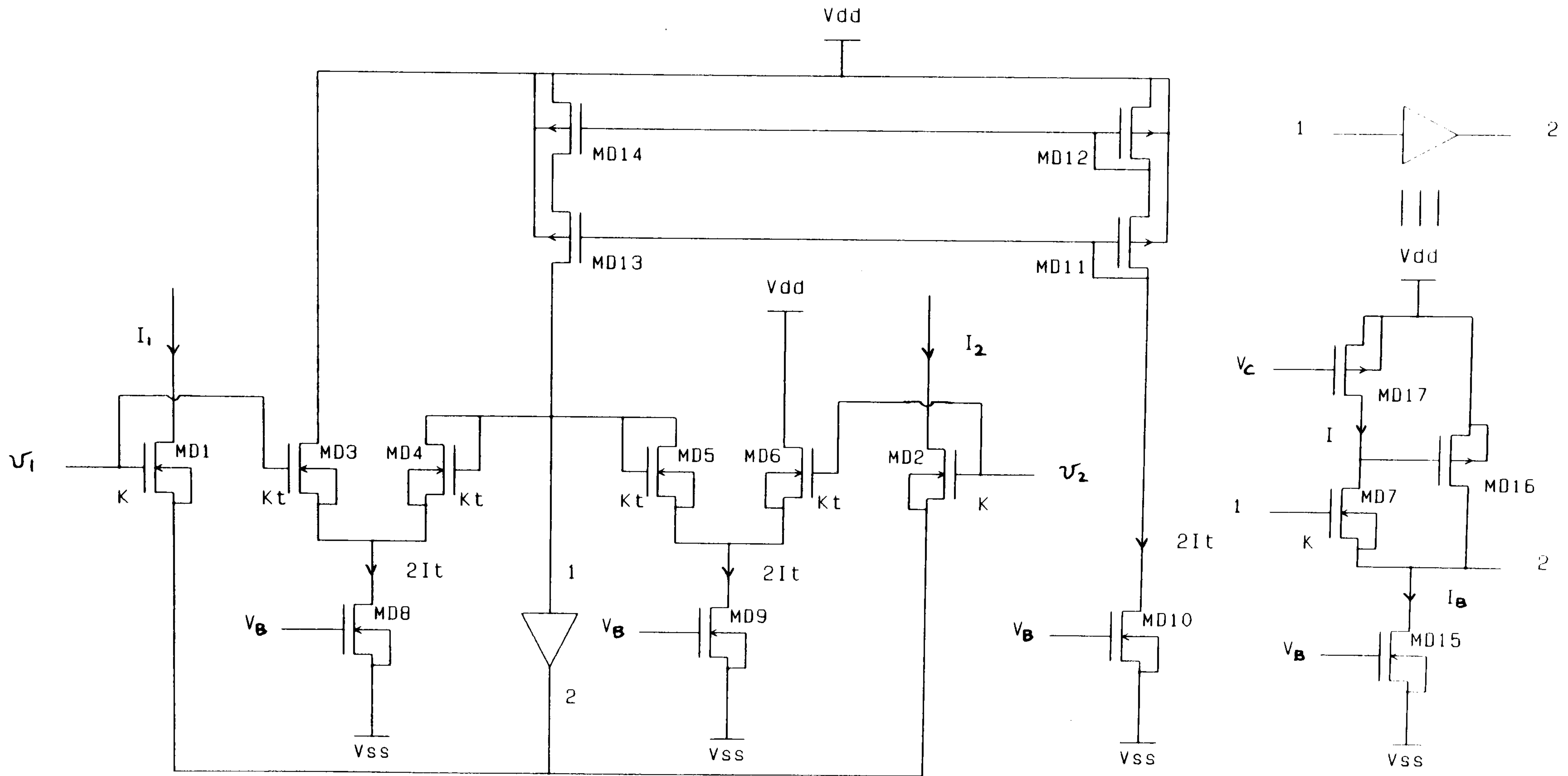


figure 4.7: Anti-phase common-source pair transconductor

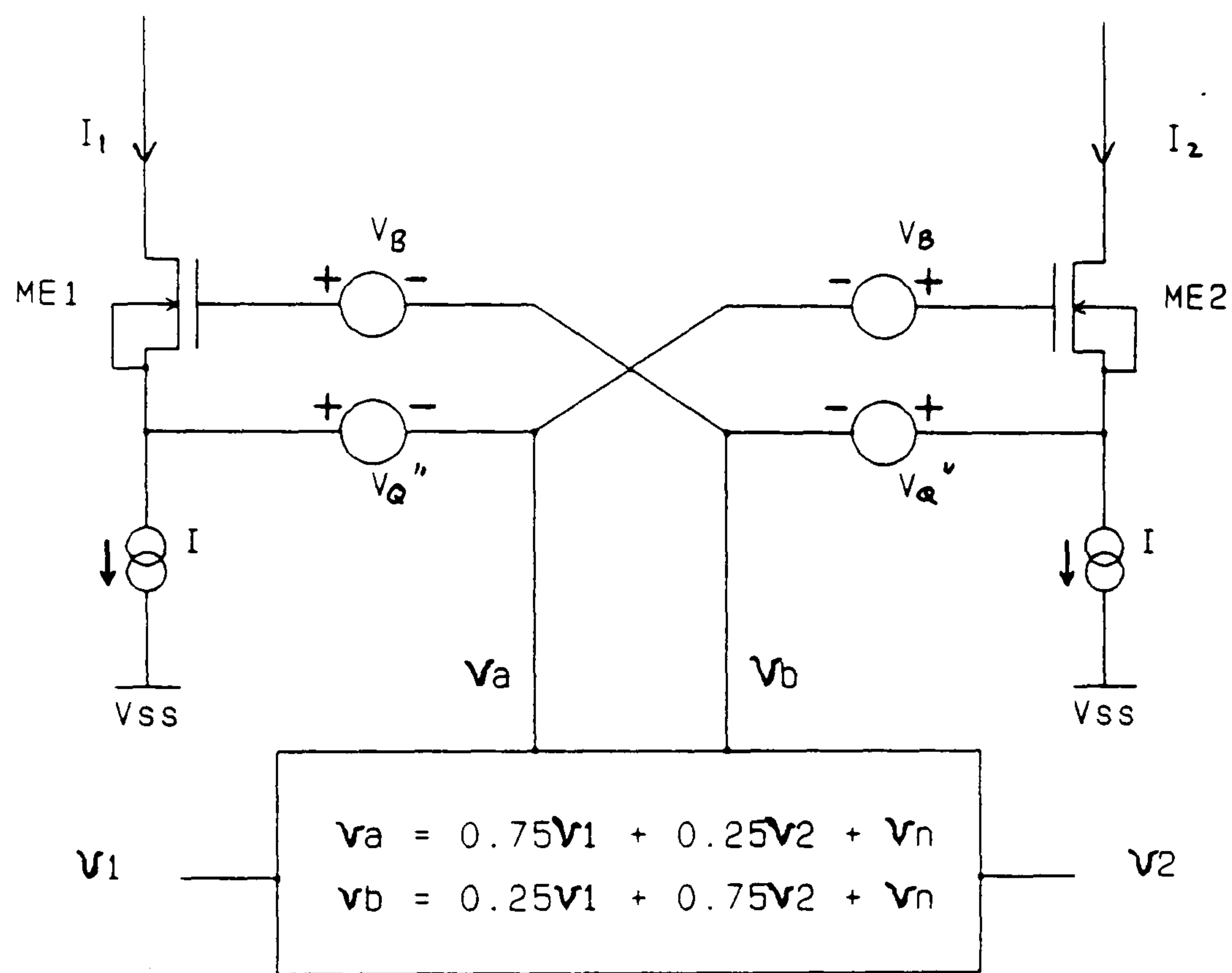


Figure 4.8: Proposed offset-biased cross-coupled pair scheme

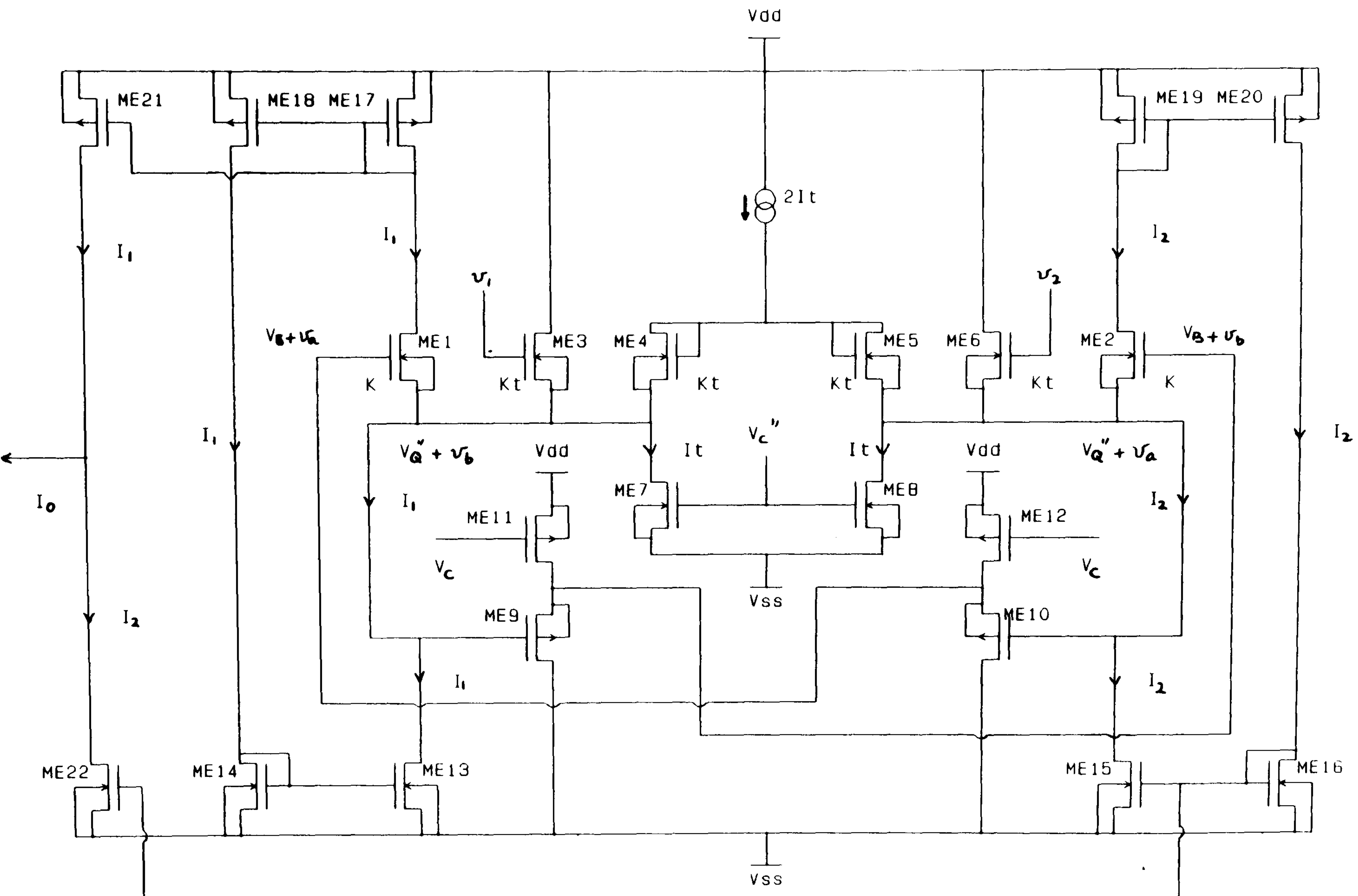


Figure 4.9: Implementation of offset-biased cross-coupled pair transconductor

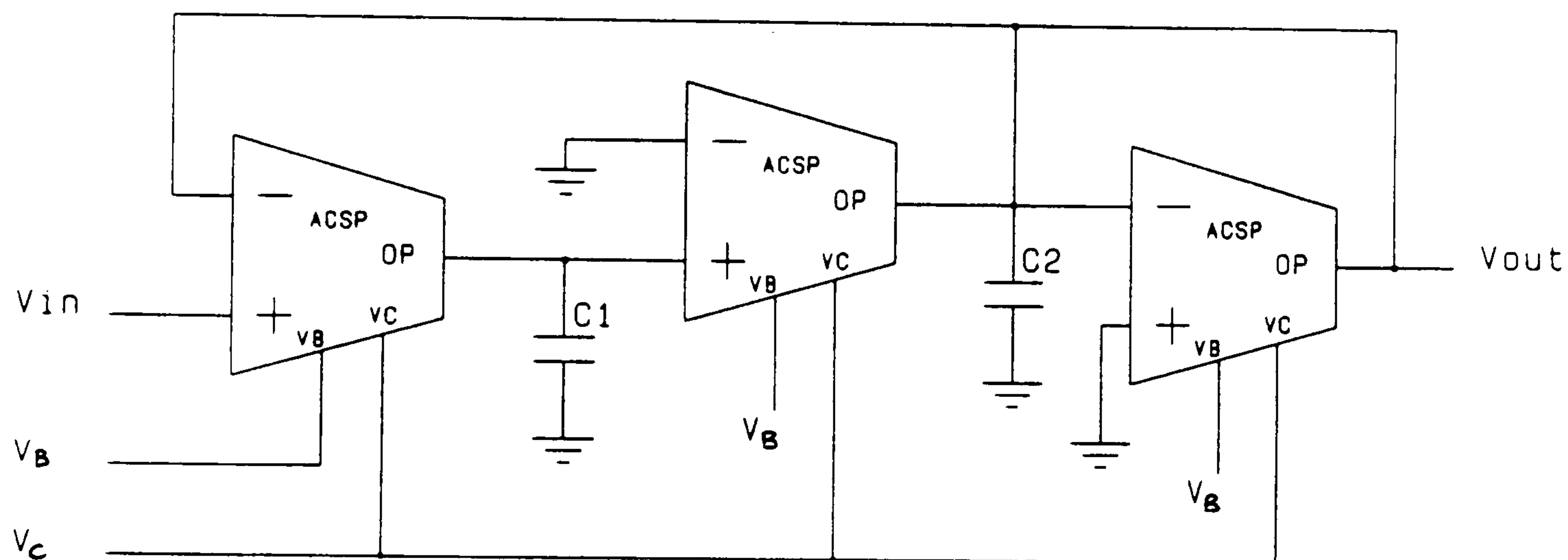


Figure 4.10: Second-order transconductor-C lowpass filter

Chapter 5

Performance Comparison of MOS Transconductor Circuits

5.1 Simulation Results

5.1.1 Linearisation of LTP

It has been shown in Chapter 4 that linearisation of the LTP can be economically achieved by means of employing process with high mobility factor at the expense of reduced transconductance. In addition, the relationship between the third-harmonic distortion and effective transconductance with the mobility factor has been discussed. The objective of this section is to investigate how large a mobility factor is needed to linearise the LTP and to compare results from a series of SPICE simulations with the theoretical predictions.

With reference to the schematic diagram of Fig. 4.1 and the Eqns (K.3), (K.14) and (K.15), they are given as

$$V_b = V_{GS} - V_{TO} = \frac{\theta I}{2K_{oc}} + \sqrt{\frac{I}{K_{oc}}(1 + \frac{\theta^2 I}{4K_{oc}})}, \tag{5.1}$$

$$G_1 = \frac{(2+\theta V_b)}{(1+\theta V_b)^2} K_{oc} V_b, \tag{5.2}$$

and

$$G_3 = -\frac{1+(1+\theta V_b)^2}{(2+\theta V_b)(1+\theta V_b)^4} \frac{K_{oc}}{4V_b} \tag{5.3}$$

The influence of θ on V_b, G_1 and G_3 (normalised with respect to their $\theta = 0$ values) is plotted in Fig. 5.1 for $I = 25\mu A/V^2$ and $K_{oc} = 8.53\mu A/V^2$. The value of the zero-gate-field transconductance parameters K_{oc}, which is defined in Appendix A, is obtained by assuming the transistor pair has an aspect ratio of $10\mu m/30\mu m$ and the process parameters defined in Appendix B. It is particularly noteworthy that over the range $0 < \theta \leq 0.25$, V_b increases by around 26%, whereas the linear transconductance falls by 35%. The G_3 coefficient, on the other hand, reduces by a factor of 6! Thus, the third-haramonic distortion coefficient changes more rapidly than the linear transconductance coefficient.

A series of SPICE simulations using Level-3 device models have been made and the validity of the equivalent voltage source model adopted in the analysis has been established. Simulation predictions for the transconductance coefficient G_1 are shown superimposed on the computed result in Fig. 5.1 and demonstrate a remarkable concurrence.

In the estimation of the third-harmonic distortion, the new equation $(K.18)$ and the standard equation $(K.17)$ are used to compare the accuracy. They are given as

$$HD3 = \frac{1+\frac{1}{(1+\theta \mathrm{V_b})^2}}{(2+\theta \mathrm{V_b})^2}[\frac{V_p}{4V_b}]^2 \times 100\% \tag{5.4}$$

and

$$HD3 = \frac{K_o}{32I} V_p^2 \times 100\% \tag{5.5}$$

The variation of third-harmonic distortion as a function of the quiescent drain current is illustrated in Fig. 5.2. This shows the estimates given by SPICE together

with those from Eqns (5.4) and (5.5) for three values of the mobility degradation factor. Although Eqn (5.5) indicates a reduction of distortion with increasing bias current, the constant-mobility assumption produces results which are significantly pessimistic and therefore unreliable for design purposes. In contrast, however, the distortion estimates from Eqn (5.4) are reliable provided that the differential-pair elements are not driven into cutoff and the current mirror/sink devices remain in saturation.

It can be noted that at higher bias-current levels the computed distortion results are marginally pessimistic. This discrepancy is largely due to the exclusion of the velocity-saturation effect and channel-length modulation from the analysis. However, as Fig. 5.2 suggests, these effects are small, and Eqn (5.4) should prove sufficiently accurate for long-channel devices.

The observation that distortion reduces as mobility degradation increases is at variance with the behaviour of some other linearised saturation-mode transconductors [55]→[56], [59]→[74] for which distortion increases with the mobility reduction factor. This raises the interesting question as to whether differential-pair-based transconductors can be designed with acceptable distortion without resorting to linearisation. The simulation studies have shown that linearity can be improved some $10dB$ or more by employing processes with higher θ levels together with an appropriate choice of bias current and aspect ratios.

Although mobility factor is a technology-dependent constant and cannot be modified by the circuit designer, where several process options are available, the simplicity and low power consumption of the differential pair could make it an attractive candidate for a siiicon-efficient transconductor design.

5.1.2 Linearised Transconductors

The operating principles of the various transconductors have been described in Chapter 4. In this section, the signal-distortion levels of the different circuits are compared in the presence of second-order effects such as mobility degradation and geometrical mismatches. The problems of tuning are examined and the major factors which affect the tuning characteristic of the transconductors are identified. The power consumption for each case is also compared.

All the transconductor outputs (except the OBCCP which has a different architecture) are connected to identical differential-to-single-ended current converters (employing the double-cascode mirror arrangement [61]) as illustrated in Fig. 5.3. The comparison is made on the basis that for all structures, the transconductances are equal, the power supplies are common, and the transistors are sufficiently long to exclude channel-length modulation effect.

Table 5.1 shows the device aspect ratios employed for the transconductors in Fig. 4.1, 4.5, 4.7 and Fig. 4.9. The aspect ratios for the cascode mirror transistors (not shown in Fig. 4.1,4.3,4.5 and 4.7) are $140\mu m/10\mu m$. The device models used are those specified in Appendix B.

Fig. 5.4→5.8 show the family of static characteristics obtained for each of the five transconductors at appropriate control voltage levels. It can be observed that all offer different degrees of tuning capability. The tuning characteristic can be assessed by plotting distortion against the variation of transconductance for a given input signal level. This relationship is fully illustrated in both Fig. 5.9 and Fig. 5.10. The tunability of each transconductor and the trend of the THD curves will be deferred for later discussion.

In order to provide an assessment of the relative linearity for the group of

transconductors, their simulated transfer characteristics (for a nominal transconductance of $26\mu A/V$) are shown collectively in Fig. 5.11. It can be seen that although the CCSP has the largest linear range for positive excursions, nonlinearity occurs for relatively small negative swings. By contrast, the wide linear range for both the ACSP and OBCCP extends to both quadrants.

The variation of THD as a function of different input voltages is shown in Fig. 5.12. It can be observed that, for low signal levels, the THD for CCSP, ACSP and OBCCP are similar as predicted by the mobility degradation analysis of Appendices L and N. However, for larger signals, the CCSP-controlled transistors are driven into the ohmic region of operation, resulting in a sharp departure from linearity. The signal-handling capabilities of the ACSP and OBCCP are not similarly degraded and linearity is maintained over a wide range of input voltage. The principal reasons will be discussed later. In the case of the CCP, the effect of a high mobility degradation results in a generally inferior performance. Since the mobility degradation factor employed is up to 0.15, it produces a distortion performance similar to that of the LTP. For some quiescent bias conditions (see Fig. 5.9-5.10) the LTP even offers lower distortion level than the CCP. Thus, as previously noted, a pronounced mobility degradation effect has the advantage of lowering nonlinearity in the LTP but increasing the nonlinearity in other transconductors. It is clear that low distortion levels are critically dependent on the extent of mobility degradation effect. In order to confirm the SPICE simulation results, a comparison has been made with the results predicted by the analytical expressions (see Appendices K to N) as shown in Fig. 5.13. The simulated curves demonstrate a remarkable agreement with the theoretical results.

Although mobility effects in the CCSP are the same for both the ACSP and

OBCCP, this may not be valid under all conditions of operation. Discrepancies occur in the THD curves for the CCSP shown in Fig. 5.9 and Fig. 5.10. In order to explain the phenomenon, the circuit (Fig. 4.3) of the CCSP is examined, As the circuit is simulated by assuming $v_1 = V_{in}$ and $v_2 = 0$, the first-order approximation shows that $v_X \geq v_N \geq v_Y$ using the Eqns (4.17), (4.23) and (4.24) for $n = 2.155$ [60]. As a consequence, the transistor MB4 tends to cut off earlier than MB2 due to a larger signal swing in the source node of the auxiliary differential pair MB3-MB4. Thus, the signal v_N is no longer a common-mode signal, and transistor MB4 is driven into the cut-off region. However, some degree of current compensation still occurs due to the auxiliary differential pair MB5-MB6. This explains why some portion of the CCSP distortion curve is less sensitive to bias current.

In addition to the mobility degradation effect, other second-order effects can be of significance. Since the length of the input devices was chosen to be greater than $10\mu m$ and the body terminals were tied to the respective source terminals, the effects of channel-length modulation and body effect have been minimised. Mismatch remains one of the important factors affecting the overall distortion of the transconductors.

The variation of THD with transconductance is plotted in Fig. 5.14 and Fig. 5.15 for $\pm 2\%$ worst-case mismatching in each transconductor. Table 5.2 summarises the relative figures. It can be observed that the LTP offers the lowest level of mismatch sensitivity because even-order harmonic distortion are only generated from mismatch in the differential-pair transistors. Mismatch in the mirror pairs does not contribute to even-order distortion, but only produces a dc offset. However, other transconductors rely on precise current-mirror pairs to subtract the even-order components. As the number of mirror pairs increases, the sensitivity is

increased. Since more mirror transistors are employed in the OBCCP structure, it therefore suffers the highest sensitivity figure. Although the CCP has a greater dependence on the mobility degradation effect by comparison with the ACSP and CCSP, it is however rather insensitve to mismatch. This is largely due to the insensitivity of the shunt-feedback buffers (see Fig. 4.5). The ACSP and CCSP, on the other hand, exhibit similar sensitivity as a result of a comparable number of components. As can be inferred from Fig. 5.9 and 5.10 as well as Fig. 5.14 and Fig. 5.15, mismatch in the CCSP raises the distortion levels which mask the minute distortion details under low bias conditions. Thus, the ACSP has better linearity performance than the CCSP under mismatch situation.

With reference to Table 5.2, the distortion caused by the mobility degradation effect is not as significant as the mismatch effect in the ACSP, CCSP and OBCCP. at low signal level ($1V_{pp}$). This is based on the observation of the difference in THD figures between mismatch and no-mismatch. However, The LTP produces better distortion performance than the CCP, CCSP and OBCCP due to its insensitivity to mismatch. Under larger signal drives ($2.5V_{pp}$), the cubic nonlinearity of the LTP increases more rapidly than the mobility-related distortion products of the ACSP. The linearity of the CCP, on the other hand, is degraded by the strong mobility effect. Even though the CCSP has similar mobility degradation level and mismatch sensitivity in comparison with the ACSP, it performs less well than the ACSP because of the saturation constraint of the current-sink devices. The distortion of the OBCCP, on the other hand, is degraded significantly by the mismatch effect, causing higher distortion level compared with other transconductors. The gives ACSP the best distortion performance amongst this group of transconductors.

Apart from the linearity problems due to second-order effects, a major problem in transconductor design is to guarantee reasonable signal-handling capability when the transconductance is tuned by an on-chip automatic system. There are several factors limiting the tunability of a transconductor; they are the constraint that the current source/sink must remain in saturation, the architecture, supply voltages and signal level. For saturation-mode convertors, the maximum value of input signal is governed by the constraint that all the transistors must operate in their saturation region. Transconductors with stacked structures [55]-[56],[62],[66],[71]-[73] typically exhibit poor tunability. Although the saturation requirement can be relaxed by an increasing supply voltages and/or decreasing input signal levels, this is not a cost-effective solution for applications requiring low-supply operation and large signal-handling capability.

With reference to the tuning-range figure in Table 5.2, the ACSP offers a superior tuning performance in comparison with the LTP, CCP and CCSP. This is mainly because the cubic nonlinearity in the LTP is degraded significantly with changes in bias and the increase of signal levels. Since the sourcing/sinking current in the ACSP is stabilised via negative feedback in the buffer, it can accommodate a higher common-mode signal swing than that in the CCSP. In the case of the ACSP transconductor, despite the higher mismatch sensitivity, it has a lower mobility degradation and offers an extended signal-handling capability. This can be explained by examining the operation of the respective buffer. As the summing currents $I_1 + I_2$ are combined into the output node of the buffer in the ACSP, they tend to cancel each other because I_1 is in anti-phase with I_2. This leads to very small voltage swings at the drain of transistor MD17 even under large signal drives. However, no partial cancellation occurs in the CCP as currents I_1 and I_2 flow into

the corresponding buffers. Under these circumstances, transistors MC7 and MC8 cannot be maintained in saturation for large input signals. The insensitivity of the ACSP to these problems is largely reponsible for its superior performance. In comparison with the OBCCP, the ACSP has a narrower tuning range but it maintains a better distortion performance. The superior tuning performance of the OBCCP arises from the fact that the bias voltage of differential-pair transistors is shifted far beyond the saturation limit of the current-controlled transistors. However, the architecture is subject to a higher distortion figure due to its sensitivity to mismatch. Thus, the level of distortion degradation with tuning depends on a combination of non-ideal effects.

It is also important to note that a performance limitation occurs with both the ACSP and OBCCP due to cut-off in the AC common-mode generator differential pairs. Since the DC bias voltage is fixed, they can support a large input signal before cut-off occurs. Optimisation of the factor $\sqrt{\frac{I_t}{K_t}}$ in the differential pair may be neccessary so as to achieve maximum signal handling capability, and a consequential improvement in tunability.

The simplicity of the LTP gives the lowest power comsumption. The CCP, on the other hand, offers a reasonably low power consumption based on its high transconductance efficiency. As expected, both the ACSP and CCSP incur a higher power consumption due to their complexity. However, it is interesting to note that the power dissipation of the OBCCP is lower than those of the ACSP and CCSP despite its higher complexity. The principal reason lies in the Class-AB operation of the current-loop voltage sources. This is in sharp contrast with the ACSP which relies on a Class-A shunt-feedback buffer to achieve coupling as well as sourcing/sinking currents. Although the ACSP shunt-feedback buffer can be

replaced by a simple source follower plus current-loop voltage source, the price paid for the reduction in power consumption is an increase in mismatch sensitivity and silicon area as more mirror transistors are required in the design.

It may be concluded that not only are the distortion and tuning performance of a linearised transconductor dependent on the mobility degradation and mismatching, but the saturation constraint in current-controlled devices is also an important factor lowering the linearity and tunability. For large-signal tunable applications, the ACSP and OBCCP are the appropriate choices in view of their superior tuning capability and low distortion levels. However, the application of complex linearisation techniques to transconductor design does demand higher power consumption and silicon area. For low-signal applications, a simple linearised LTP which can exploit a strong mobility effect for effective source degeneration may prove attractive, particularly in terms of silicon efficiency, sensitivity to second-order effects and power consumption.

5.1.3 MOS Transconductor-C Filter Example

Simulation results are now presented for an ACSP-based transconductor-C filter having a Chebyshev lowpass function with $0.5dB$ passband ripple. The performance assessment deals with tunability, distortion levels and signal-handling capability.

The fundamental components for the synthesis of a transconductor filter have been illustrated in the circuit diagram of Fig. 4.10. It may be recalled that the capacitor values together with the aspect ratio for the ACSP transistors are given in Section 4.7 and Table 5.1, respectively. The models adopted correspond to the Plessey $2\mu m$ process detailed in Appendix B and the supply voltages were set at

$\pm 5V$.

As shown in Fig. 5.16, the $3dB$ cut-off frequency of the filter was varied from $2.66KHz$ to $6.82KHz$; a tuning ratio of 2.6. It can be seen that the stopband attenuation is better than $75dB$ over the indicated tuning range. In Fig. 5.17, the simulated cut-off frequency is compared with the ideal case at $4.7KHz$. It conforms excellently with the theoretical expectation up to $100KHz$. The THD curves based on the input frequencies being one-third of the cut-off frequencies are depicted in Fig. 5.18. These curves indicate that THD depends on the cut-off frequency which in turn is controlled by the bias. In general, higher bias levels lower the THD. These results also reveal that a worst-case $3V_{pp}$ signal was supported over a tuning ratio of 2.6. It may be noted that this ratio is larger than the value of 2.2 obtained for the GVCR based filter. This highlights the improved tunability performance of the ACSP structure.

5.2 Experimental Results

5.2.1 Layout Techniques

The LTP and ACSP have been fabricated in the Plessey twin-well $1\mu m$ CMOS technology. Fig. 5.19 shows the microphotograph of both transconductors. Their transistor aspect ratios are given in Table 5.3. It should be noted that all the mirror pairs for the bias network and the output current converter are based on simple current mirrors with aspect ratios of $140\mu m/10\mu m$. The estimated silicon area for the LTP and ACSP is $0.36\times10^5\mu m^2$ and $1.16\times10^5\mu m^2$, respectively. Since mismatch would have a significant effect on the linearity of the ACSP and other transconductors, attention has been placed on layout techniques. The layout

adopts traditional methods for the larger devices (with minimum $10\mu m$ for channel length and width in this layout example) and places matched devices close to each other so as to improve matching. In addition, a common-centroid [2] technique was employed, in which devices to be matched were split into two sub-devices and connected in parallel around a central point so as to eliminate the effect of gradient in process parameter and temperature. These strategies were also applied to the match-sensitive devices: differential-pair transistors and mirror transistors. Finally, electrical protection of the transconductors was accomplished via the Plessey ESD cells described previously.

5.2.2 LTP and ACSP Transconductors

The distortion for both the LTP and ACSP transconductors was measured using $\pm 2.5V$ supplies with the experimental set-up in Fig. 5.20. As shown in the figure, the feedback passive resistor $R(120K\Omega)$ and operational amplifier ($TL072$) forms a current-to-voltage converter. The THD was measured by examining the output of the amplifier with an HP distortion analyser HP339A. Since the amplifier exhibits less than $-80dB$ (with the $v\sim i$ converter replaced by a conventional passive resistor), the non-linearity was mainly due to the non-ideal transconductor.

By fixing the magnitude of the input signal and tuning the control voltage of each transconductor, different distortion figures with respect to the corresponding transconductance values were obtained and shown in Fig. 5.20. At $0.5V_{pp}$, the THD for the ACSP stays below $-56dB$. However, the LTP did not achieve comparable results, the major reason being that the mobility degradation factor in this case (Appendix C) is only 0.05. This low value not only reduces the odd-order mobility-related products of the ACSP but increases the cubic non-linearity

in the LTP. As the mobility distortion products tend to be small in the ACSP, the figures obtained are mainly contributed by the mismatch effect at low signal levels. However, experimental evidence shows that even under mismatch conditions associated with the errors in the fabrication process, the ACSP exhibits a significantly better THD performance than that of the LTP.

Replacing the analyser with an oscilloscope, the voltage transfer characteristic can be obtained using the X-Y mode measurement. Fig. 5.22 illustrates the voltage transfer characteristic of the ACSP. The settings for the X and Y mode were 0.2V/div and 2V/div. The resistance R was $120K\Omega$. The three curves which are corresponding to transconductance values of $41\mu A/V$, $72\mu A/V$ and $100\mu A/V$ demonstrate the tunability of the proposed transconductor.

$I - V$ static measurements were conducted at the nominal transconductance of $72\mu A/V$, and the results are depicted in Fig. 5.23. It can be seen that the LTP static characteristic exhibits a symmetrical saturation shape with respect to the polarity of input signal. The ACSP, on the other hand, displays a fairly straight line within $\pm 1V$ range, demonstrating a high degree of linearity. Fig. 5.24 plots the distortion against input signal. For distortion below $-40dB$, the maximum input swing for the LTP and ACSP is $0.6V_{pp}$ and $2V_{pp}$, respectively. Thus, the ACSP has higher signal-handling capability than the LTP.

Having discussed the experimental performance of the LTP and ACSP, the analytical expression for the LTP HD3 is evaluated. Owing to the current-limiting behaviour of the LTP, the bias current (or tail current) can be extracted by applying a large input signal such that one of the transistor in the differential pair is cut-off. Using the current value obtained together with process data in Appendix C and Eqn (K.17), the predicted THD is plotted Fig. 5.25. It can be compared

with the experimental data with the estimation provided by the classical HD3 expression of Eqn (K.18). This prediction closely agrees with the experiment. It excludes the need for complex computation in solving the nonlinear equations in Ref [58]. It also confirms that even-order distortion is small enough to be neglected and the THD is dominated by HD3. This conclusion is based on its insensitivity to the mismatch effect. However, mismatch is critical in the case of the ACSP, since any mismatch in the transistor pairs raises the distortion level. This has been predicted by the simulation results in Fig. 5.14 and Fig. 5.15. Thus, the HD3 expression derived in Eqn (L.14), which takes account of mobility degradation effect, is only valid when the mismatch has been minimised by careful attention to layout.

Device	*Aspect Ratio* $(\mu m)/(\mu m)$
MA1-MA2	10/30
MA3	50/10
MB1-MB2,MB4-MB5,MB7	10/30
MB3, MB6	21.55/30
MB8-MB9	78.875/10
MB10-MB11	100/10
MB12-MB14	140/10
MC1-MC4	10/60
MC5-MC6	60/10
MC7-MC8	44/10
MC9-MC10	50/10
MD1-MD2,MD7	10/30
MD3-MD6	10/10
MD8-MD10	60/20
MD11-MD14	140/10
MD15	120/10
MD16-MD17	50/10
ME1-ME2, ME9-ME10	10/30
ME3-ME6	10/10
ME7-ME8	60/20
ME11-ME12	50/10
ME13-22	140/10

Table 5.1: Device aspect ratios for the simulated transconductors

$G = 26\mu A/V$	LTP	CCSP	CCP	ACSP	OBCCP
THD(dB) at $1V_{pp}$, no mismatch	-63.22	-71.70	-61.01	-73.15	-73.07
THD(dB) at $1V_{pp}$, 2% mismatch	-62.05	-56.25	-53.35	-58.79	-50.00
Increase of THD(dB) at $1V_{pp}$, 2% mismatch	1.17	15.45	7.66	14.36	23.07
Tuning Range ($\mu A/V$) for THD $\leq$ 1% at $1V_{pp}$, 2% mismatch	18	21	21	25	31
THD(dB) at $2.5V_{pp}$, no mismatch	-46.84	-57.52	-44.75	-57.02	-57.08
THD(dB) at $2.5V_{pp}$, 2% mismatch	-46.50	-47.43	-42.32	-49.34	-41.28
Increase of THD(dB) at $2.5V_{pp}$, 2% mismatch	0.34	10.09	2.43	7.68	15.80
Tuning Range ($\mu A/V$) for THD $\leq$ 1% at $2.5V_{pp}$, 2% mismatch	7	11	4	16	20
Power Consumption (mW)	1.48	6.19	3.23	5.69	4.17

Table 5.2: Performance comparison of OTAs at nominal transconductance $26\mu A/V$

Device	*Aspect Ratio* $(\mu m)/(\mu m)$
MA1-MA2	20/10
MA3	50/10
MD1-MD2,MD7	20/10
MD3-MD6	20/10
MD8-MD10	50/10
MD15	200/10
MD16-MD17	50/10

Table 5.3: Device aspect ratios for the experimental LTP and ACSP transconductors

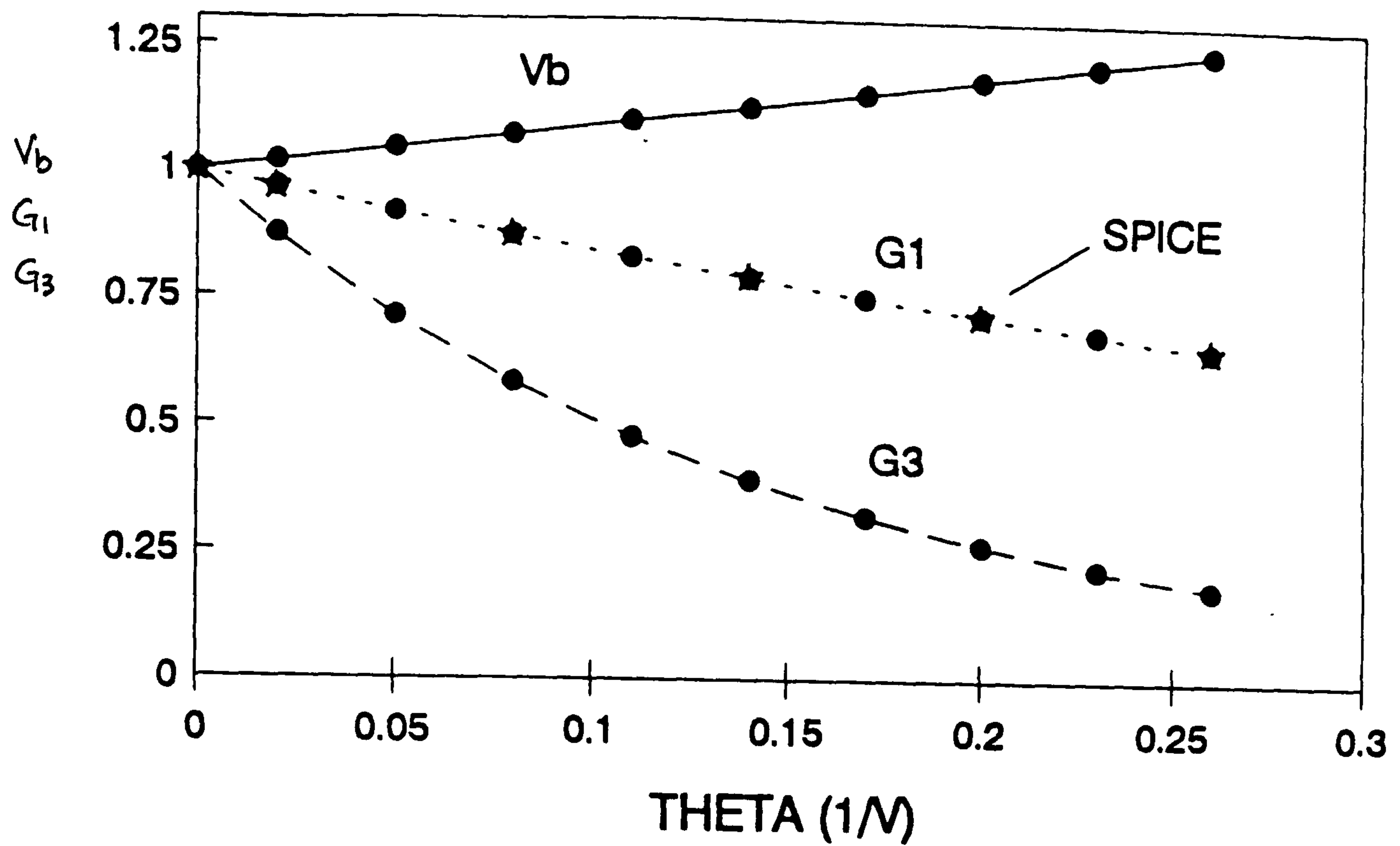


Figure 5.1: Variation of quiescent gate overdrive and transconduction coefficients (normalised with respect to their $\theta = 0$ values) with mobility factor

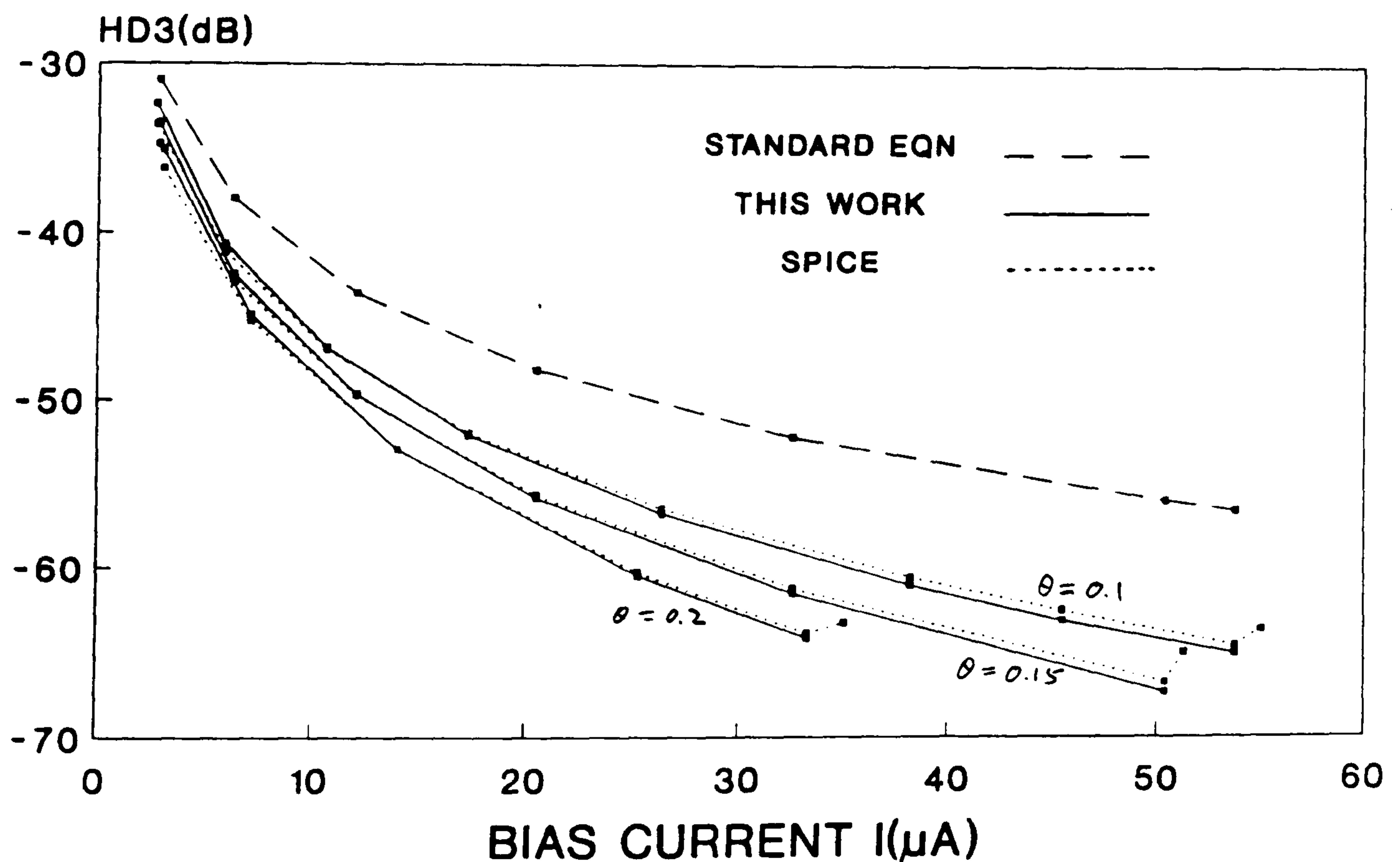


Figure 5.2: Third-harmonic distortion versus input bias current at 1KHz with a $1V_{pp}$ input signal and a $10\mu m/30\mu m$ aspect ratio

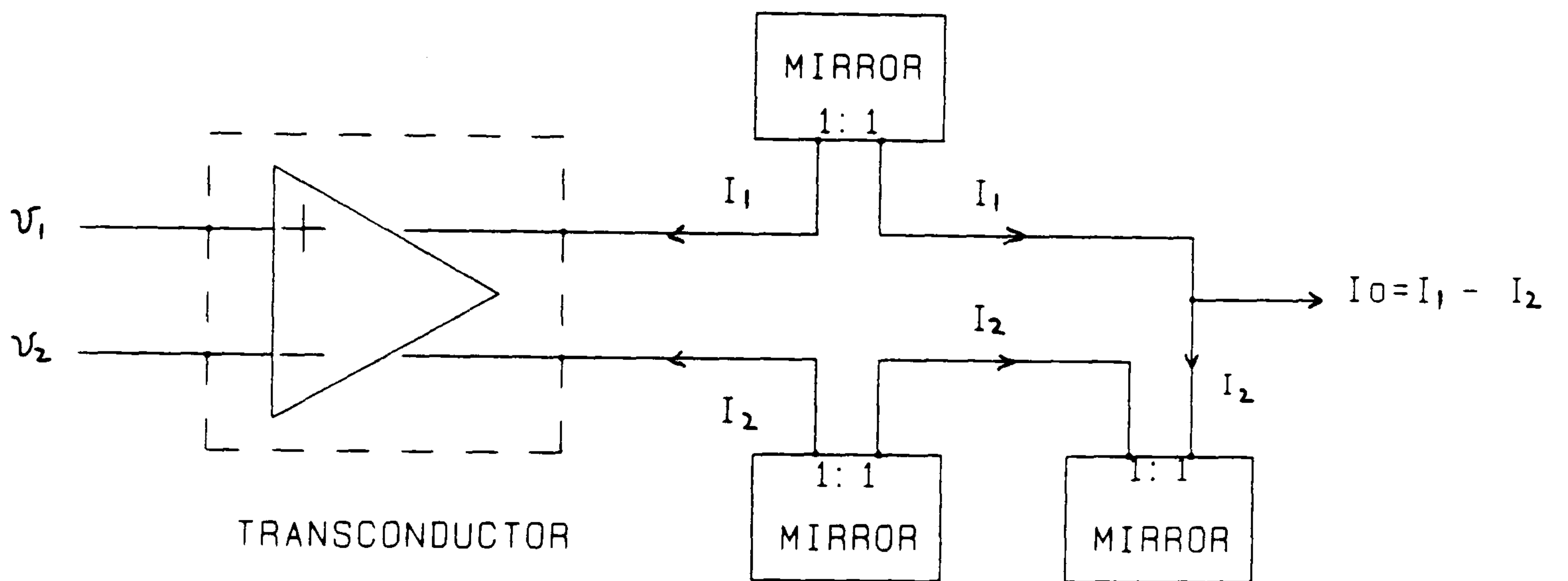


Figure 5.3: Transconductor structure

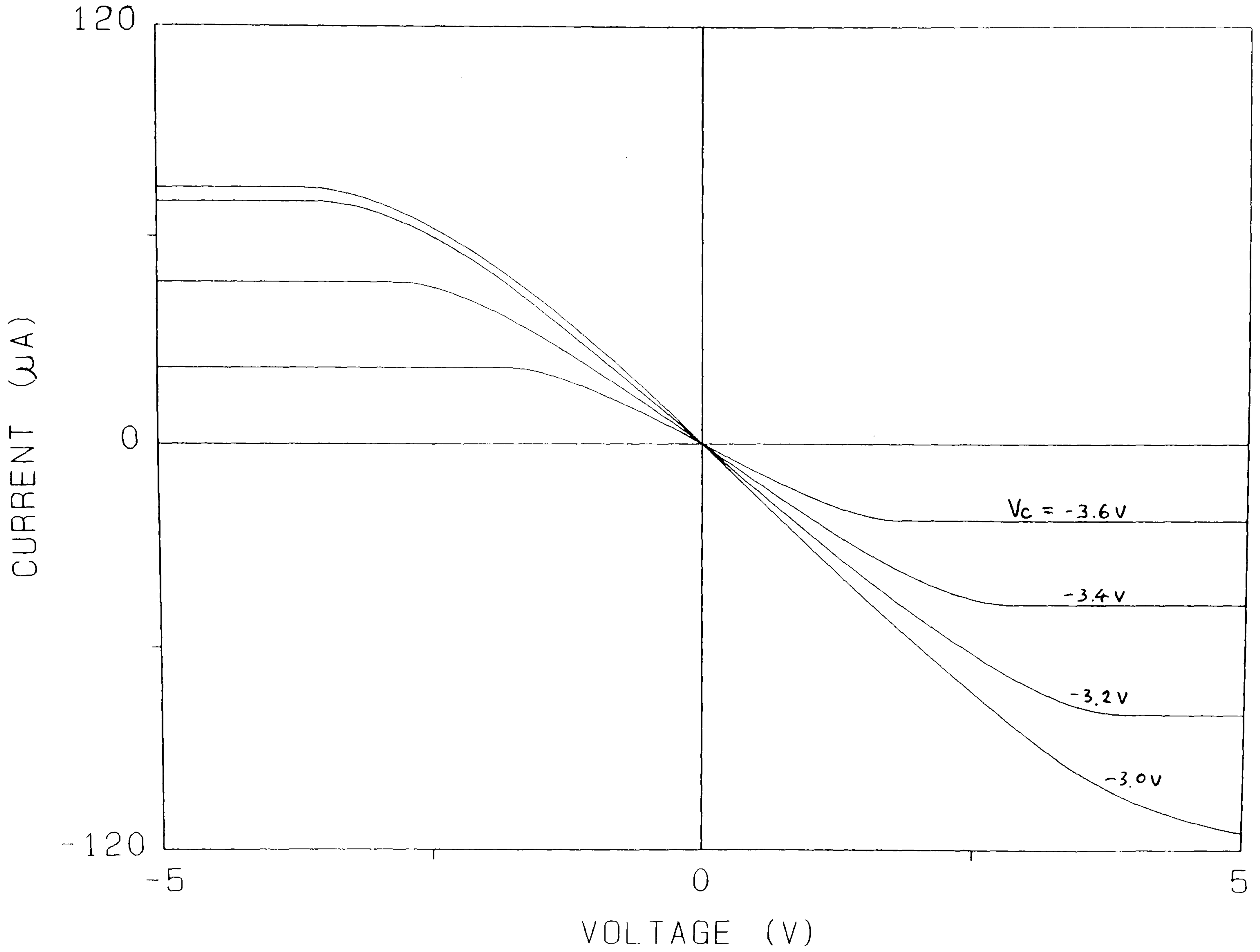


Figure 5.4: Control voltage tuning of static characteristic for LTP transconductor

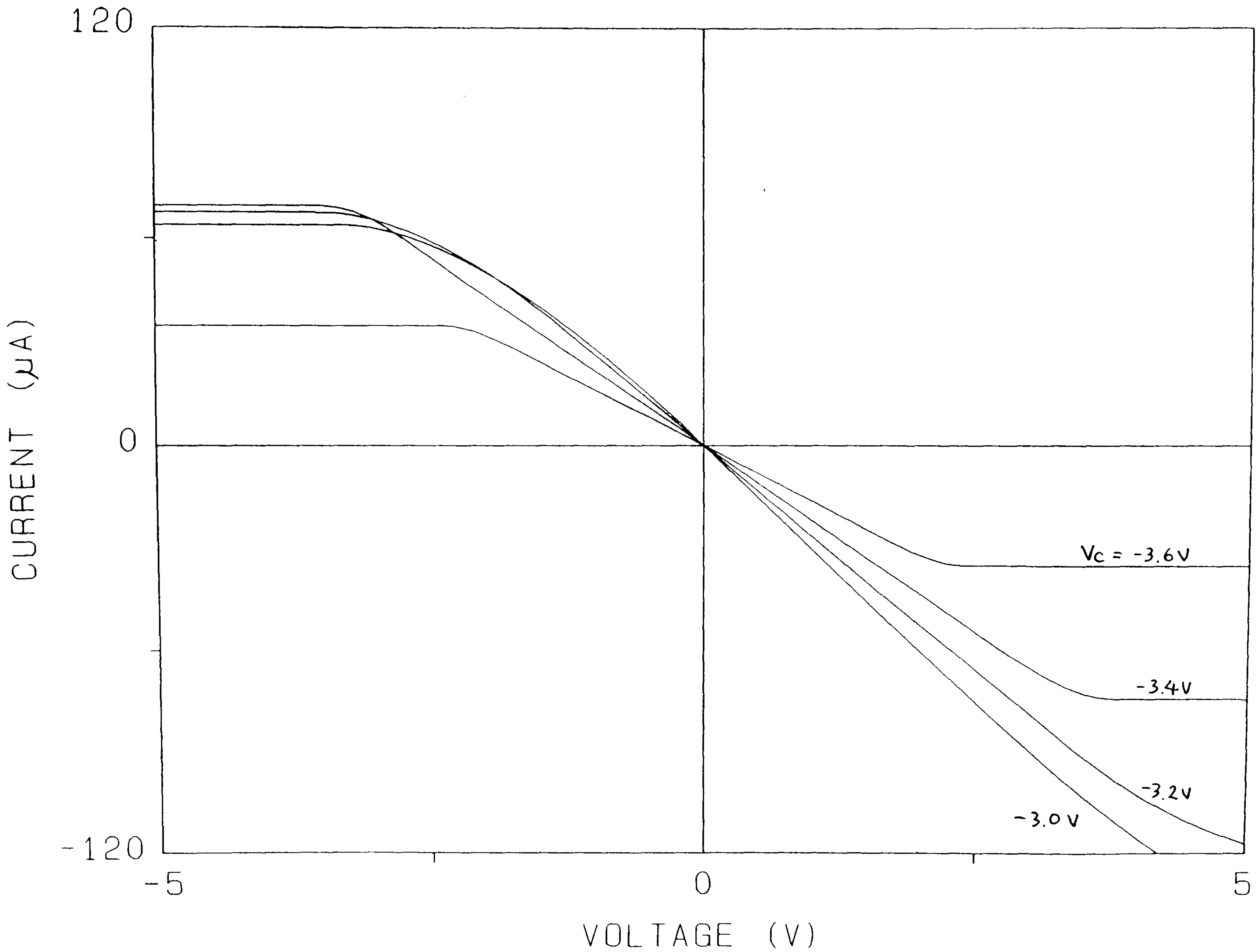


Figure 5.5: Control voltage tuning of static characteristic for CCSP transconductor

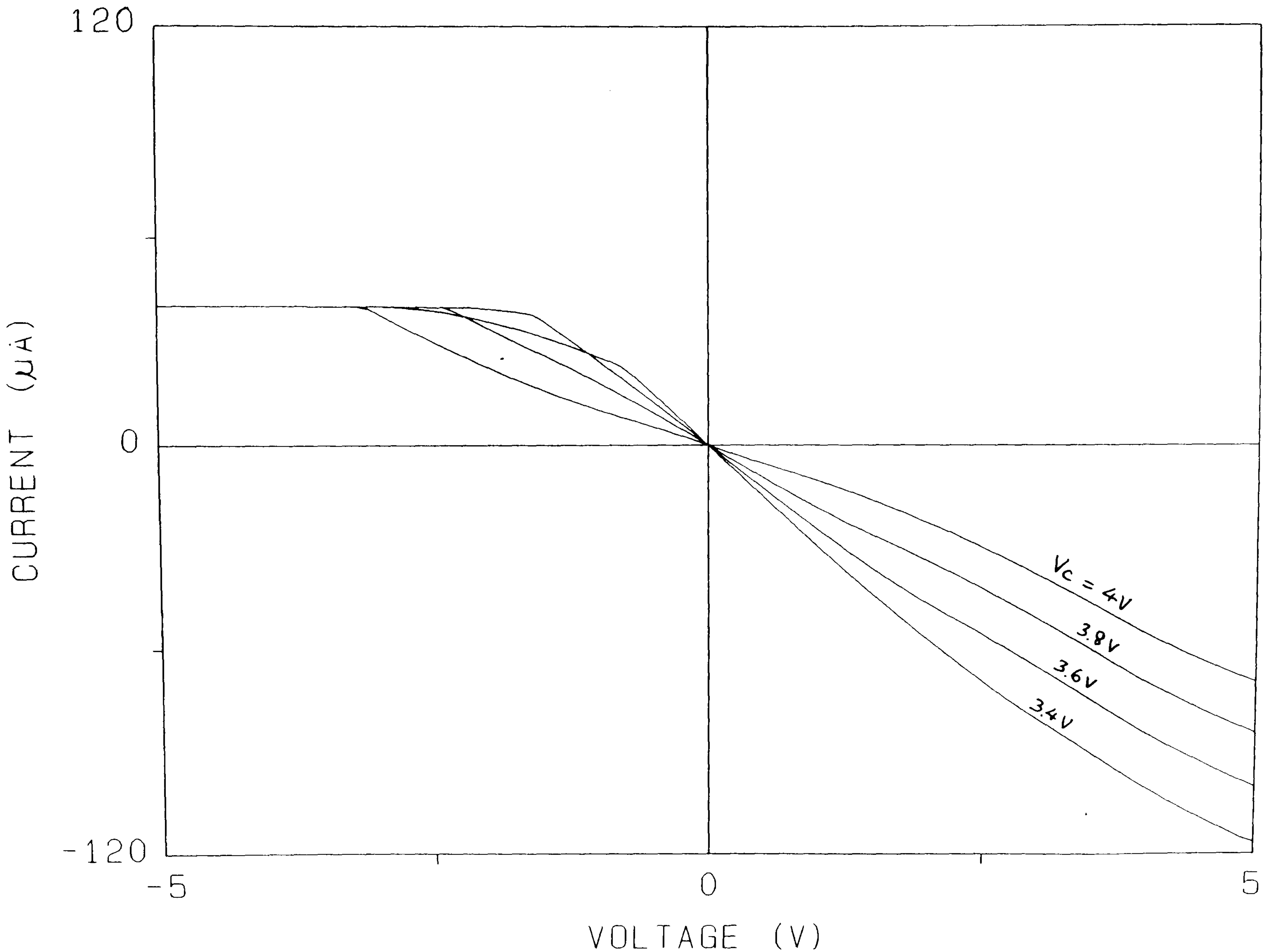


Figure 5.6: Control voltage tuning of static characteristic for CCP transconductor

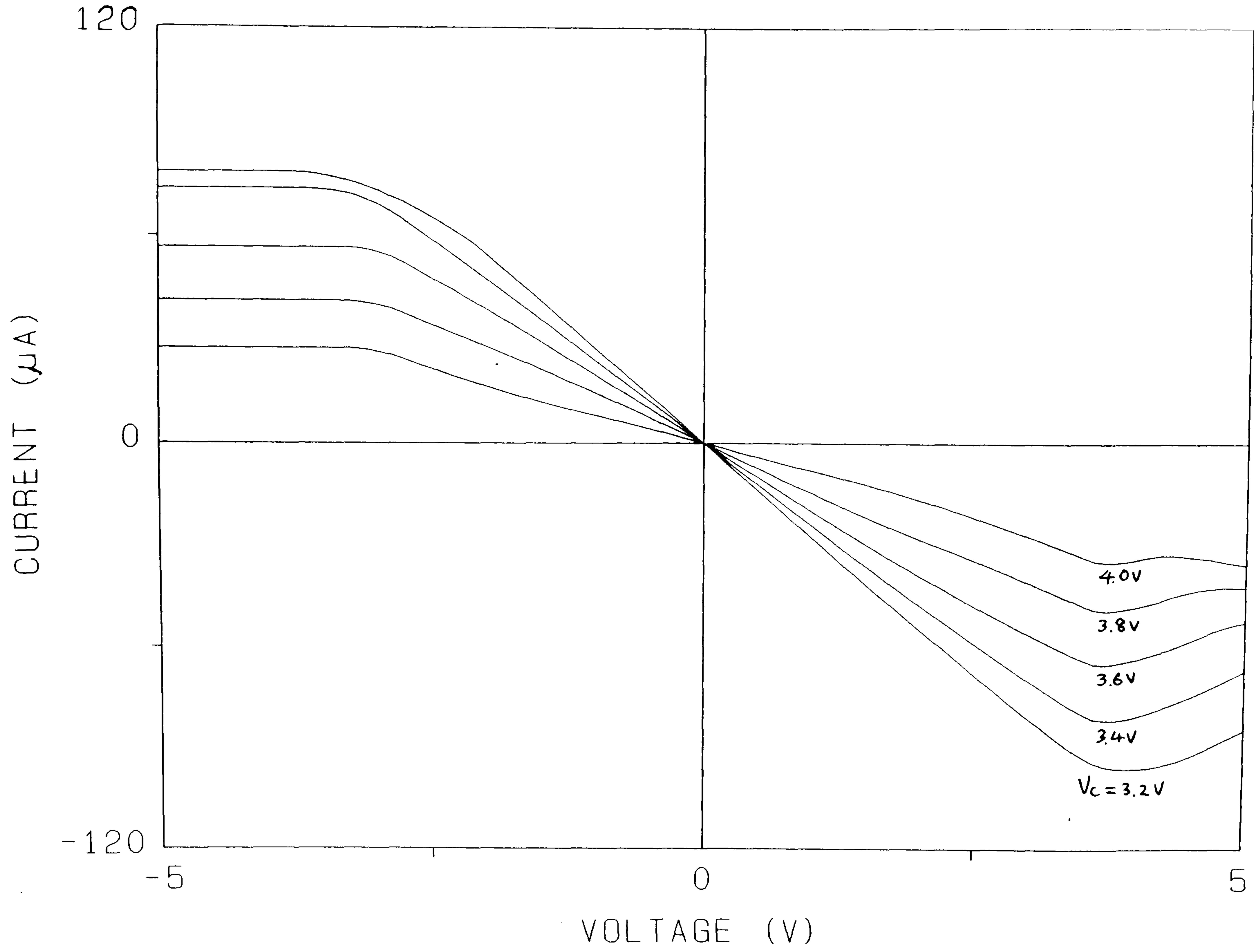


Figure 5.7: Control voltage tuning of static characteristic for ACSP transconductor

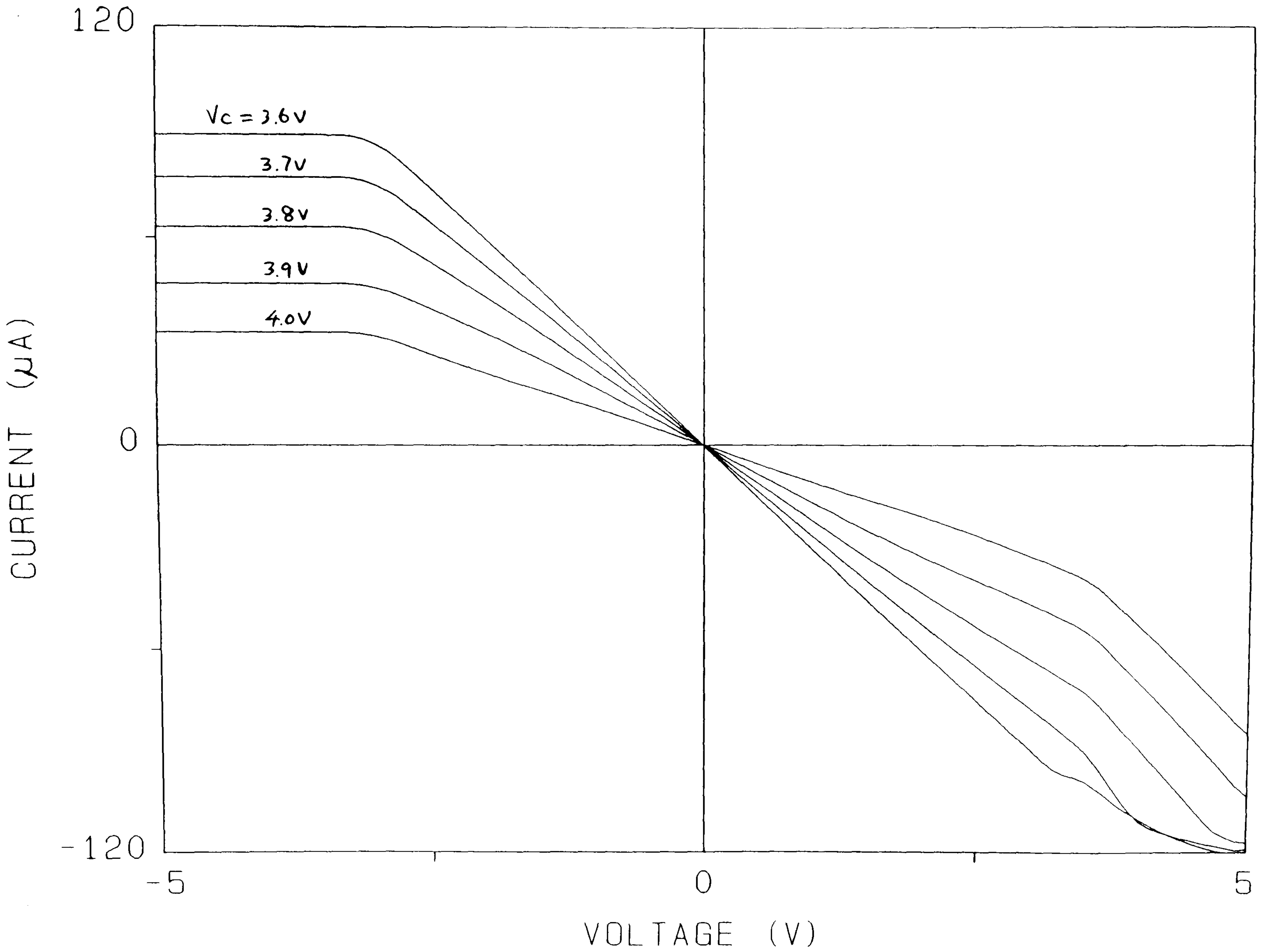


Figure 5.8: Control voltage tuning of static characteristic for OBCCP transconductor

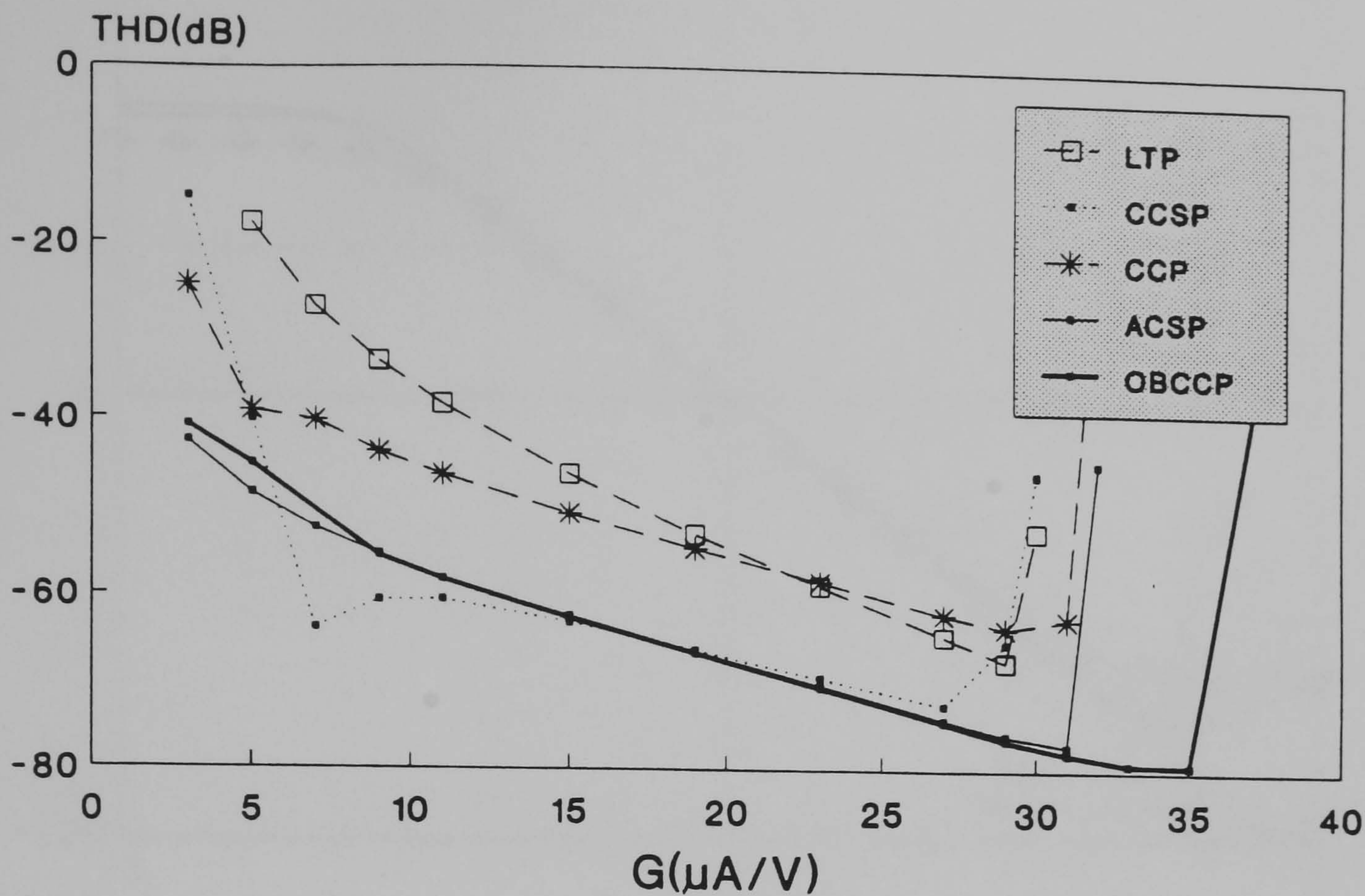


Figure 5.9: THD of OTAs with different transconductance values at $1V_{pp}$ and $\pm 5V$ supplies

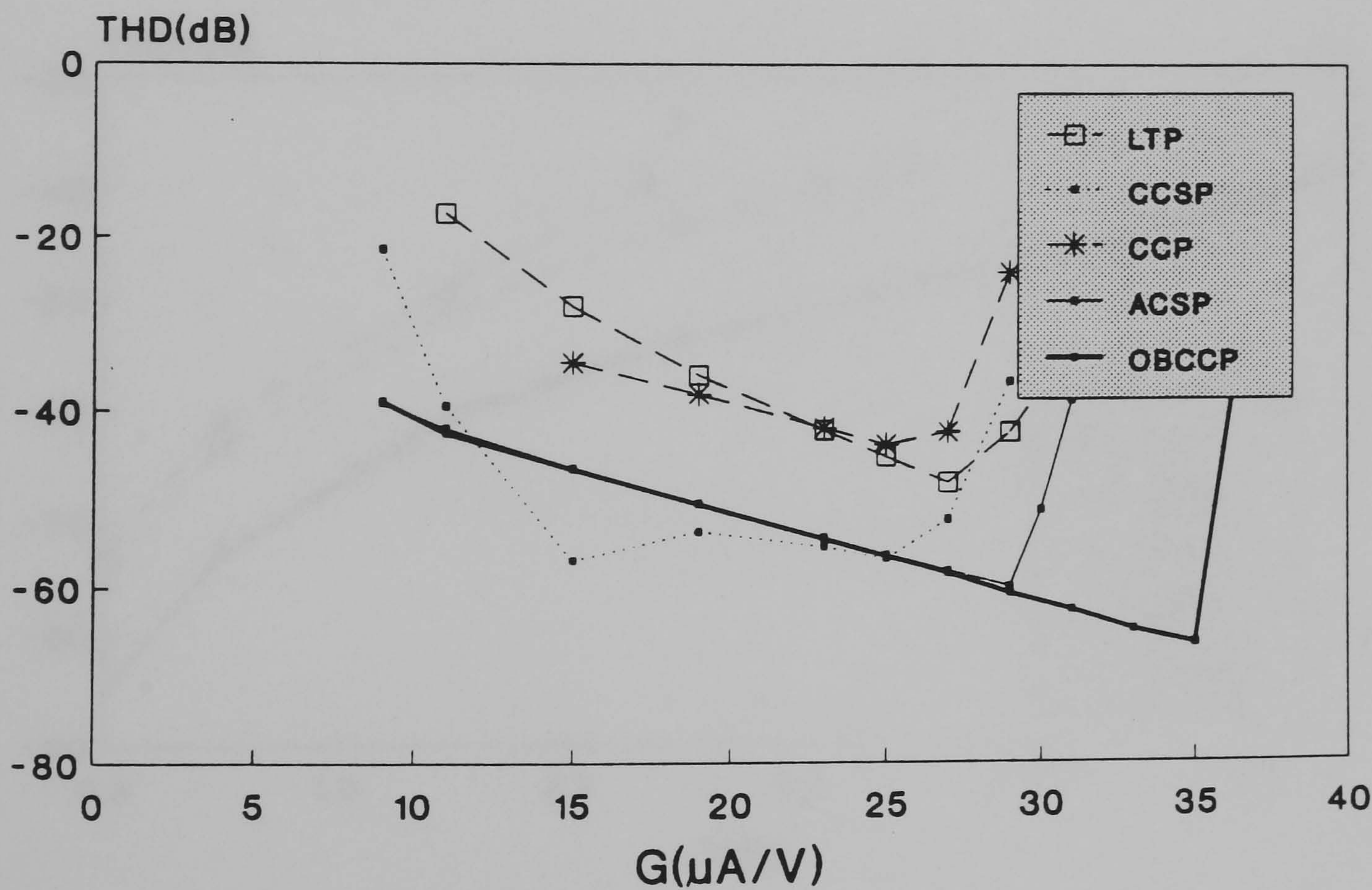


Figure 5.10: THD of OTAs with different transconductance values at $2.5V_{pp}$ and $\pm 5V$ supplies

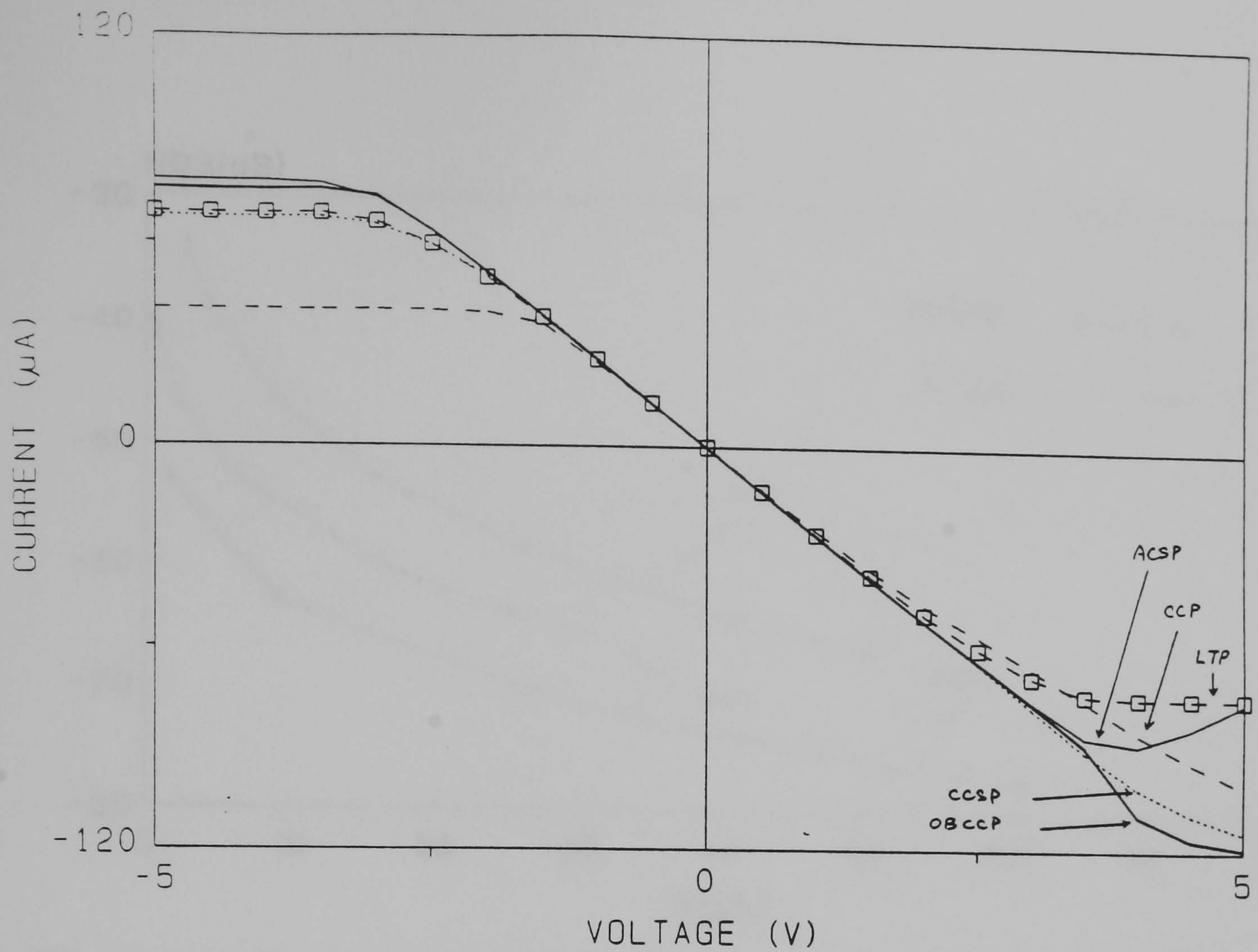


Figure 5.11: Static Characteristics of the OTAs ($26\mu A/V$)

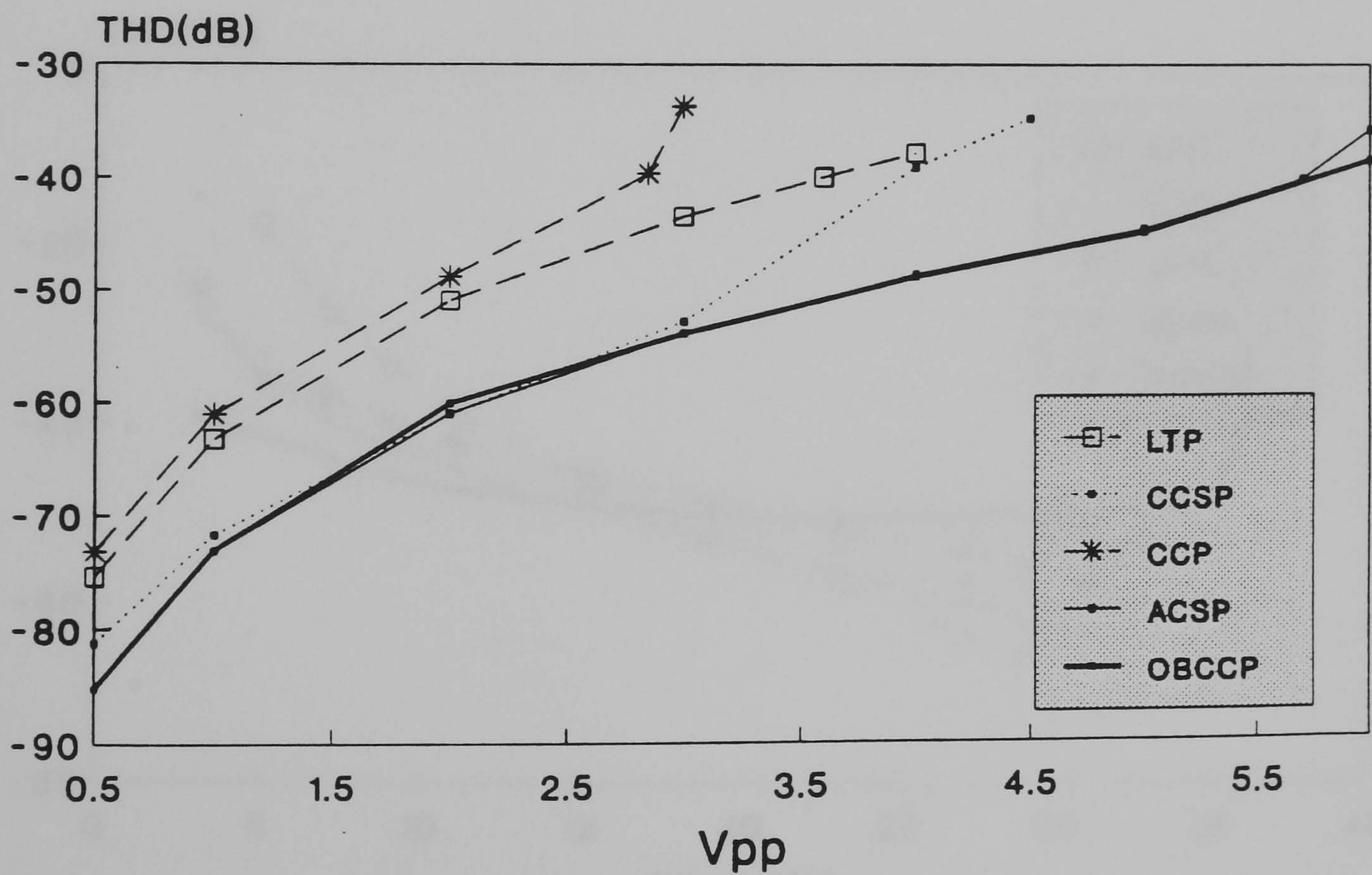


Figure 5.12: Comparison of OTAs with THD against input signal at nominal $26\mu A/V$

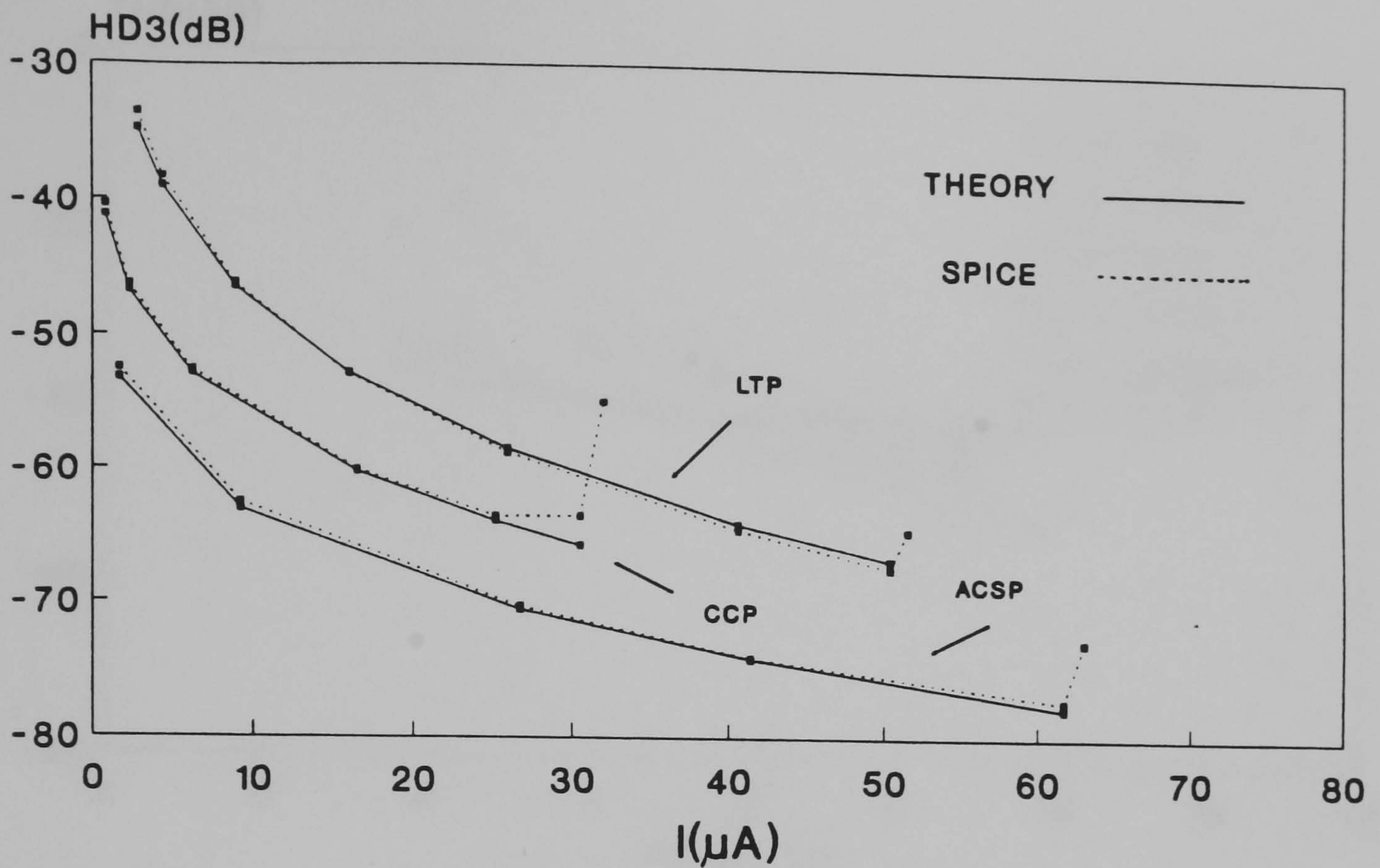


Figure 5.13: Predicted third-harmonic distortion against bias current for LTP, CCP and ACSP at $1V_{pp}$ input signal

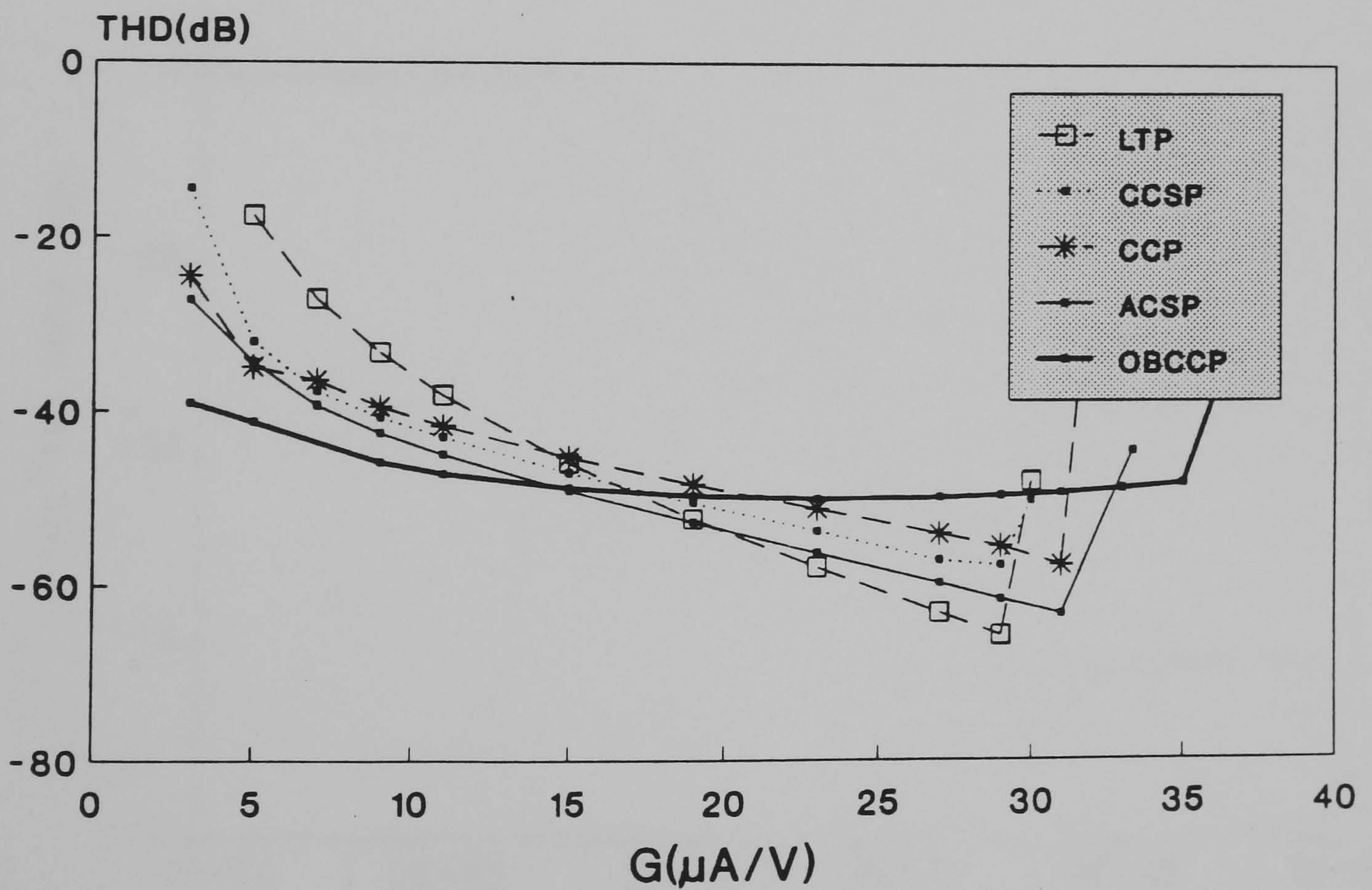


Figure 5.14: THD comparison of OTAs with variation of transconductance at $1V_{pp}$, 2% mismatches

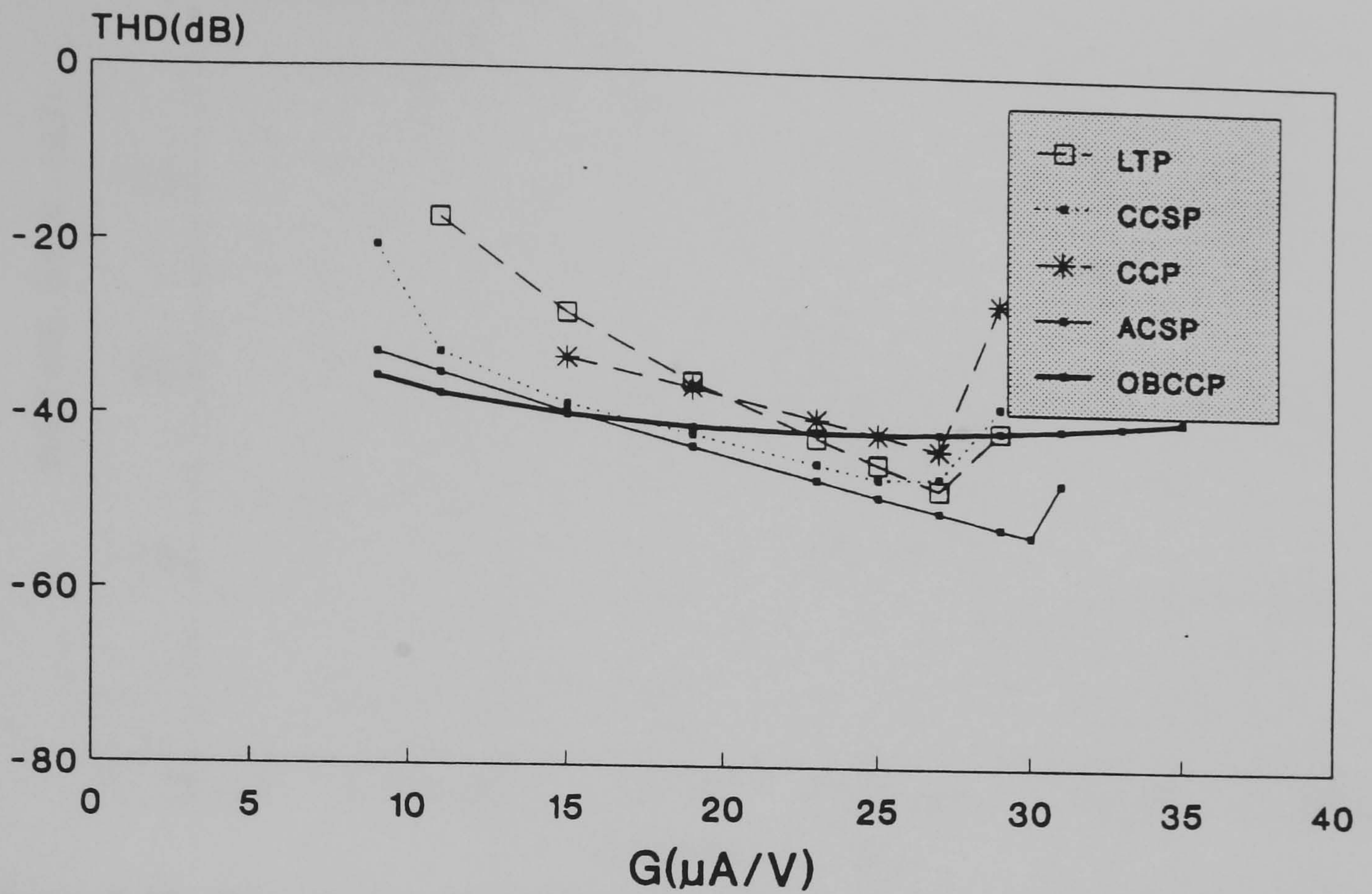


Figure 5.15: THD comparison of OTAs with variation of transconductance at $2.5Vpp$, 2% mismatches and $\pm 5V$ supplies

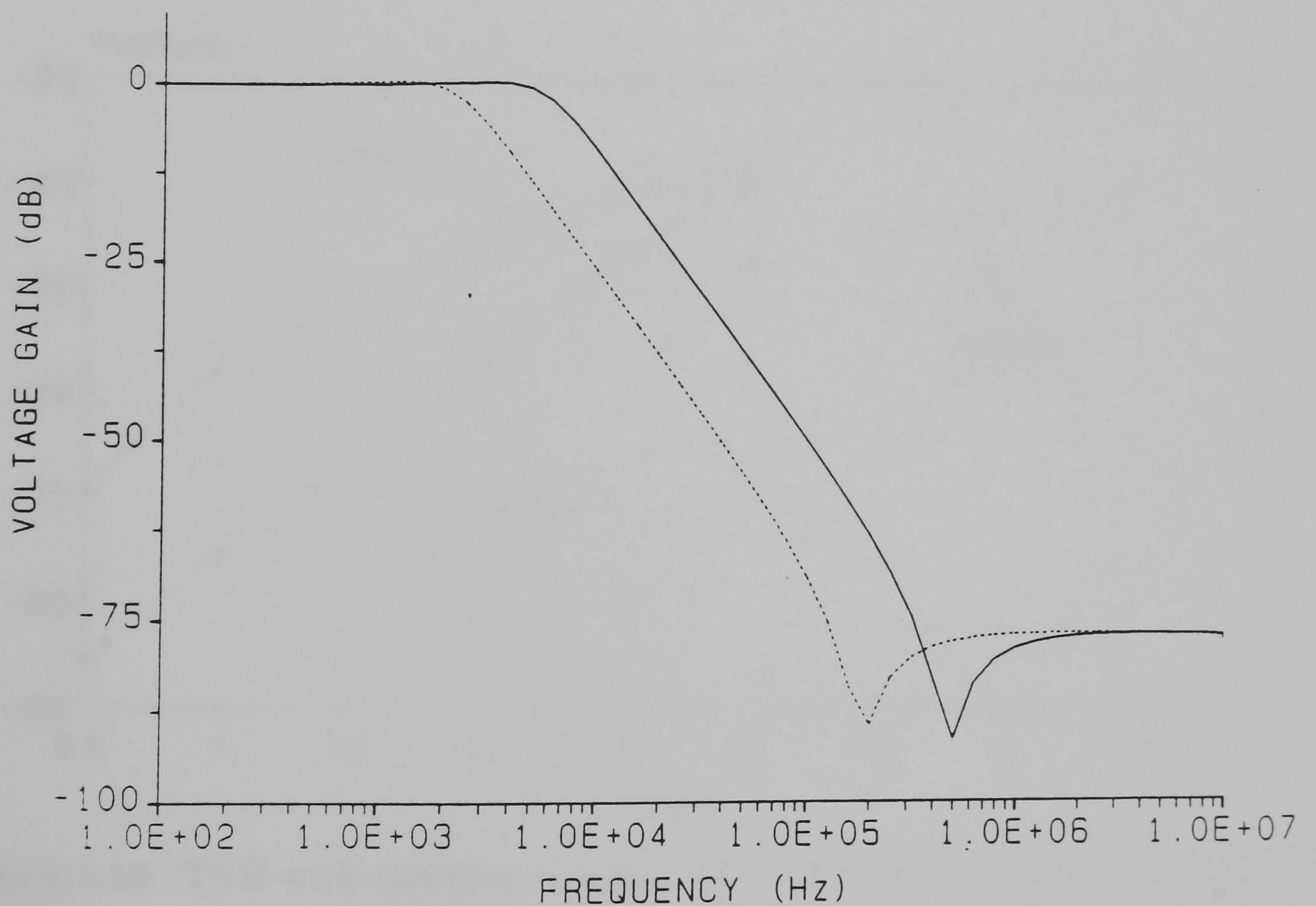


Figure 5.16: Tuning of lowpass cut-off frequency in the ACSP-based filter

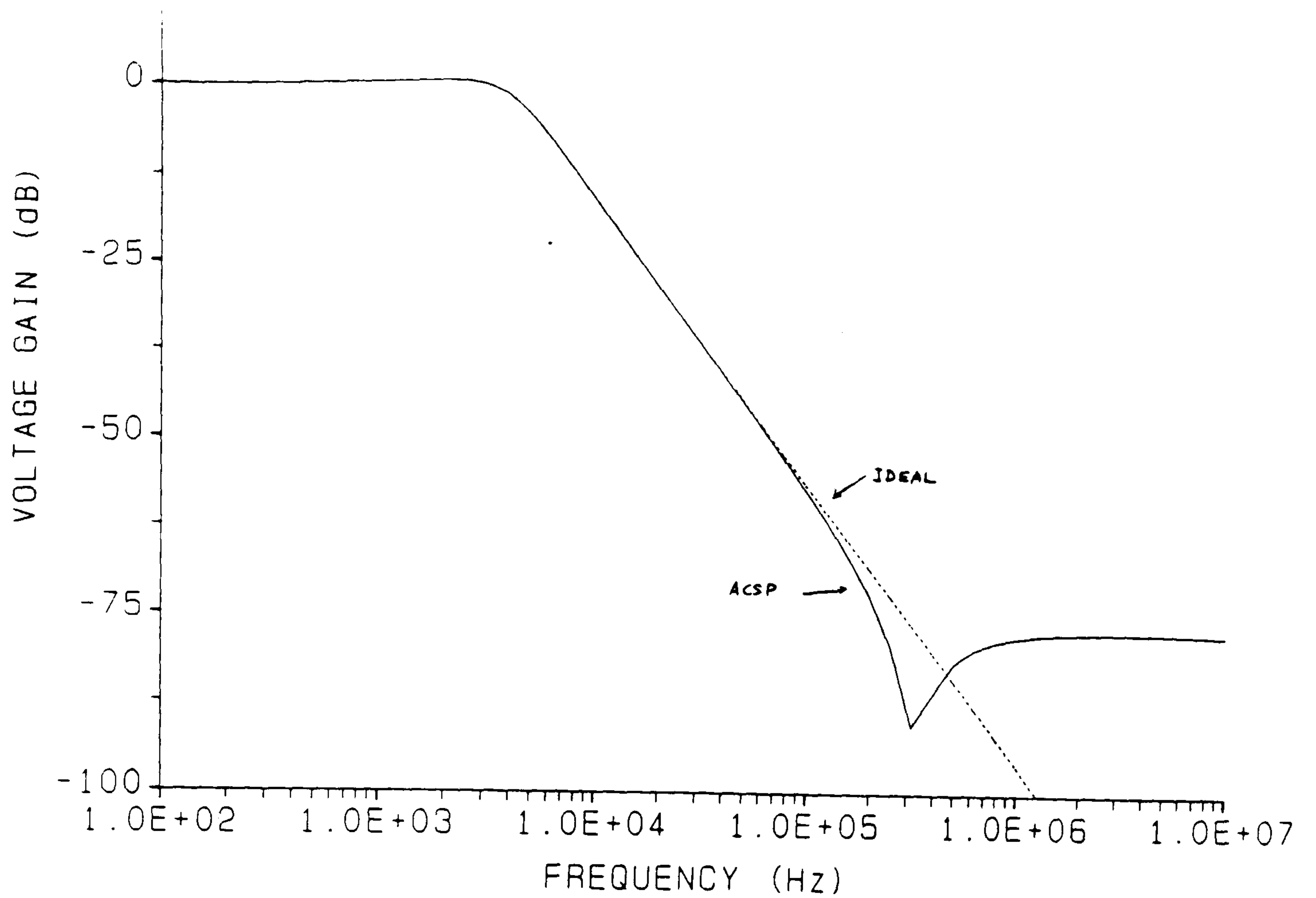


Figure 5.17: Comparsion of simulated and ideal frequency characteristic at nominal 4.7KHz cut-off frequency for ACSP-based filter

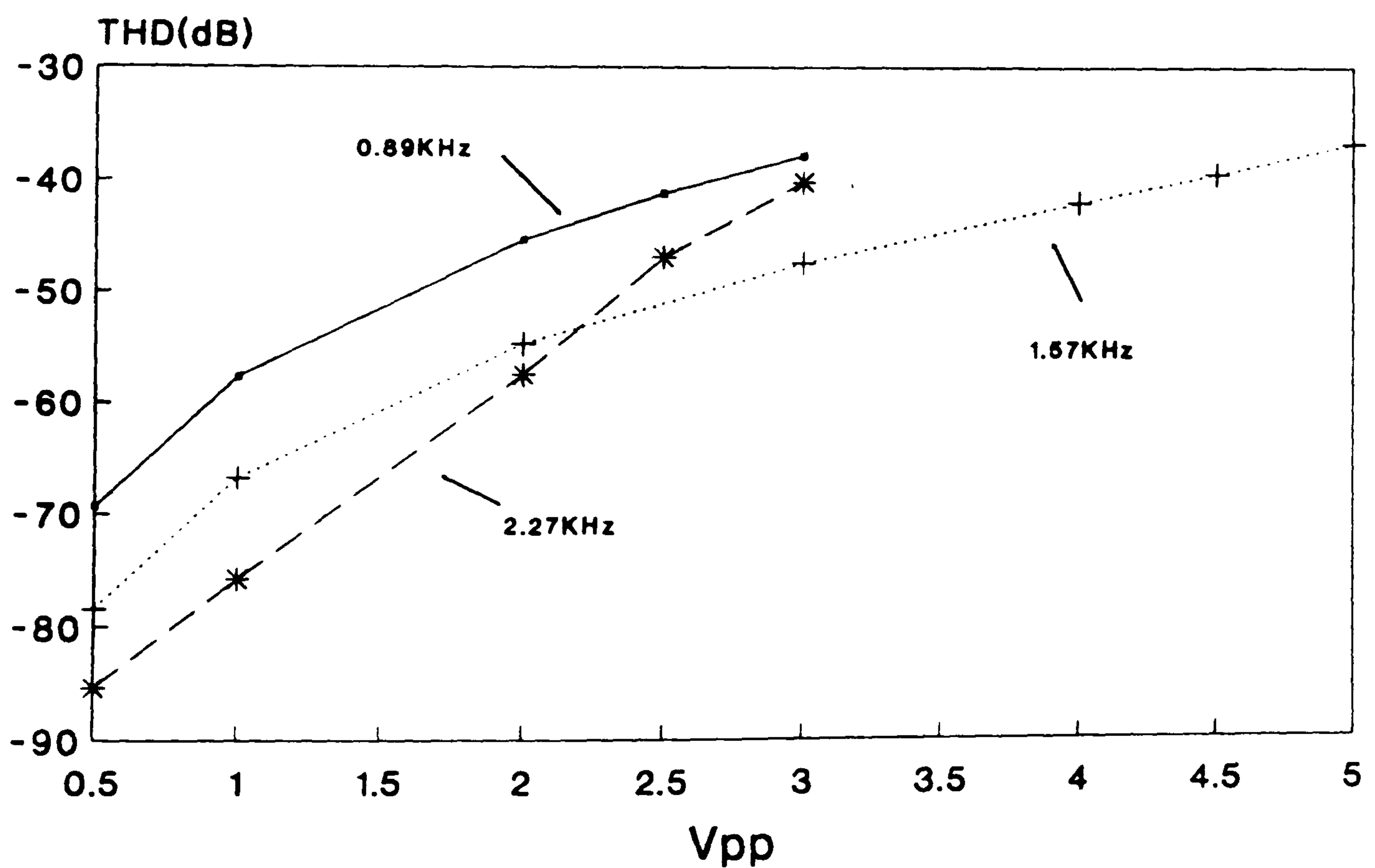


Figure 5.18: THD with variation of input signal at different frequencies (1/3 of cut-off frequencies) for ACSP-based filter

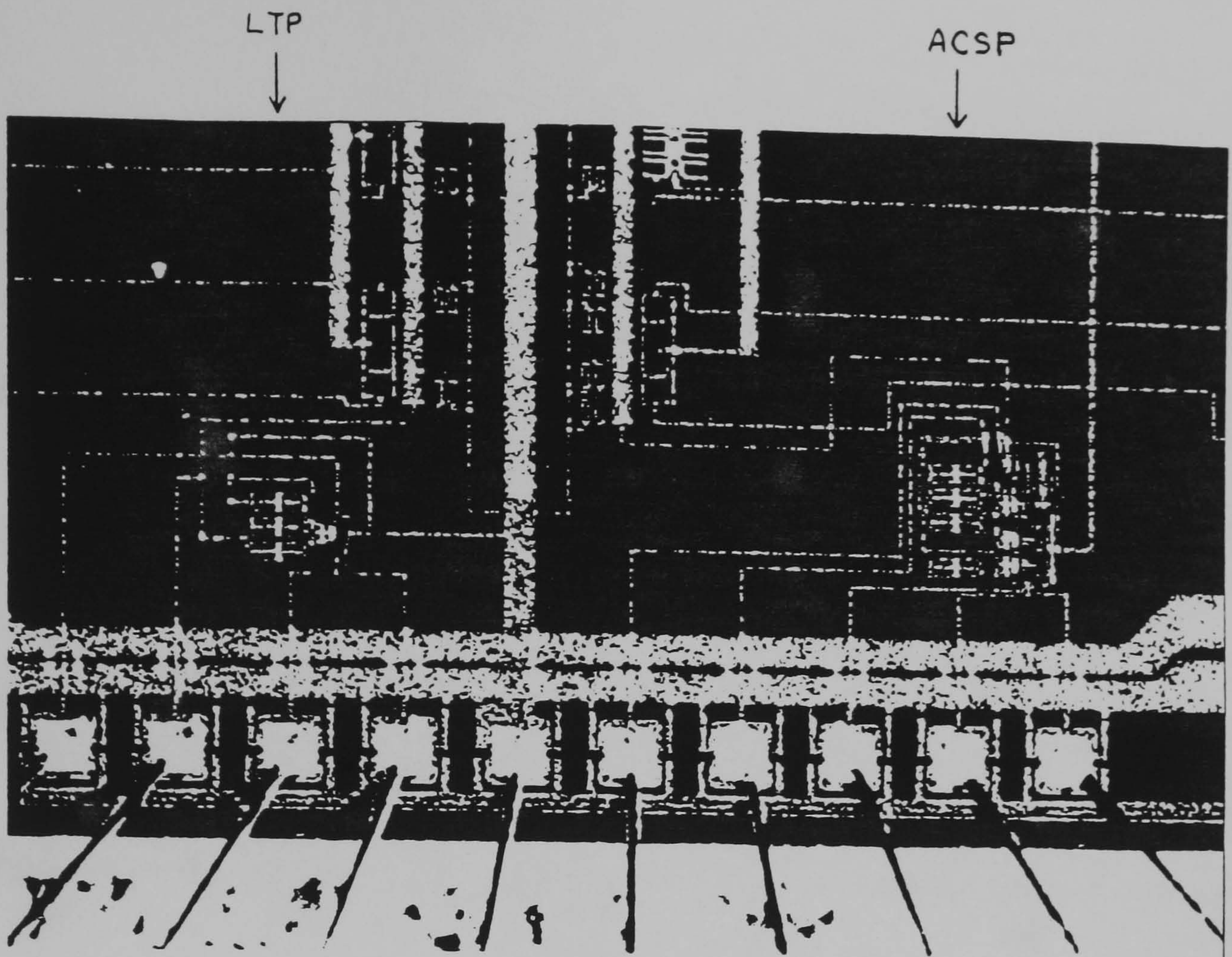


Figure 5.19: A microphotograph of the LTP and ACSP transconductors

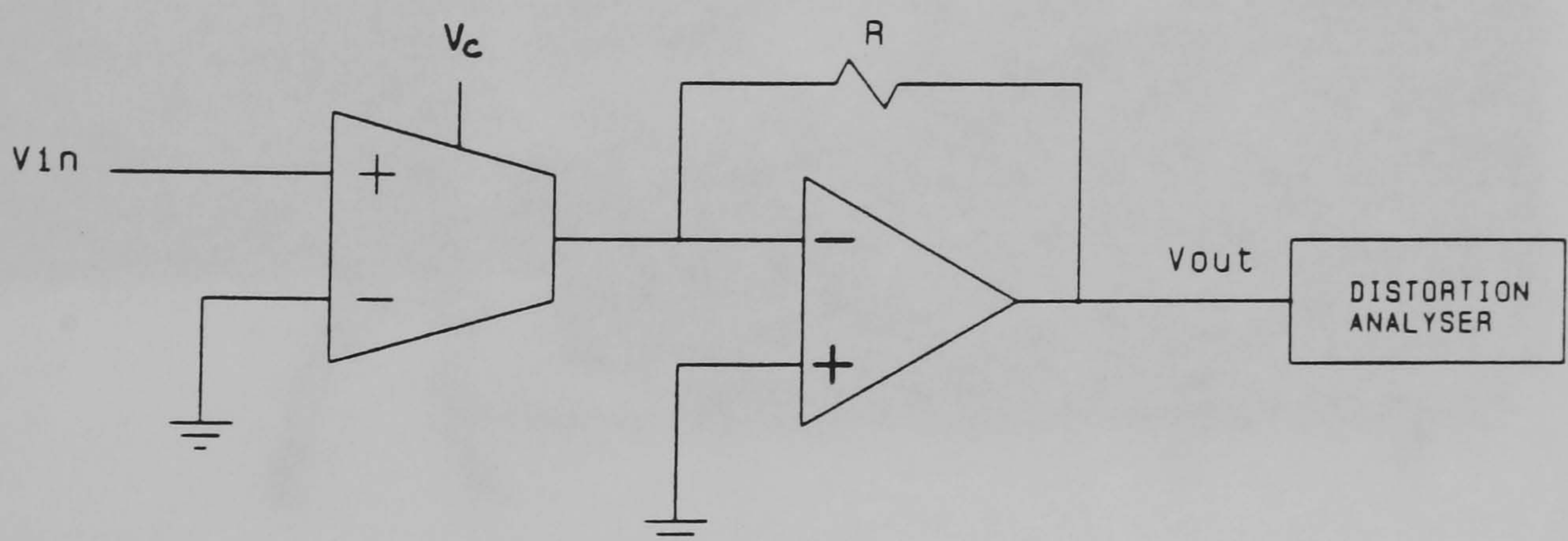


Figure 5.20: Experimental set-up for measuring the total harmonic distortion of the LTP and ACSP

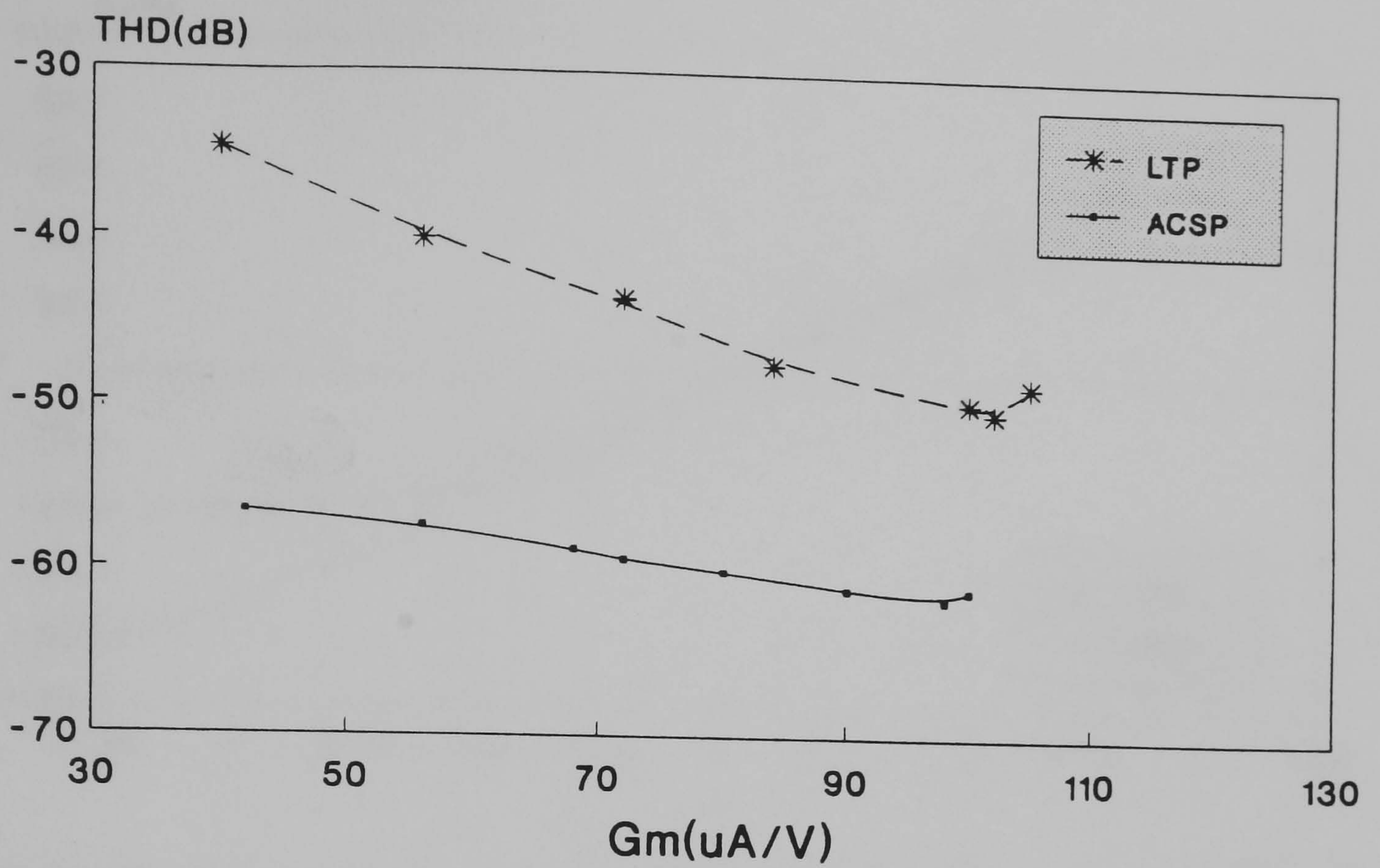


Figure 5.21: Experimental THD comparison of LTP and ACSP with variation of transconductance value

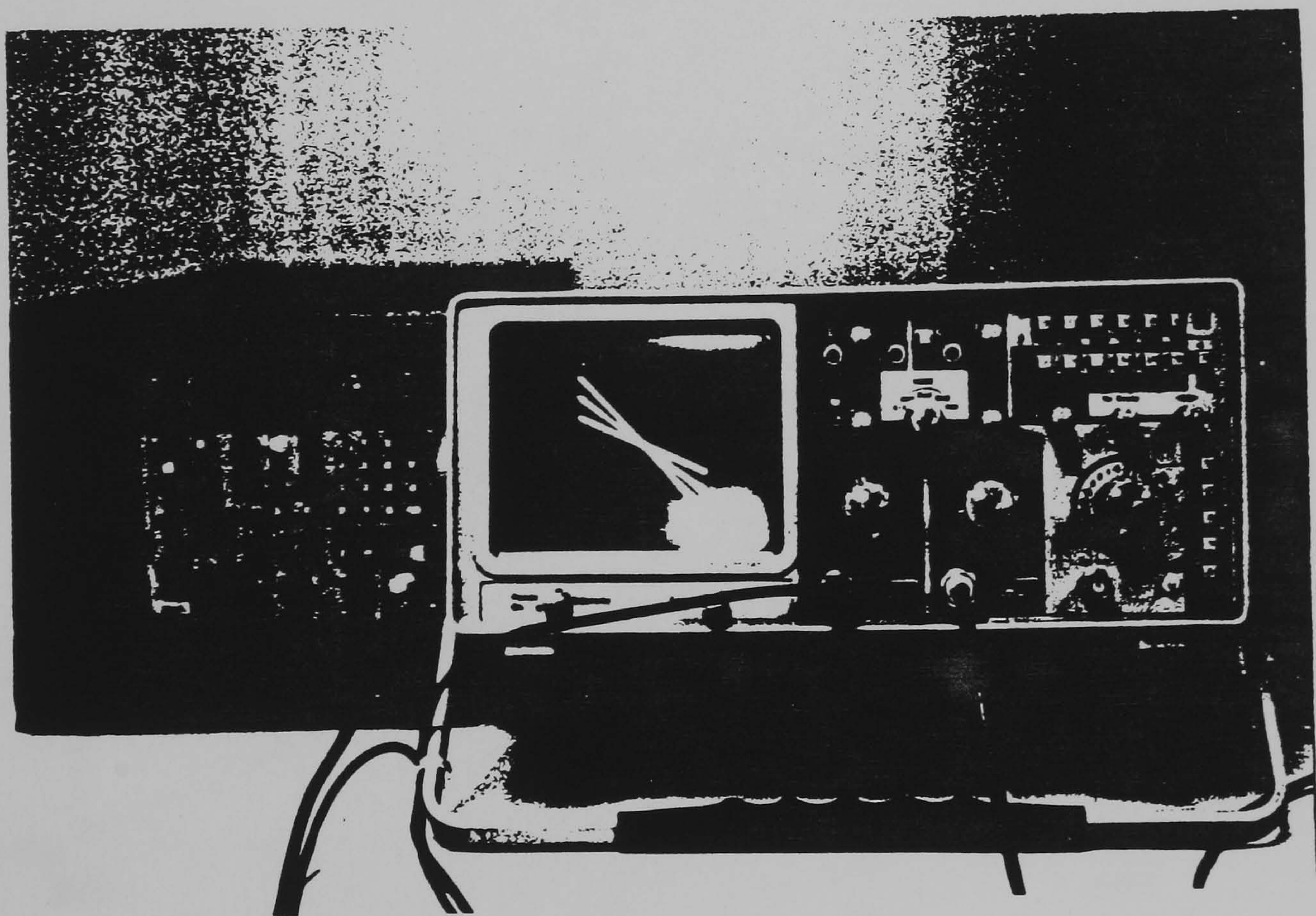


Figure 5.22: Experimental family static characteristics of the ACSP

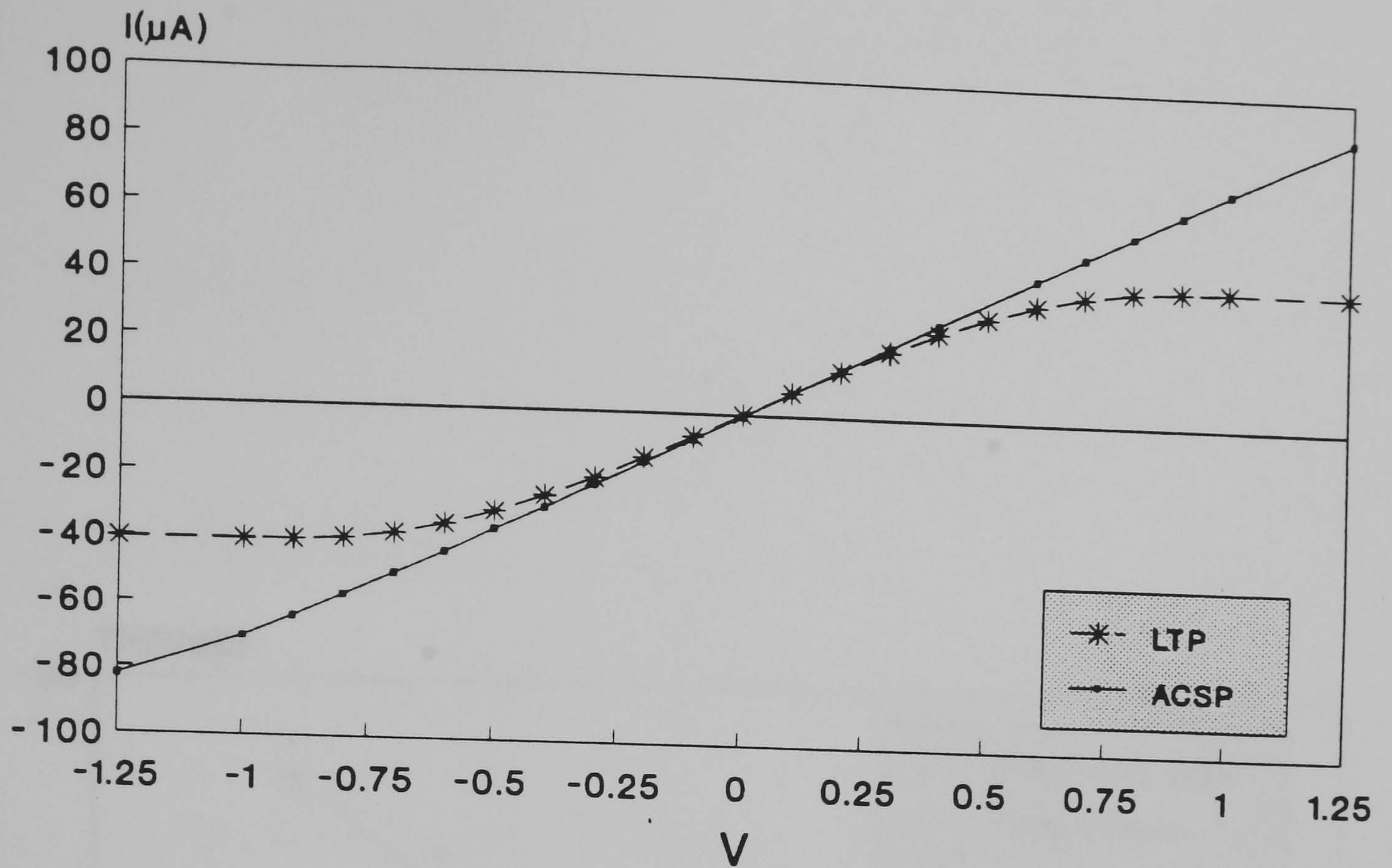


Figure 5.23: Expermental comparison of static characteristics for the LTP and ACSP at the nominal $72\mu A/V$

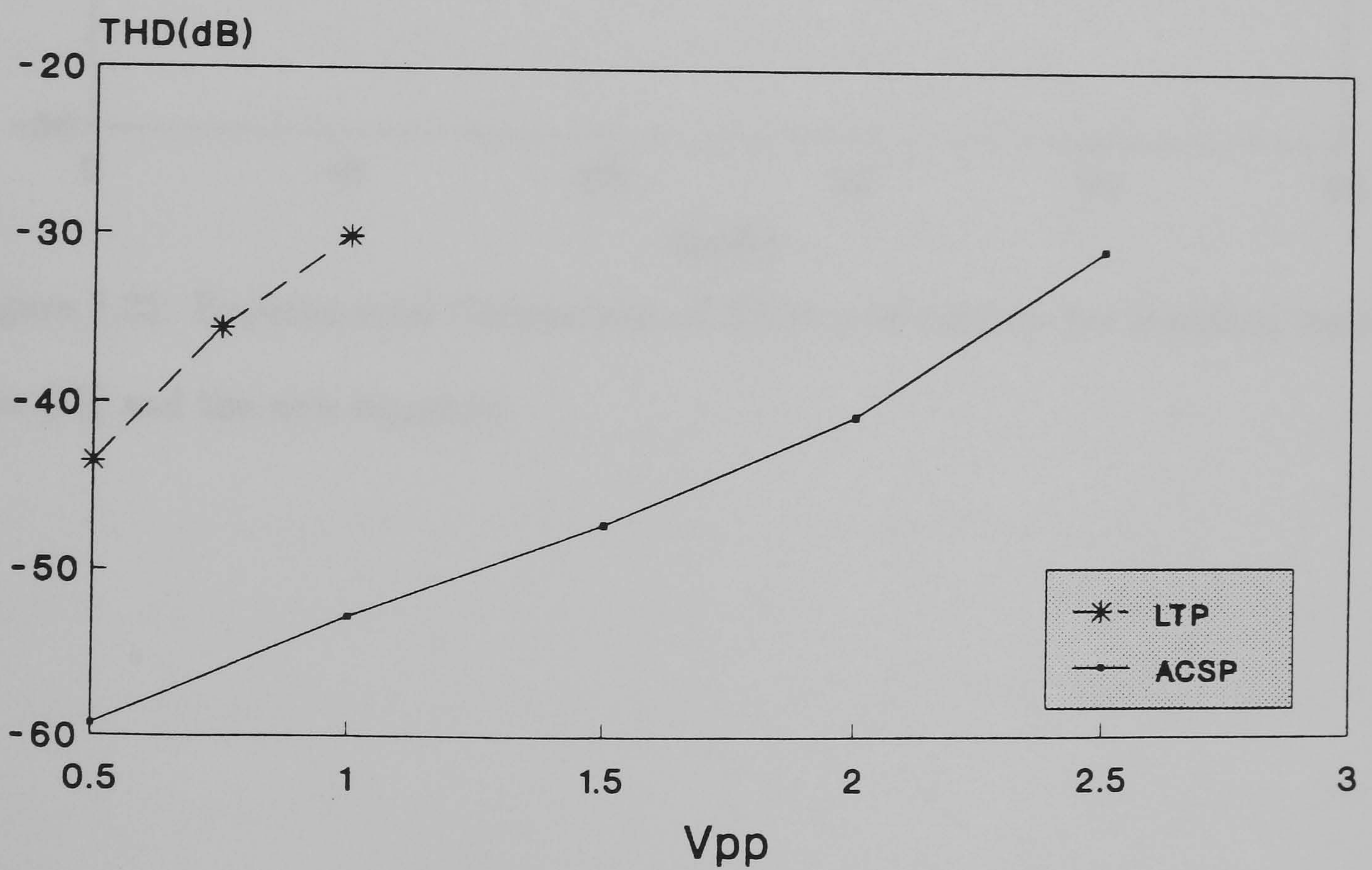


Figure 5.24: Experimental THD comparison of the LTP and ACSP against input signal at the nominal $72\mu A/V$

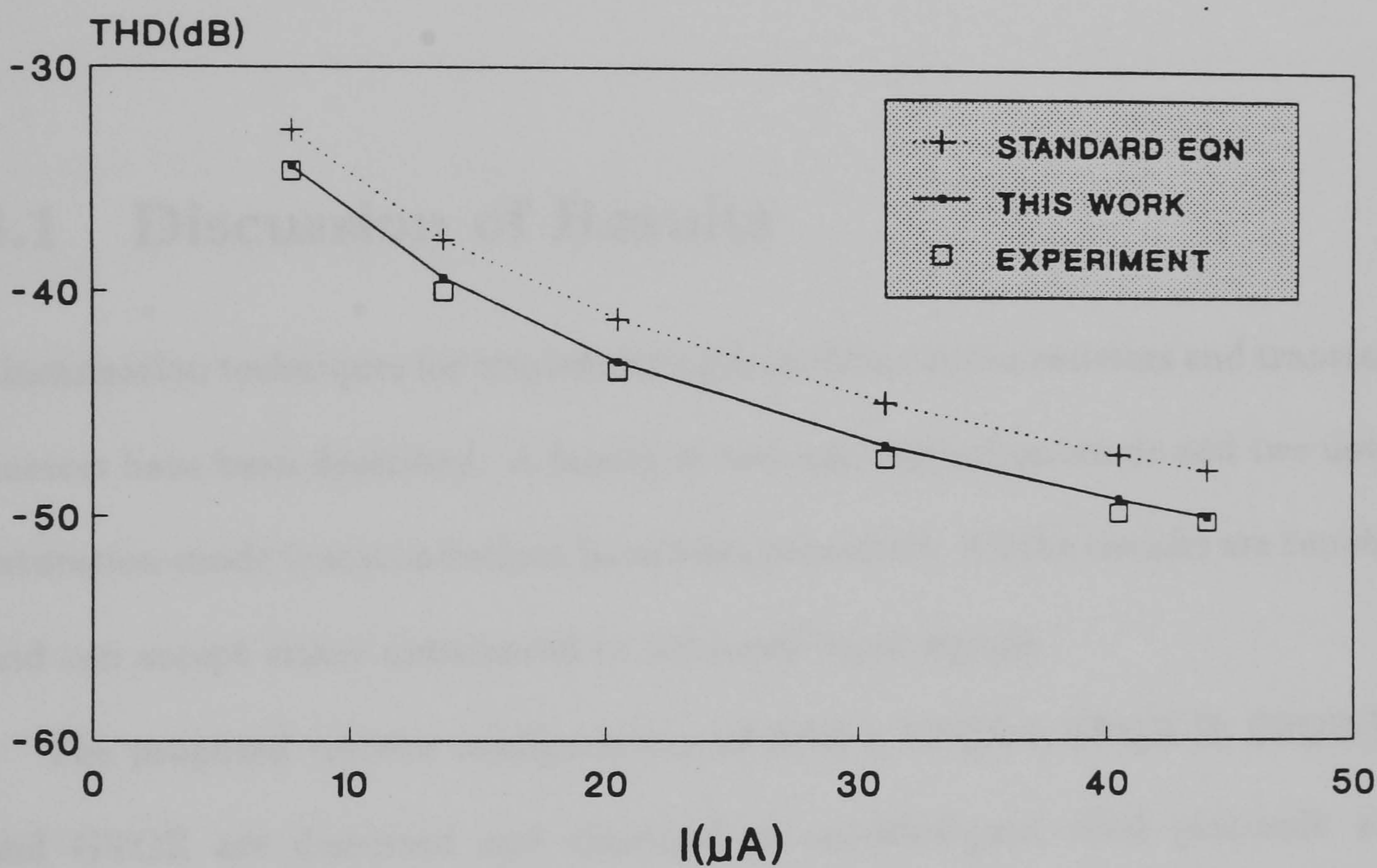


Figure 5.25: Experimental Comparison of THD predicted by the standard equation [47] and the new equation

Chapter 6

Conclusions

6.1 Discussion of Results

Linearisation techniques for implementing monolithic active resistors and transconductors have been described. A family of new non-saturation-mode and two novel saturation-mode transconductors have been presented. All the circuits are tunable and can accept either unbalanced or balanced input signals.

The proposed resistor configurations of SPR-I, SPQR-I, SPQR-II, SPQR-III and GVCR are discussed and classified as unscaled-gate, dual gate-bulk and scaled-gate compensation types. It has been shown that the bulk effect dominates the distortion in the unscaled-gate compensation resistors. On the other hand, the mobility effect and mismatch are the major factors contributing to the nonlinearity in both dual gate-bulk compensation and scaled-gate compensation resistors. Experimental and simulation results correlate well with the theoretical analysis presented and it is concluded that the proposed resistors improve on the distortion performance of previously reported counterparts [3]→[6],[8]→[18].

Five representative transconductors have been discussed in detail. The simu-

lation results suggest that the mobility effect which suppresses the third-harmonic distortion of the LTP is a fundamental cause of odd-order distortion in the other transconductors: CCSP, CCP, ACSP and OBCCP. Geometrical mismatch effects on linearity are exceptionally small in the LTP but have a significant impact in most low-distortion circuits. It has been shown that in the presence of second-order effects, the proposed ACSP and OBCCP structures exhibit superior tunability whilst maintaining acceptably low distortion levels.

Experimental results presented for both the ACSP and LTP transconductors in a CMOS process with a low mobility degradation factor, confirm the predicted distortion behaviour. The large improvement in linearity and signal-handling capability of the ACSP justifies the increase in silicon area and power consumption. The results also indicate that the low mobility factors typically found in an CMOS process would not sufficiently reduce distortion in the LTP unless some means of source degeneration is introduced. However, it is interesting to note that the third-harmonic distortion predicted for the LTP via a closed-form analytical expression conforms remarkably well with the experimental results. This agreement allows a rapid computation of distortion in LTP and significantly improves on the accuracy that the standard estimate equation for third-harmonic distortion offers.

The feasibility of the proposed resistors and transconductors in the application to continuous-time filters is demonstrated via illustrative examples. Apart from filtering, these circuits can have applications in other analogue signal-processing tasks such as oscillators, multipliers and nonlinear networks.

6.2 Recommendations of Future Work

The use of Level-3 mobility models to quantify mobility degradation effect in saturation-mode devices provides sufficent accuracy for predicting the harmonic distortion. However, for linearised non-saturation-mode resistors where the bulk effect is reduced, Level-2 and Level-3 mobility models are generally inadequate. The major reason lies in the fact that for transistors operating in non-saturation, the conducting channel is tapered and the normal electric field no longer depends only on the gate and source terminal potential, but also the drain potential. Since Level-2 and Level-3 models disregard the drain potential, they do not adequate accurately predict mobility degradation. A model [97] which takes account of all terminal potentials would provide more accurate distortion estimate. Given the normal device symmetry, it is likely that good results could be achieved using the average of drain-to-source voltage term rather than the gate-source potential in the mobility expression.

This view can be tested by a research program in which experimental results for devices compensated using the dual gate-bulk linearisation strategy are compared with simulation based on a mobility model using the average channel potential.

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Appendix A

List of Symbols

The symbols together with the relevant equations shown in this appendix are used for hand analysis. The equations are based on SPICE Level-3 MOSFET model equations simplified by ignoring second-order factors such as short-channel effect, narrow-width effect, velocity saturation etc. . The reader may consult references [38],[40],[86],[87] for the detailed discussions. It should be noted that all the symbols are defined in terms of the NMOS model shown below.

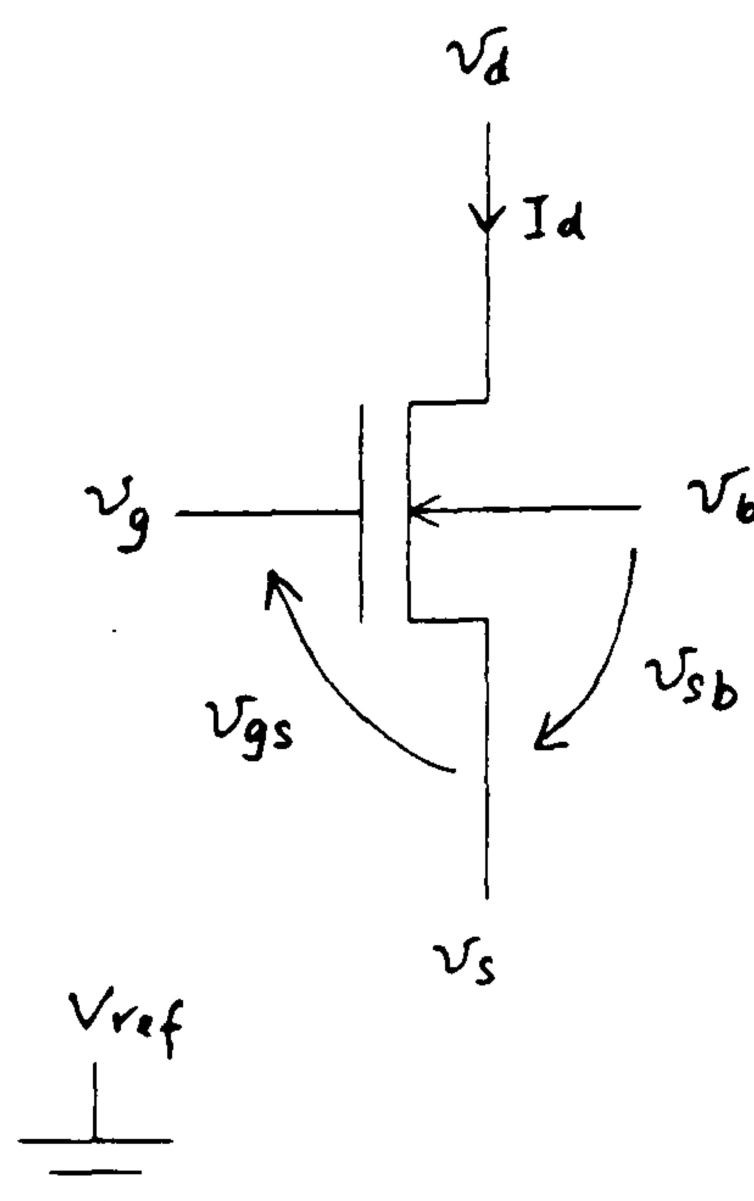


Figure A.1: A NMOS Transistor with Terminal Voltages and Current

Symbol	Unit	Description
$k = 1.38\times10^{-23}$	J/K	Boltzmann's constant
$T = 300$	K	Default temperature
$q = 1.6\times10^{-19}$	C	Electronic charge
$\phi_t = \frac{kT}{q}$	V	Thermal voltage at 300 K
$n_i = 1.45\times10^{10}$	cm^{-3}	Intrinsic carrier concentration at 300 K
$\epsilon_o = 8.854\times10^{-12}$	F/m	Permittivity of free space
$\epsilon_{si} = 1.04\times10^{-10}$	F/m	Permittivity of silicon
$\epsilon_{ox} = 3.45\times10^{-11}$	F/m	Permittivity of silicon dioxide
v_{gs}	V	Gate to source voltage
v_{ds}	V	Drain to source voltage
v_{sb}	V	Source to bulk voltage
v_{db}	V	Drain to bulk voltage
L	m	Drawn channel length
W	m	Drawn channel width
t_{ox}	m	Thin gate oxide thickness
$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$	F/m^2	Gate oxide capacitance per unit area
$\phi_B = 2\phi_t ln\frac{N_{SUB}}{ni}$	V	Surface potential; typical value is $0.6V$
N_{SUB}	cm^{-3}	Substrate doping; typical value is $1\times10^{15}cm^{-3}$

Symbol	Unit	Description
$\gamma = \frac{(2q\epsilon_{si}N_{SUB})^{\frac{1}{2}}}{C_{ox}}$	$V^{\frac{1}{2}}$	Bulk threshold parameter; typical value is 0.6
λ	V^{-1}	Channel length modulation factor; typical value is 0.02(Level 1)
V_{FB}	V	Flat band voltage
$V_{TO} = V_{FB} + \phi_B + \gamma\sqrt{\phi_B}$	V	Zero bias threshold voltage; typical value is $1V$
$V_t = V_{TO} + \gamma(\sqrt{\phi_B + v_{sb}} - \sqrt{\phi_B})$	V	Threshold votage
μ_o	cm^2/Vs	Zero field carrier mobility
$K_o = \frac{\mu_o C_{ox} W}{2L}$	$\mu A/V^2$	Zero gate field transconductance parameter, typical value is $25\mu A/V^2$
θ	V^{-1}	Mobility degradation factor; typical value is 0.1
$\mu = \frac{\mu_o}{1+\theta(v_{gs}-V_t)}$	cm^2/Vs	Effective mobility
$K = \frac{K_o}{1+\theta(v_{gs}-V_t)}$	$\mu A/V^2$	Effective transconductance parameter
$\delta = \frac{\gamma}{4(\phi_B+v_{sb})^{\frac{1}{2}}}$	-	Drain current correction term; typical value is 0.2
$K_{oc} = \frac{K_o}{1+\delta}$	$\mu A/V^2$	Drain current corrected K_o term
$K_c = \frac{K_{oc}}{1+\theta(v_{gs}-V_t)}$	$\mu A/V^2$	Drain current corrected K term
V_{pp}	V	Peak-to-Peak Voltage

Appendix B

CMOS Parameters for Plessey $2\mu m$ P-well Process

Parameter	NMOS	PMOS
VTO,V	0.99	-0.8
TOX,$\times\ 10^{-10}m$	400	400
NSUB,$\times\ 10^{15}cm^{-3}$	7	4
XJ,$\times\ 10^{-6}m$	0.18	0.21
LD,$\times\ 10^{-6}m$	0.341	0.45
UO,$\times\ cm^2/Vs$	710	300
VMAX,$\times\ 10^5m/s$	1.5	3
DELTA	0.3	0.75
THETA, V^{-1}	0.15	0.4
ETA	0.15	0.15
KAPPA	0.6	1.5
TPG	1	-1
GAMMA, $V^{0.5}$	0.65	0.46
NFS, $\times\ 10^{11}cm^{-2}$	2.4	1.68
CGSO, $\times\ 10^{-10}F/m$	0.87	1.24
CGDO, $\times\ 10^{-10}F/m$	0.87	1.24
CGBO, $\times\ 10^{-11}F/m$	2.79	4.03
PB, V	0.6	0.6
CJ, $\times\ 10^{-4}F/m^2$	1.78	1.83
JS, $\times\ 10^{-8}A/m^2$	8.2	3.46
MJ	0.481	0.526
CJSW, $\times\ 10^{-10}F/m$	3.58	2.29
MJSW	0.218	0.172

Appendix C

CMOS Parameters for Plessey $1\mu m$ Twin Well Process

Parameter	NMOS	PMOS
VTO,V	0.84	-0.84
TOX,$\times\ 10^{-10}m$	200	200
NSUB,$\times\ 10^{15}cm^{-3}$	20	20
XJ,$\times\ 10^{-6}m$	0.08	0.02
LD,$\times\ 10^{-6}m$	0.056	0.045
UO,$\times\ cm^2/Vs$	520	180
VMAX,$\times\ 10^5 m/s$	7	100
DELTA	0.52	0.35
THETA, V^{-1}	0.05	0.1
ETA	0.05	0.001
KAPPA	0.1	0.01
TPG	1	-1
GAMMA, $V^{0.5}$	-	0.53
NFS, $\times\ 10^{11}cm^{-2}$	0.16	0.15
CGSO, $\times\ 10^{-10}F/m$	1.3	1.3
CGDO, $\times\ 10^{-10}F/m$	1.3	1.3
CGBO, $\times\ 10^{-11}F/m$	1	1
PB, V	0.87	0.5035
CJ, $\times\ 10^{-4}F/m^2$	2.5	2.5
FC	0.5	0.5
MJ	0.556	0.487
CJSW, $\times\ 10^{-10}F/m$	4.1	4.1
MJSW	0.279	0.25

Appendix D

Simplified Level-2 Non-Saturation-Mode Drain-Current Equations

The objective of this appendix is to develop alternative expressions for the signal current in a single MOSFET. All the potentials are assumed to be referenced to ground. These expressions play a major role in the analysis of the non-saturation-mode linear resistor.

The non-saturation or linear-mode drain current for the single MOSFET shown in Fig. A.1, is given [36]→[38] by

$$\begin{aligned} I_d &= 2K\{(v_g - v_b - V_{FB} - \phi_B)(v_d - v_s) - \frac{1}{2}[(v_d - v_b)^2 - (v_s - v_b)^2] \\ &\quad - \frac{2}{3}\gamma[(\phi_B + v_d - v_b)^{\frac{3}{2}} - (\phi_B + v_s - v_b)^{\frac{3}{2}}]\} \end{aligned} \tag{D.1}$$

where the parameters are defined in Appendix A. Rearranging $(D.1)$ gives

$$\begin{aligned} I_d &= 2K\{(v_g - V_{FB} - \phi_B)(v_d - v_s) - \frac{1}{2}(v_d^2 - v_s^2) \\ &\quad - \frac{2}{3}\gamma[(\phi_B + v_d - v_b)^{\frac{3}{2}} - (\phi_B + v_s - v_b)^{\frac{3}{2}}]\} \end{aligned} \tag{D.2}$$

The binomial expansion of $(1+x)^n$ is given by

$$(1+x)^n = 1 + nx + \frac{n(n-1)}{2!}x^2 + \frac{n(n-1)(n-2)}{3!}x^3 + \ldots \quad (D.3)$$

Consider the first $\frac{3}{2}$ term in $(D.2)$,

$$(\phi_B - v_b + v_d)^{\frac{3}{2}} = (h + v_d)^{\frac{3}{2}} = h^{\frac{3}{2}}(1 + \frac{v_d}{h})^{\frac{3}{2}} \quad (D.4)$$

where

$$h = \phi_B - v_b \quad (D.5)$$

Using Eqn $(D.3)$ to expand the Eqn $(D.4)$ gives

$$h^{\frac{3}{2}}(1 + \frac{v_d}{h})^{\frac{3}{2}} = h^{\frac{3}{2}} + \frac{3}{2}\sqrt{h}v_d + \frac{3}{8}\frac{v_d^2}{\sqrt{h}} - \frac{1}{16}\frac{v_d^3}{h^{\frac{3}{2}}} + \frac{3}{64}\frac{v_d^4}{h^{\frac{5}{2}}} + \ldots \quad (D.6)$$

with $v_d << (\phi_B - v_b)$. Since the coefficients for the higher-order terms are progressively smaller, the following approximation can be made:

$$\begin{aligned}(\phi_B + v_d - v_b)^{\frac{3}{2}} \approx\ & (\phi_B - v_b)^{\frac{3}{2}} + \frac{3}{2}\sqrt{(\phi_B - v_b)}v_d^2 \\ & + \frac{3}{8}\frac{v_d^2}{\sqrt{\phi_B - v_b}} - \frac{1}{16}\frac{v_d^3}{(\phi_B - v_b)^{\frac{3}{2}}} \end{aligned} \quad (D.7)$$

Similarly,

$$\begin{aligned}(\phi_B + v_s - v_b)^{\frac{3}{2}} \approx\ & (\phi_B - v_b)^{\frac{3}{2}} + \frac{3}{2}\sqrt{(\phi_B - v_b)}v_s^2 \\ & + \frac{3}{8}\frac{v_s^2}{\sqrt{\phi_B - v_b}} - \frac{1}{16}\frac{v_s^3}{(\phi_B - v_b)^{\frac{3}{2}}} \end{aligned} \quad (D.8)$$

where $v_s << (\phi_B - v_b)$. By substituting $(D.7)$ and $(D.8)$ into $(D.2)$, the drain current can be approximated as

$$\begin{aligned} I_d =\ & 2K[(v_g - V_{FB} - \phi_B - \gamma\sqrt{\phi_B - v_b})(v_d - v_s) \\ & - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - v_b}})(v_d^2 - v_s^2) + \frac{\gamma}{24(\phi_B - v_b)^{\frac{3}{2}}}(v_d^3 - v_s^3)] \end{aligned} \quad (D.9)$$

or

$$I_d = 2K[(v_g - V_t^*)(v_d - v_s) - \frac{m'}{2}(v_d^2 - v_s^2) + \frac{\gamma}{24(\phi_B - v_b)^{\frac{3}{2}}}(v_d^3 - v_s^3)] \quad (D.10)$$

where

$$V_t^* = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - v_b} \tag{D.11}$$

and

$$m' = 1 + \frac{\gamma}{2\sqrt{\phi_B - v_b}} \tag{D.12}$$

The drain current $(D.1)$ can be rewritten as the form

$$\begin{aligned} I_d &= 2K\{(v_{gs} - V_{FB} - \phi_B)v_{ds} - \frac{1}{2}v_{ds}^2 \\ &\quad - \frac{2}{3}\gamma[(\phi_B + v_{sb} + v_{ds})^{\frac{3}{2}} - (\phi_B + v_{sb})^{\frac{3}{2}}]\} \end{aligned} \tag{D.13}$$

Let $h = \phi_B + v_{sb}$. By expanding the first $\frac{3}{2}$ term in binomial expansion $(D.3)$,

$$\begin{aligned} (\phi_B + v_{sb} + v_{ds})^{\frac{3}{2}} &\approx (\phi_B + v_{sb})^{\frac{3}{2}} + \frac{3}{2}v_{ds}\sqrt{\phi_B + v_{sb}} \\ &\quad + \frac{3}{8}\frac{v_{ds}^2}{\sqrt{\phi_B + v_{sb}}} - \frac{1}{16}\frac{v_{ds}^3}{(\phi_B + v_{sb})^{\frac{3}{2}}} \end{aligned} \tag{D.14}$$

where $v_{ds} << (\phi_B + v_{sb})$. Therefore,

$$\begin{aligned} \frac{2}{3}\gamma[(\phi_B + v_{sb} + v_{ds})^{\frac{3}{2}} - (\phi_B + v_{sb})^{\frac{3}{2}}] &\approx \gamma v_{ds}\sqrt{\phi_B + v_{sb}} + \frac{\gamma v_{ds}^2}{4\sqrt{\phi_B + v_{sb}}} \\ &\quad - \frac{\gamma v_{ds}^3}{24(\phi_B + v_{sb})^{\frac{3}{2}}} \end{aligned} \tag{D.15}$$

Substituting $(D.15)$ into $(D.13)$, the drain current is

$$\begin{aligned} I_d &= 2K[(v_{gs} - V_{FB} - \phi_B - \gamma\sqrt{\phi_B + v_{sb}})v_{ds} \\ &\quad - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb}}})v_{ds}^2 + \frac{\gamma v_{ds}^3}{24(\phi_B + v_{sb})^{\frac{3}{2}}}] \end{aligned} \tag{D.16}$$

or

$$I_d = 2K[(v_{gs} - V_t)v_{ds} - \frac{m}{2}v_{ds}^2 + \frac{\gamma v_{ds}^3}{24(\phi_B + v_{sb})^{\frac{3}{2}}}] \tag{D.17}$$

where

$$V_t = V_{FB} + \phi_B + \gamma\sqrt{\phi_B + v_{sb}} \tag{D.18}$$

and

$$m = 1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb}}} \tag{D.19}$$

It should be noted that Eqn $(D.16)$ is equivalent to $(D.9)$. The following proof is shows that they are identical.

Consider Eqn $(D.13)$, the binomial expansion of the square-root terms are

$$\gamma\sqrt{\phi_B + v_{sb}} = \gamma\sqrt{\phi_B - v_b} + \frac{\gamma v_s}{2\sqrt{\phi_B - v_b}} - \frac{\gamma v_s^2}{8(\phi_B - v_b)^{\frac{3}{2}}} + \cdots \tag{D.20}$$

$$\frac{\gamma v_{ds}^2}{2\sqrt{\phi_B + v_{sb}}} = \frac{\gamma v_{ds}^2}{2\sqrt{\phi_B - v_b}} - \frac{\gamma v_{ds}^2 v_s}{4(\phi_B - v_b)^{\frac{3}{2}}} + \frac{3\gamma v_{ds}^2 v_s^2}{16(\phi_B - v_b)^{\frac{5}{2}}} + \cdots \tag{D.21}$$

$$\frac{\gamma v_{ds}^3}{24\sqrt{\phi_B + v_{sb}}} = \frac{\gamma v_{ds}^3}{24\sqrt{\phi_B - v_b}} - \frac{\gamma v_{ds}^3 v_s}{96(\phi_B - v_b)^{\frac{3}{2}}} + \frac{3\gamma v_{ds}^3 v_s^2}{384(\phi_B - v_b)^{\frac{5}{2}}} + \cdots \tag{D.22}$$

$(D.20)$, $(D.21)$ and $(D.22)$ are valid only when $v_s << (\phi_B - v_b)$. By substituting Eqns $(D.20)$, $(D.21)$ and $(D.22)$ back into the Eqn $(D.16)$ and ignoring the contribution due to the fourth-order term or above gives $(D.9)$.

Appendix E

Simplified Level-3 Saturation-Mode Drain-Current Equations

The Level-3 equations are based on a semi-empirical model. Several empirical parameters (parameters not obviously related to or motivated by the MOSFET device physics of the MOSFET) are introduced in the Level-3 model. This appendix simplifies the Level-3 saturation-mode drain current equation to obtain manageable equations for the transistors operating in the saturation region.

In the absence of short-channel and narrow-width effects, the saturation drain current equation [87] is given by

$$I_d = [\frac{\mu_o}{1 + \theta(v_{gs} - V_t) + \frac{\mu_o v_{dsat}}{V_{max} L}}] \frac{C_{ox} W}{L} (v_{gs} - V_t - \frac{1+\delta}{2} v_{dsat}) v_{dsat} (1 + \frac{\Delta L}{L}) \quad \text{(E.1)}$$

where

$$V_t = V_{FB} + \phi_B + \gamma\sqrt{\phi_B + v_{sb}} \quad \text{(E.2)}$$

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{\frac{1}{2}} \quad \text{(E.3)}$$

$$v_{sat} = \frac{v_{gs} - V_t}{1+\delta} \quad (E.4)$$

$$v_c = \frac{V_{max}L[1+\theta(V_{gs} - V_t)]}{\mu_o} \quad (E.5)$$

$$\Delta L = -\frac{xd^2ep}{2} + [(\frac{xd^2ep}{2})^2 + xd^2KAPPA(vds - v_{dsat})]^{\frac{1}{2}} \quad (E.6)$$

$$ep = \frac{v_c(v_c + v_{dsat})}{v_{dsat}L} \quad (E.7)$$

$$\delta = \frac{\gamma}{4\sqrt{\phi_B + v_{sb}}} \quad (E.8)$$

where the symbols are defined in the Appendix A. Assuming that $v_{dsat} \approx v_{sat}$, Eqn $(E.1)$ becomes

$$I_d = [\frac{\mu_o}{1+\theta(v_{gs} - V_t) + \frac{\mu_o v_{sat}}{V_{max}L}}]\frac{C_{ox}W}{L}(v_{gs} - V_t - \frac{1+\delta}{2}v_{sat})v_{dsat}(1+\frac{\Delta L}{L}) \quad (E.9)$$

Using Eqn $(E.4)$, the drain current can be approximated as

$$I_d \approx \frac{K_{oc}}{[1+(\theta+\alpha)(v_{gs} - V_t)]}(v_{gs} - V_t)^2(1+\frac{\Delta L}{L}) \quad (E.10)$$

where

$$K_{oc} = \frac{\mu_o C_{ox} W}{2L(1+\delta)} \quad (E.11)$$

and

$$\alpha = \frac{\mu_o}{V_{max}L(1+\delta)} \quad (E.12)$$

For the long channel transistor, the channel length modulation and the velocity saturation effect is negligible. The drain current in Eqn (E.9) can be further simplified as

$$I_d \approx \frac{K_{oc}}{[1+\theta(v_{gs} - V_t)]}(v_{gs} - V_t)^2 \quad (E.13)$$

or

$$I_d = K_c(v_{gs} - V_t)^2 \quad (E.14)$$

where

$$K_c = \frac{K_{oc}}{1+\theta(v_{gs} - V_t)} \quad (E.15)$$

In many cases, the drain current correction factor δ can be ignored and Eqn $(E.11)$ becomes

$$K_o = \frac{\mu_o C_{ox} W}{2L} \tag{E.16}$$

and the drain current is

$$I_d \approx K(v_{gs} - V_t)^2 \tag{E.17}$$

where

$$K = \frac{K_o}{1 + \theta(v_{gs} - V_t)} \tag{E.18}$$

Appendix F

Dual Gate-Bulk Compensation Technique for Single-Transistor Resistor

It will be demonstrated that by applying a common-mode signal to the gate and bulk terminal of a single MOSFET transistor, the quadratic term due to bulk effect would be eliminated. Fig. F.1 shows the schematic for this technique. The two expressions derived in Appendix D are used to show that they give the same result. It should be noted that the proof assumes constant mobility. The quadratic approximation to drain current $(D.9)$ is

$$\begin{aligned} I_d &= 2K[(v_g - V_{FB} - \phi_B - \gamma\sqrt{\phi_B - v_b})(v_d - v_s) \\ &\quad - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - v_b}})(v_d^2 - v_s^2)] \end{aligned} \tag{F.1}$$

If the gate and bulk control voltages are defined by

$$v_g = V_C + \frac{v_d + v_s}{2} \tag{F.2}$$

$$v_b = V_B + \frac{v_d + v_s}{2} \tag{F.3}$$

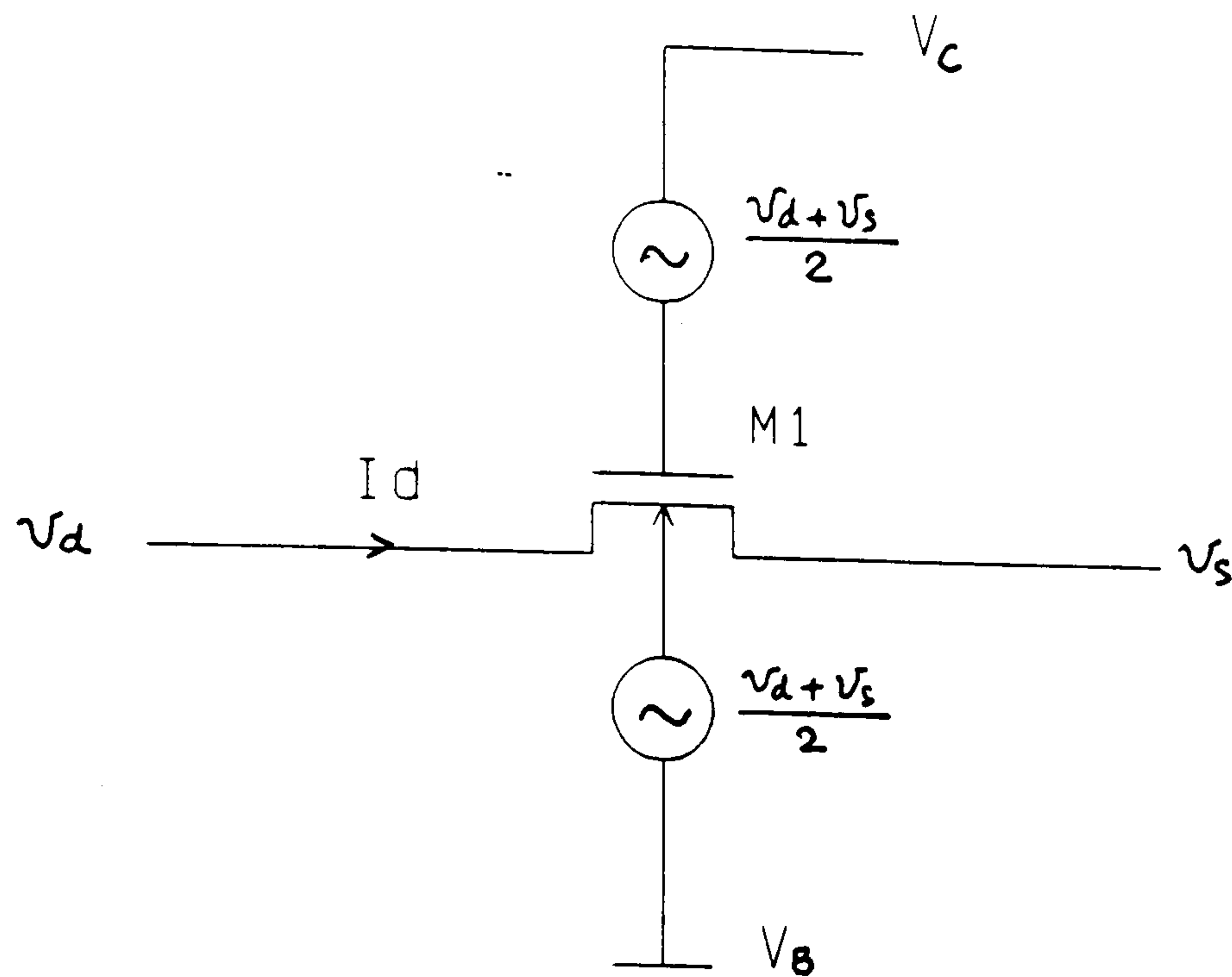


Figure F.1: Dual Gate-Bulk Compensation Single Transistor

where V_C and V_B are the gate and bulk dc bias control voltages respectively. Substituting $(F.2)$ and $(F.3)$ back into $(F.1)$ gives

$$\begin{aligned} I_d &= 2K[(V_C + \frac{v_d + v_s}{2} - V_{FB} - \phi_B - \gamma\sqrt{\phi_B - V_B - \frac{v_d + v_s}{2}})(v_d - v_s) \\ &\quad - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B - \frac{v_d+v_s}{2}}})(v_d^2 - v_s^2)] \end{aligned} \tag{F.4}$$

On expanding the square root terms and ignoring the contribution of the cubic term and higher-order terms,

$$\begin{aligned} I_d &\approx 2K\{[V_C + \frac{v_d + v_s}{2} - V_{FB} - \phi_B - \gamma\sqrt{\phi_B - V_B} + \frac{\gamma(v_d + v_s)}{4\sqrt{\phi_B - V_B}}](v_d - v_s) \\ &\quad - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})(v_d^2 - v_s^2)\} \end{aligned} \tag{F.5}$$

which reduces to the ideal linear relationship

$$I_d = 2K(V_C - V_T)v_{ds} \tag{F.6}$$

where

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V_B} \tag{F.7}$$

Alternatively, using the drain current expression of Eqn $(D.16)$ and assuming the cubic term is zero,

$$I_d = 2K[(v_g - V_{FB} - \phi_B - \gamma\sqrt{\phi_B + v_{sb}})v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb}}})v_{ds}^2] \quad \text{(F.8)}$$

Since

$$v_{sb} = v_s - v_b = -V_B - \frac{v_{ds}}{2} \quad \text{(F.9)}$$

Substituting $(F.2)$ and $(F.9)$ into $(F.8)$, the drain current is

$$\begin{aligned} I_d = {} & 2K[(V_C + \frac{v_d + v_s}{2} - V_{FB} - \phi_B - \gamma\sqrt{\phi_B - V_B - \frac{v_{ds}}{2}})v_{ds} \\ & - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B - \frac{v_{ds}}{2}}})v_{ds}^2] \end{aligned} \quad \text{(F.10)}$$

Expanding the square root term and ignoring the third and higher order terms, the current is obtained as

$$\begin{aligned} I_d \approx {} & 2K\{[V_C + \frac{v_d + v_s}{2} - V_{FB} - \phi_B - \gamma\sqrt{\phi_B - V_B} + \frac{\gamma v_{ds}}{4\sqrt{\phi_B - V_B}}]v_{ds} \\ & - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B - V_B}})v_{ds}^2\} \end{aligned} \quad \text{(F.11)}$$

Simplifying $(F.11)$ gives a expression which is identical to $(F.6)$. It can be seen that the non-saturation drain current expressions $(D.9)$ and $(D.16)$ are consistent.

Appendix G

Analysis of Parallel-Form Resistor Based on Simplified Level-2 Non-Saturation Drain-Current Equation

The main purpose of this Appendix is to derive the current expression for the gate-bulk compensated parallel form resistor with mobility degradation effect taken into account. The equation will be based on the simplified Level-2 equation as described in the Appendix D. The basic structure of the parallel form resistor is shown in Fig. 2.9. It should be noted that the buffer is based on the LSB proposed by VanPeteghem and Rice as depicted in Fig. 2.8. Assume the bias current in the LSB is I_{Bp} and all the transistors are identical and matched. The upper current (Eqn (D.16)) of the PFR is given by

$$I_1 = 2K_1[(v_{g1s} - V_{t1})v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb1}}})v_{ds}^2 + \frac{\gamma v_{ds}^3}{24(\phi_B + v_{sb1})^{\frac{3}{2}}}] \quad (G.1)$$

with

$$K_1 = \frac{K_{op}}{1+\theta(v_{g1s} - V_{t1})} \tag{G.2}$$

$$v_{g1s} = V_C' + v_{ds} \tag{G.3}$$

$$v_{sb1} = -V_B' - v_{ds} \tag{G.4}$$

$$V_C' = \sqrt{\frac{I_{Bp}}{K_p'}} + V_T \tag{G.5}$$

$$V_B' = \sqrt{\frac{I_{Bp}}{K_p'}} + V_{TO} \tag{G.6}$$

$$K_p' = \frac{K_{op}}{1+\theta\sqrt{\frac{I_{Bp}}{K_p'}}} \tag{G.7}$$

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V_B'} \tag{G.8}$$

$$V_{t1} = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V_B' - v_{ds}} \tag{G.9}$$

where K_{op} is the transconductance parameter of the PFR at zero mobility effect and the remaining symbols have been defined in the Appendix A.

Substituting $(G.2)$-$(G.9)$ into $(G.1)$,

$$\begin{aligned} I_1 \approx\ & 2K_p'[\sqrt{\frac{I_{Bp}}{K_p'}}v_{ds} + \frac{1}{2}(1+\delta_{Bp})v_{ds}^2 - \theta_p(1+\delta_{Bp})\sqrt{\frac{I_{Bp}}{K_p'}}v_{ds}^2 \\ & - \frac{1}{2}\theta_p(1+\delta_{Bp})^2 v_{ds}^3 + \frac{\gamma v_{ds}^3}{24(\phi_B + \sqrt{\frac{I_{Bp}}{K_p'}} + V_{TO})^{\frac{3}{2}}}] \end{aligned} \tag{G.10}$$

where

$$\theta_p = \frac{\theta}{1+\theta\sqrt{\frac{I_{Bp}}{K_p'}}} \tag{G.11}$$

$$\delta_{Bp} = \frac{\gamma}{2\sqrt{\phi_B + \sqrt{\frac{I_{Bp}}{K_p'}} + V_{TO}}} \tag{G.12}$$

and the cross-product terms in $\theta\gamma$ are neglected in the analysis. Similarly, the lower branch current for the PFR is given by

$$I_2 = 2K_2[(v_{g2s} - V_{t2})v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb2}}})v_{ds}^2 + \frac{\gamma v_{ds}^3}{24(\phi_B + v_{sb2})^{\frac{3}{2}}}] \tag{G.13}$$

where

$$K_2 = \frac{K_{op}}{1+\theta(v_{g2s} - V_{t2})} \quad (G.14)$$

$$v_{g2s} = V'_C \quad (G.15)$$

$$v_{sb2} = -V'_B \quad (G.16)$$

$$V_{t2} = V_T \quad (G.17)$$

Substituting $(G.14)$-$(G.17)$ into $(G.13)$ and using the definition of $(G.5)$-$(G.8)$,

$$I_2 \approx 2K'_p[\sqrt{\frac{I_{Bp}}{K'_p}}v_{ds} - \frac{1}{2}(1+\delta_{Bp})v_{ds}^2 + \frac{\gamma v_{ds}^3}{24(\phi_B + \sqrt{\frac{I_{Bp}}{K'_p}} + V_{TO})^{\frac{3}{2}}}] \quad (G.18)$$

Therefore, summation of the two branch currents gives

$$I_p = I_1 + I_2 \approx 4K'_p[\sqrt{\frac{I_{Bp}}{K'_p}}v_{ds} - \frac{1}{2}\theta_p(1+\delta_{Bp})\sqrt{\frac{I_{Bp}}{K'_p}}v_{ds}^2 \quad (G.19)$$

$$- \frac{1}{4}\theta_p(1+\delta_{Bp})^2 v_{ds}^3 + \frac{\gamma v_{ds}^3}{24(\phi_B + \sqrt{\frac{I_{Bp}}{K'_p}} + V_{TO})^{\frac{3}{2}}}]$$

Appendix H

Analysis of Series-Pair Resistors Based on Simplified Level-2 Non-Saturation Drain-Current Equation

This Appendix provides the mobility analysis of the gate-bulk compensated series pair resistors using the simplified Level-2 drain current equation. The notation and configurations refer to Fig. 2.10 and the buffers are the VanPeteghem-Rice LSB shown in Fig. 2.8. The basic assumptions are that the LSB bias current in this group of resistors is I_{Bs} and the transistors have equal transconductance parameters.

Refer to the basic structure of SPR-I (Fig. 2.10) and the buffer of Fig. 2.8, the current expressions (using Eqn (D.16)) for transistors M1 and M2 are

$$I_{s1} = 2K_1[(v_{g1m} - V_{t1})v_{dm} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{mb1}}})v_{dm}^2 + \frac{\gamma v_{dm}^3}{24(\phi_B + v_{mb1})^{\frac{3}{2}}}] \quad (H.1)$$

$$I'_{s1} = 2K_2[(v_{g2s} - V_{t2})v_{ms} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb2}}})v_{ms}^2 + \frac{\gamma v_{ms}^3}{24(\phi_B + v_{sb2})^{\frac{3}{2}}}] \quad (H.2)$$

with

$$K_1 = \frac{K_{os}}{1 + \theta(v_{g1m} - V_{t1})} \quad (H.3)$$

$$K_2 = \frac{K_{os}}{1 + \theta(v_{g2s} - V_{t2})} \quad (H.4)$$

$$v_{g1m} = V'_C + v_{dm} \quad (H.5)$$

$$v_{g2s} = V'_C \quad (H.6)$$

$$v_{mb1} = -V'_B - v_{dm} \quad (H.7)$$

$$v_{sb2} = -V'_B \quad (H.8)$$

$$V'_C = \sqrt{\frac{I_{Bs}}{K'_s}} + V_T \quad (H.9)$$

$$V'_B = \sqrt{\frac{I_{Bs}}{K'_s}} + V_{TO} \quad (H.10)$$

$$K'_s = \frac{K_{os}}{1 + \theta\sqrt{\frac{I_{Bs}}{K'_s}}} \quad (H.11)$$

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V'_B} \quad (H.12)$$

$$V_{t1} = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V'_B - v_{dm}} \quad (H.13)$$

$$V_{t2} = V_T \quad (H.14)$$

where K_{os} is the transconductance paramater of the SPR at zero-mobility effect and the other symbols have been defined in the Appendix A. The analysis of this group of resistors is complicated by the need to establish the mid-point voltages. Since the cubic terms are small by comparison with the quadratic terms, when these are neglected, the roots of the resulting quadratic equation can be solved after setting $I_{s1} = I'_{s1}$. The mid-point voltage is obtained

$$v_m = \frac{v_d + v_s}{2} + \frac{(1 + \delta_{Bs})(1 - \theta_s\sqrt{\frac{I_{Bs}}{K'_s}})}{8\sqrt{\frac{I_{Bs}}{K'_s}}} v_{ds}^2 \quad (H.15)$$

where

$$\theta_s = \frac{\theta}{1+\theta\sqrt{\frac{I_{Bs}}{K'_s}}} \tag{H.16}$$

$$\delta_{Bs} = \frac{\gamma}{2\sqrt{\phi_B + \sqrt{\frac{I_{Bs}}{K'_s}} + V_{TO}}} \tag{H.17}$$

By substituting Eqns (H.3)-(H.17) back into Eqn (H.2),

$$I'_{s1} = I_{s1} \approx K'_s[\sqrt{\frac{I_{Bs}}{K'_s}}v_{ds} - \frac{1}{4}\theta_s(1+\delta_{Bs})\sqrt{\frac{I_{Bs}}{K'_s}}v_{ds}^2 \tag{H.18}$$
$$+\frac{1}{8}\theta_s(1+\delta_{Bs})^2v_{ds}^3 - \frac{(1+\delta_{Bs})^2v_{ds}^3}{8\sqrt{\frac{I_{Bs}}{K'_s}}} + \frac{\gamma v_{ds}^3}{96(\phi_B+\sqrt{\frac{I_{Bs}}{K'_s}}+V_{TO})^{\frac{3}{2}}}]$$

Consider the case of the SPR-II and SPR-III in Fig. 2.19. Since SPR-II is identical to SPR-III, only one analysis is required. The current flowing via M1 and M2 in SPR-III is given as

$$I_{s3} = 2K_1[(v_{gn}-V_{t1})v_{dn} - \frac{1}{2}(1+\frac{\gamma}{2\sqrt{\phi_B+v_{nb}}})v_{dn}^2 + \frac{\gamma v_{dn}^3}{24(\phi_B+v_{nb})^{\frac{3}{2}}}] \tag{H.19}$$

$$I'_{s3} = 2K_2[(v_{gs}-V_{t2})v_{ns} - \frac{1}{2}(1+\frac{\gamma}{2\sqrt{\phi_B+v_{sb}}})v_{ns}^2 + \frac{\gamma v_{ns}^3}{24(\phi_B+v_{sb})^{\frac{3}{2}}}] \tag{H.20}$$

with

$$K_1 = \frac{K_{os}}{1+\theta(v_{gn}-V_{t1})} \tag{H.21}$$

$$K_2 = \frac{K_{os}}{1+\theta(v_{gs}-V_{t2})} \tag{H.22}$$

$$v_{gn} = V'_C \tag{H.23}$$

$$v_{gs} = V'_C + v_{ns} \tag{H.24}$$

$$v_{nb} = -V'_B \tag{H.25}$$

$$v_{sb} = -V'_B - v_{ns} \tag{H.26}$$

$$V'_C = \sqrt{\frac{I_{Bs}}{K'_s}} + V_T \tag{H.27}$$

$$V'_B = \sqrt{\frac{I_{Bs}}{K'_s}} + V_{TO} \tag{H.28}$$

$$K_s' = \frac{K_{os}}{1+\theta\sqrt{\frac{I_{Bs}}{K_s'}}} \tag{H.29}$$

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V_B'} \tag{H.30}$$

$$V_{t1} = V_T \tag{H.31}$$

$$V_{t2} = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V_B' - v_{ns}} \tag{H.32}$$

Using the similar approach as discussed above, the mid-point voltage is

$$v_n = \frac{v_d + v_s}{2} - \frac{(1+\delta_{Bs})(1-\theta_s\sqrt{\frac{I_{Bs}}{K_s'}})}{8\sqrt{\frac{I_{Bs}}{K_s'}}} v_{ds}^2 \tag{H.33}$$

where θ_s and δ_{Bs} are defined in Eqns $(H.16)$ and $(H.17)$. By substituting $(H.21)$-$(H.33)$ back into $(H.19)$, we gives the relationship that $I_{s3} = I_{s2} \approx I_{s1}$.

Appendix I

Analysis of Series-Parallel Resistors Based on Simplified Level-2 Non-Saturation Drain-Current Equation

The aim of this Appendix is to describe the analysis of mobility degradation effect for a group of gate-bulk compensated series-parallel resistors (Fig. 2.11) using the VanPeteghem-Rice LSB (Fig. 2.8). The simplified Level-2 drain current equation is used. The bias current of the LSB is denoted to be I_{Bsp}. Since the upper branch current of SPQR-I is identical to the current (Eqn (H.18)) in SPR-I,

$$I_1' = I_1 \approx K_{sp}'\left[\sqrt{\frac{I_{Bs}}{K_{sp}'}}v_{ds} - \frac{1}{4}\theta_{sp}(1+\delta_{Bsp})\sqrt{\frac{I_{Bsp}}{K_{sp}'}}v_{ds}^2 + \frac{1}{8}\theta_{sp}(1+\delta_{Bsp})^2 v_{ds}^3 - \frac{(1+\delta_{Bsp})^2 v_{ds}^3}{8\sqrt{\frac{I_{Bsp}}{K_{sp}'}}} + \frac{\gamma v_{ds}^3}{96(\phi_B + \sqrt{\frac{I_{Bsp}}{K_{sp}'}} + V_{TO})^{\frac{3}{2}}}\right] \tag{I.1}$$

and

$$v_{m1} = \frac{v_d + v_s}{2} - \frac{(1+\delta_{Bsp})(1-\theta_{sp}\sqrt{\frac{I_{Bsp}}{K_{sp}'}})}{8\sqrt{\frac{I_{Bsp}}{K_{sp}'}}}v_{ds}^2 \tag{I.2}$$

with

$$K'_{sp} = \frac{K_{osp}}{1+\theta\sqrt{\frac{I_{Bsp}}{K'_{sp}}}} \tag{I.3}$$

$$\theta_{sp} = \frac{\theta}{1+\theta\sqrt{\frac{I_{Bsp}}{K'_{sp}}}} \tag{I.4}$$

$$\delta_{Bsp} = \frac{\gamma}{2\sqrt{\phi_B + \sqrt{\frac{I_{Bsp}}{K'_{sp}}} + V_{TO}}} \tag{I.5}$$

where K_{osp} is the transconductance parameter for the matched transistors at zero mobility effect. The other symbols are described in the Appendix A.

The lower branch currents (Eqn (D.16)) in SPQR-I are

$$I_2 = 2K_3[(v_{g3m2} - V_{t3})v_{dm2} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{m2b3}}})v_{dm2}^2 + \frac{\gamma v_{dm2}^3}{24(\phi_B + v_{m2b3})^{\frac{3}{2}}}] \tag{I.6}$$

$$I'_2 = 2K_4[(v_{g3s} - V_{t4})v_{m2s} - \frac{1}{2}(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb3}}})v_{m2s}^2 + \frac{\gamma v_{m2s}^3}{24(\phi_B + v_{sb3})^{\frac{3}{2}}}] \tag{I.7}$$

with

$$K_3 = \frac{K_{os}}{1+\theta(v_{g3m2} - V_{t3})} \tag{I.8}$$

$$K_4 = \frac{K_{os}}{1+\theta(v_{g3s} - V_{t4})} \tag{I.9}$$

$$v_{g3m2} = V'_C + v_{m1} - v_{m2} \tag{I.10}$$

$$v_{g3s} = V'_C + v_{m1} - v_s \tag{I.11}$$

$$v_{m2b3} = -V'_B - v_{m1} + v_{m2} \tag{I.12}$$

$$v_{sb3} = -V'_B - v_{m1} + v_s \tag{I.13}$$

$$V'_C = \sqrt{\frac{I_{Bsp}}{K'_{sp}}} + V_T \tag{I.14}$$

$$V'_B = \sqrt{\frac{I_{Bsp}}{K'_{sp}}} + V_{TO} \tag{I.15}$$

$$K'_{sp} = \frac{K_{osp}}{1+\theta\sqrt{\frac{I_{Bsp}}{K'_{sp}}}} \tag{I.16}$$

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V'_B} \tag{I.17}$$

$$V_{t3} = V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V'_B - v_{m1} + v_{m2}} \tag{I.18}$$

$$V_{t4} \;=\; V_{FB} + \phi_B + \gamma\sqrt{\phi_B - V_B' - v_{m1} + v_s} \qquad \text{(I.19)}$$

Following the assumption as discussed in Appendix G, the mid-point voltage is obtained as

$$v_{m2} = \frac{v_d + v_s}{2} - \frac{(1+\delta_{Bsp})(1-\theta_{sp}\sqrt{\frac{I_{Bsp}}{K'_{sp}}})}{8\sqrt{\frac{I_{Bsp}}{K'_{sp}}}} v_{ds}^2 \qquad \text{(I.20)}$$

where θ_{sp} and δ_{Bsp} are defined by Eqns $(I.4)$ and $(I.5)$. Substituting $(I.2)$ and $(I.8) - (I.20)$ into $(I.7)$,

$$\begin{aligned} I_2' = I_2 \;\approx\; & K'_{sp}[\sqrt{\frac{I_{Bs}}{K'_{sp}}} v_{ds} - \frac{1}{4}\theta_{sp}(1+\delta_{Bsp})\sqrt{\frac{I_{Bsp}}{K'_{sp}}} v_{ds}^2 \\ & - \frac{1}{4}\theta_{sp}(1+\delta_{Bsp})^2 v_{ds}^3 + \frac{(1+\delta_{Bsp})^2 v_{ds}^3}{8\sqrt{\frac{I_{Bsp}}{K'_{sp}}}} + \frac{\gamma v_{ds}^3}{96(\phi_B + \sqrt{\frac{I_{Bsp}}{K'_{sp}}} + V_{TO})^{\frac{3}{2}}}] \end{aligned} \qquad \text{(I.21)}$$

Therefore, the addition of two branch currents gives

$$\begin{aligned} I_{sp1} = I_1' + I_2' \;\approx\; & 2K'_{sp}[\sqrt{\frac{I_{Bs}}{K'_{sp}}} v_{ds} - \frac{1}{4}\theta_{sp}(1+\delta_{Bsp})\sqrt{\frac{I_{Bsp}}{K'_{sp}}} v_{ds}^2 \\ & - \frac{1}{16}\theta_{sp}(1+\delta_{Bsp})^2 v_{ds}^3 + \frac{\gamma v_{ds}^3}{96(\phi_B + \sqrt{\frac{I_{Bsp}}{K'_{sp}}} + V_{TO})^{\frac{3}{2}}}] \end{aligned} \qquad \text{(I.22)}$$

Consider the SPQR-II and SPQR-III of Fig. 2.11, their mid-point voltages are common mode signals. Using the result of $(G.19)$, the current expression is obtained as $I_{sp2} = I_{sp3} \approx I_{sp1}$.

Appendix J

Analytical Expressions of Dual Gate-Bulk Compensation Resistors Based on Simplified Level-3 Non-Saturation Drain-Current Equation

This Appendix examines the mobility effect on the group of dual gate-bulk compensated resistors (PFR, SPR and SPQR) using simplified Level-3 non-saturation drain current expression [87]. The simplication ignores channel-length modulation, narrow-width effect and velocity saturation. The main reason for introducing these closed form expressions is because the Plessey models (Appendix B-C) supplied for the simulations are Level-3 based rather than Level-2. For comparison, the symbols adopted in this Appendix are based on Appendix G-I. The analysis approach is the same and is not repeated here.

Consider the simplified Level-3 non-saturation drain current in a MOSFET given [81] by

$$I_d = 2K[(v_{gs} - V_t)v_{ds} - \frac{1}{2}(1 + \frac{\gamma}{4\sqrt{\phi_B + v_{sb}}})v_{ds}^2] \tag{J.1}$$

where

$$V_t = V_{FB} + \phi_B + \gamma\sqrt{\phi_B + v_{sb}} \tag{J.2}$$

By comparison with the simplified Level-2 drain current Eqn (D.16), it can be seen that the linear term is the same but the gamma-related quadratic term is reduced by a factor of two. This error in the model is accomodated by changing the empirical value in the modelling used to fit the experimental data. Furthermore, the cubic term is absent in this Level-3 expression.

With reference to the PFR and LSB as shown in Fig. 2.9 and Fig. 2.8, respectively, the current obtained from the Level-3 equation (J.1) is

$$\begin{aligned} I_p \approx\ & 4K_p'\{\sqrt{\frac{I_{Bp}}{K_p'}}v_{ds} + [\frac{\delta_{Bp}}{4} - \frac{1}{2}\theta_p(1+\delta_{Bp})\sqrt{\frac{I_{Bp}}{K_p'}}]v_{ds}^2 \\ & - \frac{1}{4}\theta_p(1+\delta_{Bp})v_{ds}^3 + \frac{\gamma v_{ds}^3}{32(\phi_B + \sqrt{\frac{I_{Bp}}{K_p'}} + V_{TO})^{\frac{3}{2}}}\} \end{aligned} \tag{J.3}$$

where the symbols are defined in the Appendix G.

The current expression for the SPR-I of Fig. 2.10 is

$$\begin{aligned} I_{s1}' = I_{s1} \approx\ & K_s'\{\sqrt{\frac{I_{Bs}}{K_s'}}v_{ds} + [\frac{\delta_{Bs}}{8} - \frac{1}{4}\theta_s(1+\delta_{Bs})\sqrt{\frac{I_{Bs}}{K_s'}}]v_{ds}^2 \\ & + \frac{1}{8}\theta_s(1+\delta_{Bs})(1+\frac{\delta_{Bs}}{2})v_{ds}^3 - \frac{(1+\delta_{Bs})(1+\frac{\delta_{Bs}}{2})v_{ds}^3}{8\sqrt{\frac{I_{Bs}}{K_s'}}}\} \end{aligned} \tag{J.4}$$

where the symbols are defined in the Appendix H. Similar result is also obtained for the SPR-II and SPR-III that $I_{s3} = I_{s2} \approx I_{s1}$. It should be noted the mid-point voltages expressions derived from this analysis are the same as those described in the Appendix H.

The current expression for the SPQR-I is

$$I_{sp1} \approx 2K'_{sp}\{\sqrt{\frac{I_{Bs}}{K'_{sp}}}v_{ds} + [\frac{\delta_{Bsp}}{8} - \frac{1}{4}\theta_{sp}(1+\delta_{Bsp})\sqrt{\frac{I_{Bsp}}{K'_{sp}}}]v_{ds}^2 - \frac{1}{16}\theta_{sp}(1+\delta_{Bsp})(1+\frac{3}{2}\delta_{Bsp})v_{ds}^3 + \frac{\gamma v_{ds}^3}{128(\phi_B + \sqrt{\frac{I_{Bsp}}{K'_{sp}}} + V_{TO})^{\frac{3}{2}}}\} \quad (J.5)$$

where the symbols are defined in the Appendix I.

Consider the case of the SPQR-II and SPQR-III, it can be shown that

$$I_{sp2} = I_{sp3} \approx 2K'_{sp}\{\sqrt{\frac{I_{Bs}}{K'_{sp}}}v_{ds} + [\frac{\delta_{Bsp}}{8} - \frac{1}{4}\theta_{sp}(1+\delta_{Bsp})\sqrt{\frac{I_{Bsp}}{K'_{sp}}}]v_{ds}^2 - \frac{1}{16}\theta_{sp}(1+\delta_{Bsp})v_{ds}^3 + \frac{\gamma v_{ds}^3}{128(\phi_B + \sqrt{\frac{I_{Bsp}}{K'_{sp}}} + V_{TO})^{\frac{3}{2}}}\} \quad (J.6)$$

The mid-point voltages are also the same as those described in the Appendix I.

Appendix K

Analysis of the Long-Tail Differential Pair

This objective of this Appendix is to derive an analytical expression for the current in the long tail differential pair (LTP) with mobility degradation effect taken into account. The fundamental equation is based on the simplified Level-3 saturation drain current expression (E.13) including both mobility degradation and drain current correction factors but excluding the velocity saturation and channel-length modulation effects. Finally, a linear transconductance expression and third harmonic distortion expression are presented. It should be noted that these new closed form expressions [54] provides better estimates than the standard equations [47],[60].

Consider the differential pair MA1-MA2 under steady state conditions as shown in both Fig. 4.1 and Fig. 4.2; the quiescent drain current for the transistors can be expressed as

$$I = \frac{K_{oc}}{1 + \theta(V_{GS} - V_{TO})}(V_{GS} - V_{TO})^2 \tag{K.1}$$

where

$$K_{oc} = \frac{K_o}{1+\delta} \tag{K.2}$$

is the effective transconductance parameter and $\delta = \gamma/4\sqrt{\phi + v_{sb}}$ is the drain current correction factor. The parameters as shown have been defined in the Appendix A.

Eqn $(K.1)$ can be solved for the quiescient gate-to-source overdrive as

$$V_b = V_{GS} - V_{TO} = \frac{\theta I}{2K_{oc}} + \sqrt{\frac{I}{K_{oc}}(1 + \frac{\theta^2 I}{4K_{oc}})} \tag{K.3}$$

in which case,

$$V_Q = -V_{GS} = -(V_b + V_{TO}). \tag{K.4}$$

To quantify the nonlinearity v_n, consider the drain currents under ac conditions; they are

$$I_1 = \frac{K_{oc}}{1+\theta(v_{gs1} - V_{TO})}(v_{gs1} - V_{TO})^2 \tag{K.5}$$

$$I_2 = \frac{K_{oc}}{1+\theta(v_{gs2} - V_{TO})}(v_{gs2} - V_{TO})^2 \tag{K.6}$$

where

$$v_{gs1} = v_1 - v_c - V_Q - v_n = \frac{V_{in}}{2} + V_b - v_n + V_{TO} \tag{K.7}$$

$$v_{gs2} = v_2 - v_c - V_Q - v_n = -\frac{V_{in}}{2} + V_b - v_n + V_{TO} \tag{K.8}$$

with

$$V_{in} = v_1 - v_2 \tag{K.9}$$

and

$$v_c = \frac{v_1 + v_2}{2} \tag{K.10}$$

Given

$$I_1 + I_2 = 2I \tag{K.11}$$

an approximation to v_n can be obtained as

$$v_n \approx \frac{1}{4V_b(1+\theta V_b)(2+\theta V_b)} v_i^2 + higher \ \ order \ \ terms \ \ in \ \ v_i^2 \qquad \text{(K.12)}$$

Thus the constant sum nature of the drain currents is reflected in the generation of a nonlinear potential v_n comprizing an infinite series of terms in v_i^2 of which we retain only the first.

Subtracting $(K.6)$ from $(K.5)$ and solving for the signal current gives

$$I_o = I_1 - I_2 = G_1 V_{in} + G_3 V_{in}^3 \qquad \text{(K.13)}$$

where

$$G_1 = \frac{(2+\theta V_b)}{(1+\theta V_b)^2} K_{oc} V_b \qquad \text{(K.14)}$$

$$G_3 = -\frac{1+(1+\theta V_b)^2}{(2+\theta V_b)(1+\theta V_b)^4} \frac{K_{oc}}{4V_b} \qquad \text{(K.15)}$$

The resulting harmonic distortion which can be defined[1] for the sinusoidal signal: $v_i = V_p sinwt$ as

$$HD3 = \frac{1}{4} | \frac{G_3}{G_1} | V_p^2 \times 100\% \qquad \text{(K.16)}$$

can be written in the form

$$HD3 = \frac{1 + \frac{1}{(1+\theta \mathrm{V_b})^2}}{(2+\theta \mathrm{V_b})^2} [\frac{V_p}{4V_b}]^2 \times 100\% \qquad \text{(K.17)}$$

and reduces to the "standard" [36,[49] estimate

$$HD3 = \frac{K_o}{32I} V_p^2 \times 100\% \qquad \text{(K.18)}$$

on setting θ and δ to 0.

[1]This definition ignores the relatively small contribution to the fundamental from the expansion of the cubic term.

Appendix L

Analysis of the Anti-Phase Common-Source Pair

This Appendix presents a mobility analysis for an anti-phase driven differential pair (ACSP). The notations refer to Fig. 4.6 and the basic assumptions are those given in Appendix K. Closed form expressions for the linear transconductance and third harmonic distortion are given. It should be noted the analytical expressions also apply equally well to the CCSP (because the common-mode signal is generated at the common source node, results in a similar antiphase drive to the transistor pair.)

With reference to Fig. 4.6, the quiescent drain current for the transistor pair MD1-MD2 can be expressed as

$$I = \frac{K_{oc}}{1 + \theta(V_{GS} - V_{TO})}(V_{GS} - V_{TO})^2 \qquad \text{(L.1)}$$

where

$$K_{oc} = \frac{K_o}{1 + \delta} \qquad \text{(L.2)}$$

is the effective transconductance parameter and $\delta = \gamma/4\sqrt{\phi + v_{sb}}$ is the drain current correction factor. Note that the parameters are defined in Appendix A.

Eqn $(L.1)$ can be solved for the quiescent gate-to-source overdrive as

$$V_b = V_{GS} - V_{TO} = \frac{\theta I}{2K_{oc}} + \sqrt{\frac{I}{K_{oc}}(1 + \frac{\theta^2 I}{4K_{oc}})} \quad \text{(L.3)}$$

in which case,

$$V_Q = -V_{GS} = -(V_b + V_{TO}). \quad \text{(L.4)}$$

Consider the drain currents under ac conditions; the drain currents become

$$I_1 = \frac{K_{oc}}{1 + \theta(v_{gs1} - V_{TO})}(v_{gs1} - V_{TO})^2 \quad \text{(L.5)}$$

$$I_2 = \frac{K_{oc}}{1 + \theta(v_{gs2} - V_{TO})}(v_{gs2} - V_{TO})^2 \quad \text{(L.6)}$$

where

$$v_{gs1} = v_1 - v_c - V_Q = \frac{V_{in}}{2} + V_b + V_{TO} \quad \text{(L.7)}$$

$$v_{gs2} = v_2 - v_c - V_Q = -\frac{V_{in}}{2} + V_b + V_{TO} \quad \text{(L.8)}$$

with

$$V_{in} = v_1 - v_2 \quad \text{(L.9)}$$

and

$$v_c = \frac{v_1 + v_2}{2} \quad \text{(L.10)}$$

Subtracting $(L.6)$ from $(L.5)$ and gives the output signal current

$$I_o = I_1 - I_2 = G_1 V_{in} + G_3 V_{in}^3 \quad \text{(L.11)}$$

where

$$G_1 = \frac{(2 + \theta V_b)}{(1 + \theta V_b)^2} K_{oc} V_b \quad \text{(L.12)}$$

and

$$G_3 = -\frac{\theta K_{oc}}{4(1 + \theta V_b)^4} \quad \text{(L.13)}$$

For the sinusoidal signal: $v_i = V_p sinwt$, the third-harmonic distortion is predicted as

$$HD3 = \frac{\theta}{16V_b(2+\theta V_b)(1+\theta V_b)^2} V_p^2 \times 100\% \tag{L.14}$$

Appendix M

Analysis of the Cross-Coupled Pair

This Appendix presents a mobility analysis for the cross-coupled pair (CCP). The notations refer to Fig. 4.4 and the basic assumptions are those given in Appendix K. Closed form expressions for the linear transconductance and third harmonic distortion are given.

With reference to Fig. 4.4, the quiescent drain current for the transistor pair MC1-MC2 can be expressed as

$$I' = \frac{K'_{oc}}{1 + \theta(V_{GS} - V_{TO})}(V_{GS} - V_{TO})^2 \tag{M.1}$$

with

$$K'_{oc} = \frac{K'_o}{1 + \delta} \tag{M.2}$$

is the effective transconductance parameter and $\delta = \gamma/4\sqrt{\phi + v_{sb}}$ is the drain current correction factor. The drain current I' and zero gate field transconductance parameter K'_o defined in this Appendix is different with that of the attributes used in LTP, CCSP and ACSP. The remaining parameters are defined in Appendix A.

Eqn $(M.1)$ can be solved for the quiescent gate-to-source overdrive as

$$V_b' = V_{GS} - V_{TO} = \frac{\theta I}{2K_{oc}'} + \sqrt{\frac{I'}{K_{oc}'}(1 + \frac{\theta^2 I'}{4K_{oc}'})} \tag{M.3}$$

in which case,

$$V_Q' = -V_{GS} = -(V_b' + V_{TO}). \tag{M.4}$$

Consider the drain currents under ac conditions; the drain currents become

$$I_1 = \frac{K_{oc}'}{1 + \theta(v_{gs1} - V_{TO})}(v_{gs1} - V_{TO})^2 \tag{M.5}$$

$$I_2 = \frac{K_{oc}'}{1 + \theta(v_{gs2} - V_{TO})}(v_{gs2} - V_{TO})^2 \tag{M.6}$$

where

$$v_{gs1} = v_1 - v_c - V_Q = \frac{V_{in}}{2} + V_b' + V_{TO} \tag{M.7}$$

$$v_{gs2} = v_2 - v_c - V_Q = -\frac{V_{in}}{2} + V_b' + V_{TO} \tag{M.8}$$

with

$$V_{in} = v_1 - v_2 \tag{M.9}$$

and

$$v_c = \frac{v_1 + v_2}{2} \tag{M.10}$$

Subtracting $(M.6)$ from $(M.5)$ and gives the output signal current

$$I_o = I_1 - I_2 = G_1 V_{in} + G_3 V_{in}^3 \tag{M.11}$$

where

$$G_1 = \frac{(2 + \theta V_b')}{(1 + \theta V_b')^2} 2K_{oc}' V_b' \tag{M.12}$$

and

$$G_3 = -\frac{2\theta K_{oc}'}{(1 + \theta V_b')^4} \tag{M.13}$$

In order to compare with the LTP, CCSP and ACSP at the same transconductance and for the same bias conditions, the criteria can be fulfilled if $I' = I/2$ and $K'_o = K_o/2$. Thus Eqns $(M.12)$ and $(M.13)$ become

$$G_1 = \frac{(2+\theta V_b)}{(1+\theta V_b)^2} K_{oc} V_b \tag{M.14}$$

and

$$G_3 = -\frac{\theta K_{oc}}{(1+\theta V_b)^4} \tag{M.15}$$

For the sinusoidal signal: $v_i = V_p sinwt$, the third-harmonic distortion is predicted as

$$HD3 = \frac{\theta}{4V_b(2+\theta V_b)(1+\theta V_b)^2} V_p^2 \times 100\% \tag{M.16}$$

Appendix N

Analysis of the Offset-Biased Cross-Coupled Pair

This Appendix presents the analysis for the offset-biased cross-coupled pair (OBCCP) including the mobility degradation effect. The symbols refer to Fig. 4.8 and Fig. 4.9. The second-order effect assumptions are those given in Appendix K. Closed form expressions for the linear transconductance and third harmonic distortion are given.

With reference to Fig. 4.8, it is assumed that the transistors ME1-ME2 have identical transconductance K_{oc} to those in the LTP, CCSP and ACSP in Appendix K-L. The transconductance and the tail currents in the series-connected differential pairs are defined as K_t and I_t respectively. Thus, the quiescent drain current for the transistor pair ME1-ME2 can be expressed as

$$I = \frac{K_{oc}}{1+\theta(V_{GS}-V_{TO})}(V_{GS}-V_{TO})^2 \tag{N.1}$$

where

$$K_{oc} = \frac{K_o}{1+\delta} \tag{N.2}$$

is the effective transconductance parameter and $\delta = \gamma/4\sqrt{\phi + v_{sb}}$ is the drain current correction factor. Note that the parameters are defined in Appendix A.

The quiescient gate-to-source overdrive is given

$$V_b'' = V_{GS} - V_{TO} = V_B - V_Q'' - V_{TO} \tag{N.3}$$

in which case,

$$V_Q'' = -(\sqrt{\frac{I_t}{K_t}} + V_{TO}) \tag{N.4}$$

Consider the drain currents under ac conditions; the drain currents become

$$I_1 = \frac{K_{oc}}{1 + \theta(v_{gs1} - V_{TO})}(v_{gs1} - V_{TO})^2 \tag{N.5}$$

$$I_2 = \frac{K_{oc}}{1 + \theta(v_{gs2} - V_{TO})}(v_{gs2} - V_{TO})^2 \tag{N.6}$$

where

$$v_{gs1} = v_a - v_b + V_B - V_Q'' = \frac{V_{in}}{2} + V_b + V_{TO} \tag{N.7}$$

$$v_{gs2} = v_a - v_b + V_B - V_Q'' = -\frac{V_{in}}{2} + V_b + V_{TO} \tag{N.8}$$

with

$$V_{in} = v_1 - v_2 \tag{N.9}$$

and

$$v_a = \frac{3}{4}v_1 + \frac{1}{4}v_2 + v_n \tag{N.10}$$

$$v_b = \frac{1}{4}v_1 + \frac{3}{4}v_2 + v_n \tag{N.11}$$

$$v_n = \sqrt{\frac{I_t}{K_t}}(1 - \sqrt{1 - \frac{K_t V_{in}^2}{8I_t}}) \tag{N.12}$$

Subtracting $(N.6)$ from $(N.5)$ and gives the output signal current

$$I_o = I_1 - I_2 = G_1 V_{in} + G_3 V_{in}^3 \tag{N.13}$$

where

$$G_1 = \frac{(2 + \theta V_b'')}{(1 + \theta V_b'')^2} K_{oc} V_b'' \tag{N.14}$$

and

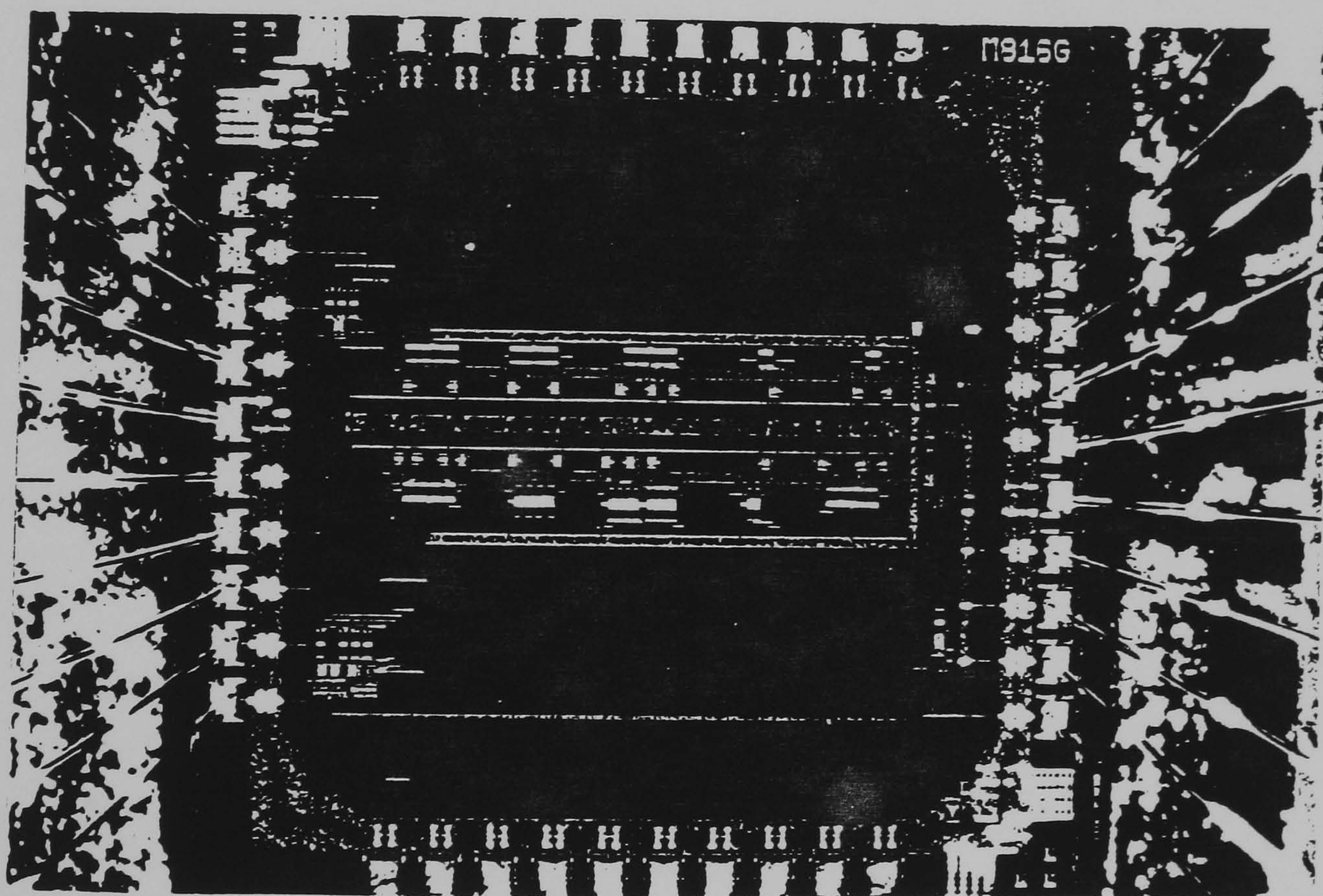
$$G_3 = -\frac{\theta K_{oc}}{4(1 + \theta V_b'')^4} \tag{N.15}$$

For the sinusoidal signal: $v_i = V_p sinwt$, the third-harmonic distortion is predicted as

$$HD3 = \frac{\theta}{16V_b''(2 + \theta V_b'')(1 + \theta V_b'')^2} V_p^2 \times 100\% \tag{N.16}$$

Appendix O

Microphotograph of a Complete Chip



Appendix P

Published Papers

NOVEL VOLTAGE-CONTROLLED GROUNDED RESISTOR

Indexing terms: Circuit theory and design, Resistors, MOS structures and devices, Filters

The letter presents a new tunable grounded resistor in which a single MOS transistor, operating in the triode region, is linearised via feedback of the drain/source potentials to the gate terminal. Preliminary simulation results show that a biquadratic section realised using the proposed resistor would exhibit less than 0·4% total harmonic distortion (THD) for input signals of 1 V_{pp}, increasing to 1% for 4 V_{pp} inputs.

Introduction: The direct implementation of resistors in analogue MOS circuits is usually avoided because of accuracy limitations, low sheet resistance and poor utilisation of die area. By contrast, the operation of a MOS transistor in its triode region offers an economic and controllable resistance. However, the strong nonlinearity of the MOSFET prohibits the use of large signals, and several circuit techniques for improving linearity have been reviewed in the literature.[1-4] In Reference 2 linearisation is economically achieved by two parallel connected MOS transistors. In practice, however, this technique suffers from potentially serious drawbacks in that the gate voltages applied to the transistors are different, resulting in different degrees of mobility degradation and thus to errors in the cancellation of distortion components.

In this letter the linearisation of a single device via terminal voltage feedback is described. The proposed arrangement essentially replaces the nonadjustable resistor-based approach, suggested by Bilotti,[5] with a voltage-controllable VLSI-compatible network.

Linearisation technique: The drain current of an *n*-channel MOS transistor in nonsaturation is given by[6]

$$I_D = K\{(V_G - V_B - V_{FB} - \phi_B)(V_D - V_S) - \tfrac{1}{2}[(V_D - V_B)^2 - (V_S - V_B)^2] - \tfrac{2}{3}\gamma[(V_D - V_B + \phi_B)^{3/2} - (V_S - V_B + \phi_B)^{3/2}]\} \quad (1a)$$

where

$$K = \mu \frac{W}{L} C_{ox} \qquad \gamma = \frac{1}{C_{ox}} \sqrt{(2qN_A\varepsilon_s)} \quad (1b)$$

Expanding the (3/2)th power terms in eqn. 1*a* in a Taylor series results in the quadratic approximation to I_D as follows:

$$I_D = K\left[(V_G - V_T)(V_D - V_S) - \frac{m}{2}(V_D^2 - V_S^2)\right] \quad (2a)$$

where

$$m = 1 + \frac{\gamma}{2\sqrt{(\phi_B - V_B)}} \qquad V_T = V_{FB} + \phi_B + \gamma\sqrt{(\phi_B - V_B)} \quad (2b)$$

These expressions show that the dominant nonlinearity term can be minimised by applying to the gate terminal a potential which results in the cancellation of the terms in V_D^2 and V_S^2, namely

$$V_G = V_C + \frac{m}{2}(V_D + V_S) \quad (3)$$

Thus the equivalent drain source resistance is obtained as

$$R = [K(V_C - V_T)]^{-1} \quad (4)$$

and is independently controllable via V_C.

Grounded voltage-controlled resistor (GVCR): As eqn. 3 shows, distortion in a floating MOSFET resistor can be minimised by applying a suitably weighted sum of the source and drain potential to the gate. In the particular case where the source terminal is maintained at ground potential, the gate voltage required for control and linearisation purposes reduces to $V_G = V_C + (m/2)V_D$.

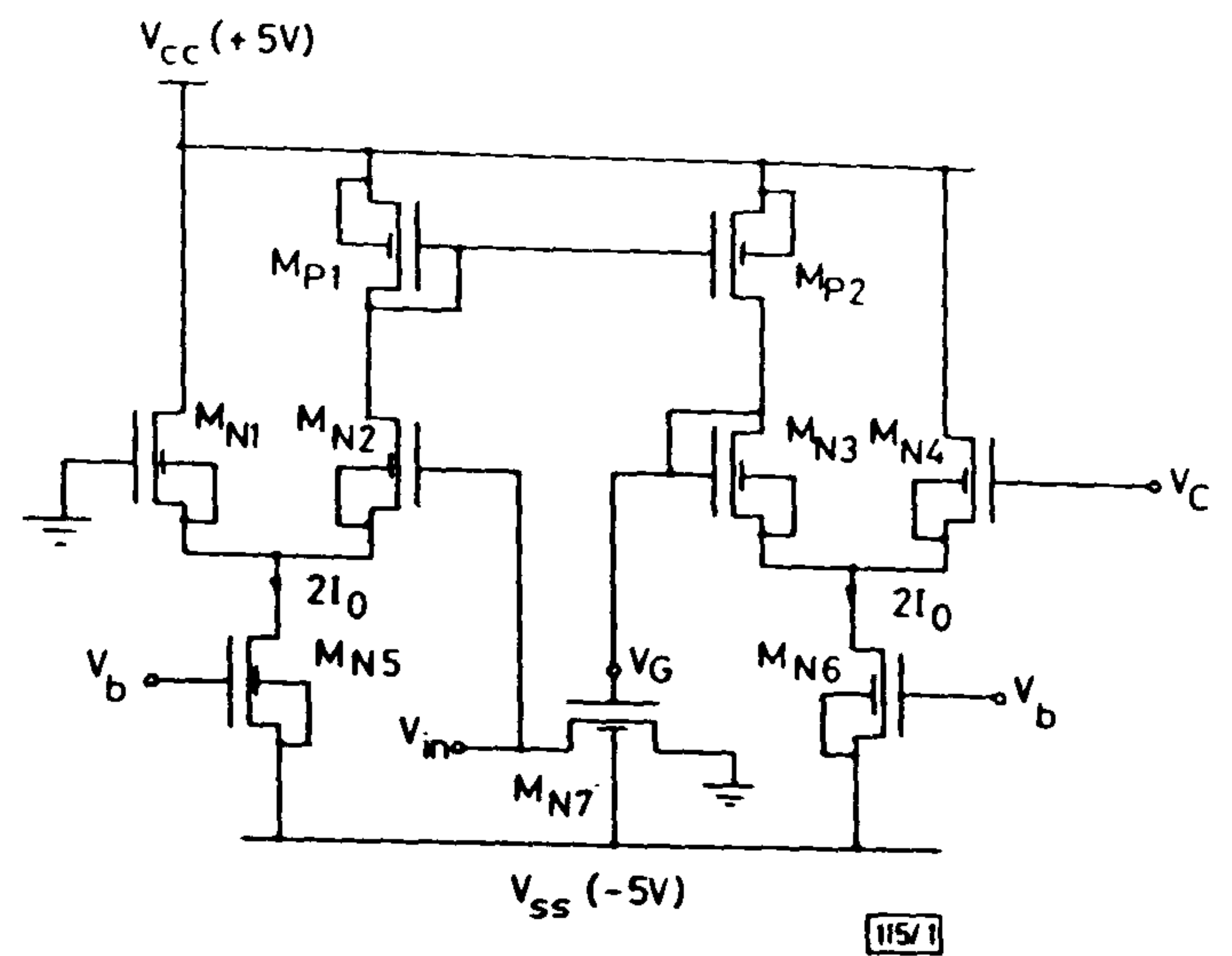


Fig. 1 *Grounded voltage-controlled resistor*

Fig. 1 shows the circuit diagram for a GVCR in which V_G is generated using the 'inverse function approach',[7] and controls/linearises transistor M_{N7}.

The circuit essentially consists of two sections: 'drive' and 'copy'. The 'drive' section is formed by transistors M_{N1}, M_{N2}, M_{N5} and M_{P1} whereas the 'copy' section is formed by transistors M_{N3}, M_{N4}, M_{N6} and M_{P2}. Transistors M_{N1}–M_{N4} constitute two differential pairs with equal tail currents $2I_0$. By means of the *p*-channel current mirror M_{P1}–M_{P2}, the voltage V_{in} is copied to the scaled differential pair M_{N3}–M_{N4}, yielding the required weighted voltage.

Since the differential pair structure offers an extremely high input impedance, the loading effect on the controlled transistor (M_{N7}) is much reduced,[5] and resistance values in the MΩ range are readily available.

It may also be noted that the extension of this technique to floating resistors, involving the feedback of V_D and V_S, would increase the quiescent power consumption and complexity, but is entirely straightforward.

Simulation results: SPICE simulations of the basic GVCR and its application as the resistive elements in the familiar two-integrator-loop biquadratic filter section have been performed. The results were obtained using realistic level 3 models (with gate-voltage-dependent mobility) for all MOS devices. However, auxiliary devices, including capacitors and operational amplifiers, were assumed to be ideal.

The DC current/voltage characteristics for the GVCR of Fig. 1 are shown in Fig. 2 for a range of control voltages. This family of curves shows that the resistor offers good linearity for terminal voltage swings up to 5 V_{pp}, combined with a wide tuning range (from 60 kΩ to over 200 kΩ for this example). It may be noted that the operational range for the gate control voltage V_C is limited by the saturation conditions on M_{N5}–M_{N6} and M_{P1}–M_{P2}. With the bias supplies set at ±5 V it was found that V_C could be varied between 2·8 and 3·9 V.

As previously shown, the values for m are dependent on V_B, ϕ_B and γ and could range from 1·05 to 1·3. In the process

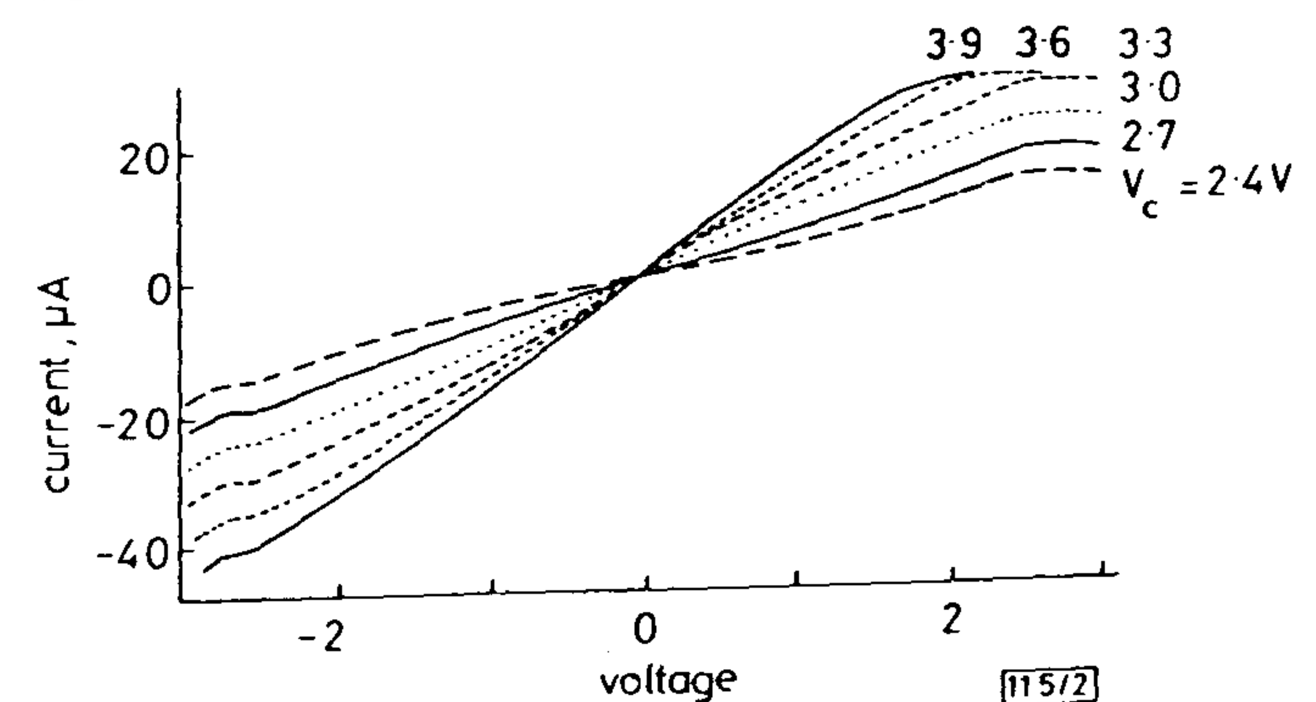


Fig. 2 *Variation of GVCR static v/i characteristics with control voltage V_C*

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considered, the model parameters employed in the n-channel transistors were $\gamma = 0.65\,V^{1/2}$, $\phi_B = 0.677\,V$ and $V_B = -5\,V$. This, it may be noted, sets $m = 1.13$ and requires the optimum K_3/K_1, K_4/K_2 ratios to be 3·1. However, simulation revealed that distortion was actually minimised with K_3/K_1 and K_4/K_2 at the lower value of 2·6. The discrepancies appear to be due to imperfections in the current-mirror (M_{P1}–M_{P2}) and the nonlinear nature of the differential pairs.

Frequency response evaluations predict a 3 dB bandwidth for the control circuitry of 3 MHz at $I_0 = 6\,\mu A$, a larger bandwidth being possible, but at the cost of increased power consumption and distortion. For example, doubling I_0 to $12\,\mu A$ gives a 3 dB bandwidth of 4·3 MHz, but increases distortion by 0·5% ($V_{in} = 1\,V_{pp}$ and $V_C = 3.2\,V$).

The aspect ratios resulting in minimum distortion were 5/50 for M_{N1}–M_{N2}, 13/50 for M_{N3}–M_{N4}, 70/10 for M_{N5}–M_{N6}, 10/50 for M_{N7} and 80/10 for M_{P1}–M_{P2}; V_{bias} was $-3.8\,V$.

Fig. 3 shows the schematic diagram for a 'biquad'-type implementation of a second-order Chebyshev lowpass function with a passband ripple of 0·5 dB and a 4·7 kHz cutoff frequency. Although this example contains six GVCRs, the presence of common inputs reduces the number of (identical) control circuits required (as embodied in Fig. 1) to only four.

Amplitude/frequency response simulations show good agreement with the design specification, and indicate that stopband attenuations in excess of 100 dB should be attainable at frequencies in the MHz range. Distortion analyses also show THD levels would typically be lower than 1% for input signals up to 4 V_{pp}.

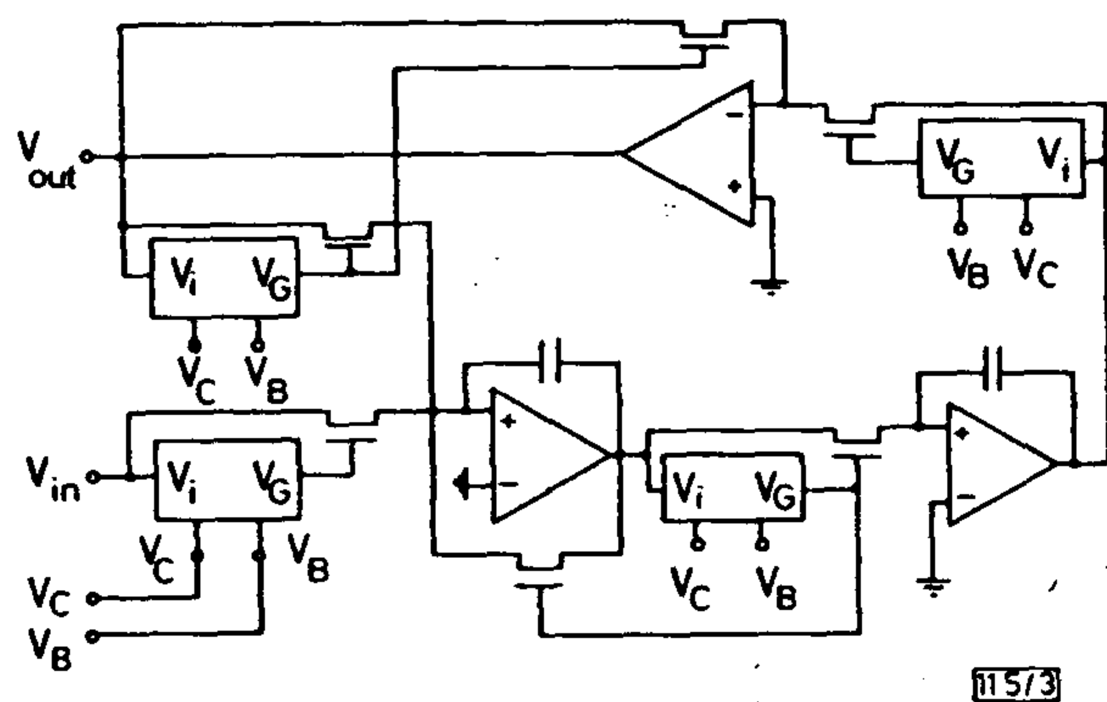

Fig. 3 *GVCR-based implementation of two-integrator-loop second-order lowpass filter structure*

Conclusions: A tunable grounded MOSFET resistor has been described in which linearisation is achieved via terminal-voltage feedback. Simulation results have shown that resistance values in the MΩ region can be realised, and that a biquadratic filter section based on the proposed device would maintain reasonably low levels of distortion with relatively large input signals.

These unbalanced structures could provide an economic alternative to the balanced arrangements previously advocated for use in fully integrated continuous-time MOSFET-C filters.

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G. WILSON
P. K. CHAN

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Department of Electrical & Electronic Engineering
Polytechnic South West
Drake Circus, Plymouth, Devon PL4 8AA, United Kingdom

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LOW-DISTORTION CMOS TRANSCONDUCTOR

Indexing terms: Circuit theory and design, Amplifiers, Distortion

A new transconductor based on MOS transistors operating in saturation is proposed. Linearisation is achieved in a common-source pair by driving the devices in a purely antiphase mode. Simulation results show that the proposed transconductor would typically exhibit less than 1% THD for input signals up to 5·7 V.

Introduction: Voltage controlled current sources or transconductors, are fundamental elements in analogue system design.[1–8] Integrated CMOS structures are of particular interest and several circuits have been described which rely on the square-law characteristics of devices in saturation. The best known of these is the long-tailed-pair (LTP) shown in Fig. 1*a*.

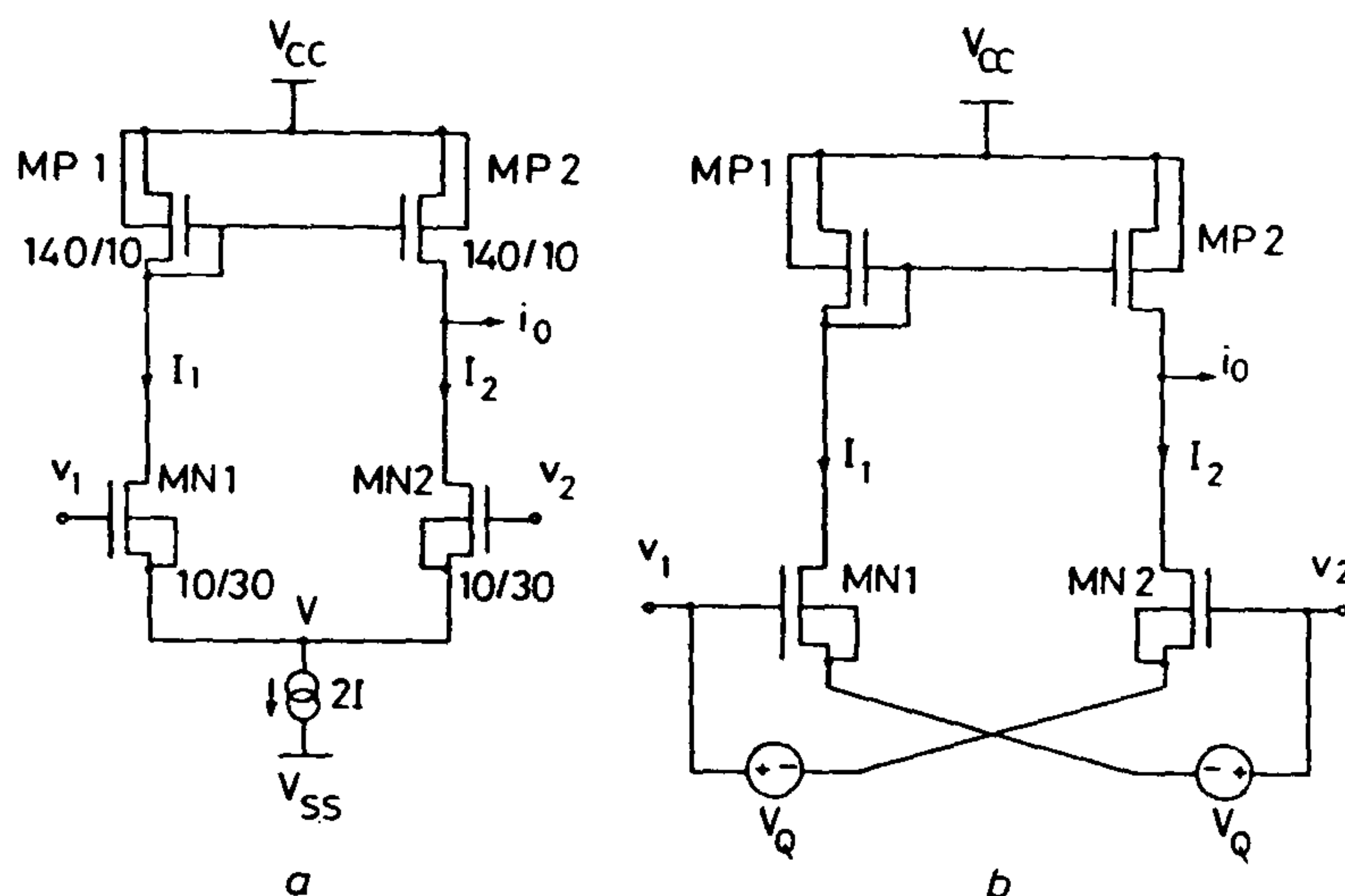

Fig. 1 *Transconductors*
a Long tailed pair
b Cross-coupled pair

The appealing simplicity of the LTP is offset by its inherently nonlinear characteristics. The constant-current condition results in a common-source node potential

$$V = V_Q + v_C + v_{NL} \tag{1}$$

where V_Q is the quiescent drive, $v_C = (v_1 + v_2)/2$ is the common-mode signal component, and

$$v_{NL} = (V_Q - V_T)\left\{1 - \sqrt{\left[1 - \frac{v^2}{4(V_Q - V_T)}\right]}\right\}$$

is an induced nonlinearity which can be written as an even-powered series in the difference signal $v = (v_1 - v_2)$. The resulting drain currents are:

$$I_1 = K\{(V_Q - V_T)^2 + v[V_Q - V_T - v_{NL}]\} \tag{2a}$$

and

$$I_2 = K\{(V_Q - V_T)^2 - v[V_Q - V_T - v_{NL}]\} \tag{2b}$$

thus the output current

$$\begin{aligned} i_0 &= I_1 - I_2 \\ &= 2Kv(V_Q - V_T - v_{NL}) \end{aligned} \tag{3}$$

contains distortion terms of all odd orders.

Although the LTP nonlinearity can be reduced using source degeneration techniques,[1] or long transistors with appropriate bias levels,[2,3] the cross-coupled pair (CCP) configuration shown schematically as Fig. 1*b*, in principle offers a distortionless $v \sim i$ conversion. This attractive prospect arises because the matched input devices are driven in a purely antiphase mode by the difference signal v producing drain currents

$$I_1 = K\{(V_Q - V_T)^2 + 2v(V_Q + V_T) + v^2\} \tag{4}$$

and

$$I_2 = K\{(V_Q - V_T)^2 - 2v(V_Q - V_T) + v^2\} \tag{5}$$

having identical (quadratic) distortion components. The difference current output

$$i_0 = I_1 - I_2 = 4Kv(V_Q - V_T) \tag{6}$$

is therefore linear and double that for the LTP.

In practice, some distortion is inevitable and departures from the ideal square-law characteristics, mismatching, mobility degradation etc., all contribute to distortion levels that generally deteriorate as the devices are driven towards cutoff.

Although the arrangement in Fig. 1*b* is unrealistic in that the inputs are required to sink the drain currents, several practical circuits[4–6] have been reported. The purpose of this letter is to show that the CCP distortion levels can be improved by applying the antiphase drive principle in a common-source pair configuration.

Antiphase common-source pair: The LTP nonlinearity is a consequence of the constant current biasing. If the current source is replaced by a voltage source generating the common-mode signal, v_C, the input devices would be driven in a purely antiphase mode. The drain and output currents for these ACSP structures can be obtained by setting v to $v/2$ in eqns. 4–6. The resulting transconductance is linear and half that of the CCP. The importance of this result lies in the observation that distortion levels are governed by the gate overdrive $(V_Q - V_T)$ and the magnitude of the gate/source signal. Higher signal levels not only increase the extent to which the devices are driven into cutoff but also lead to increase mobility degradation.[5,7,8] In comparison with the CCP, the signal swing required to drive ACSP devices into cutoff is doubled and the distortion levels correspondingly reduced. The fact that the nominal transconductance

$$g = i_0/v = 2K(V_Q - V_T) \tag{7}$$

where $K = 0{\cdot}5\mu C_{ox}(W/L)$, is half that of CCP structures is unimportant in the sense that the difference in g can normally be accommodated by modifying K with the aspect ratio. It is noteworthy that the signal swings required to drive the CCP, LTP and ACSP structures into cutoff are in the ratio $1 : \sqrt{2} : 2$.

Transconductor realisation: Fig. 2*a* details the implementation of the ACSP. The circuit consists of an AC common-mode generator,[3] a shunt feedback buffer[4] (as in Fig. 2*b*), together with a basic common-source pair. The generator is configured as two series-connected differential pairs (M3–M4 and M5–M6) with tail currents equal to $2I_0$. The AC common-

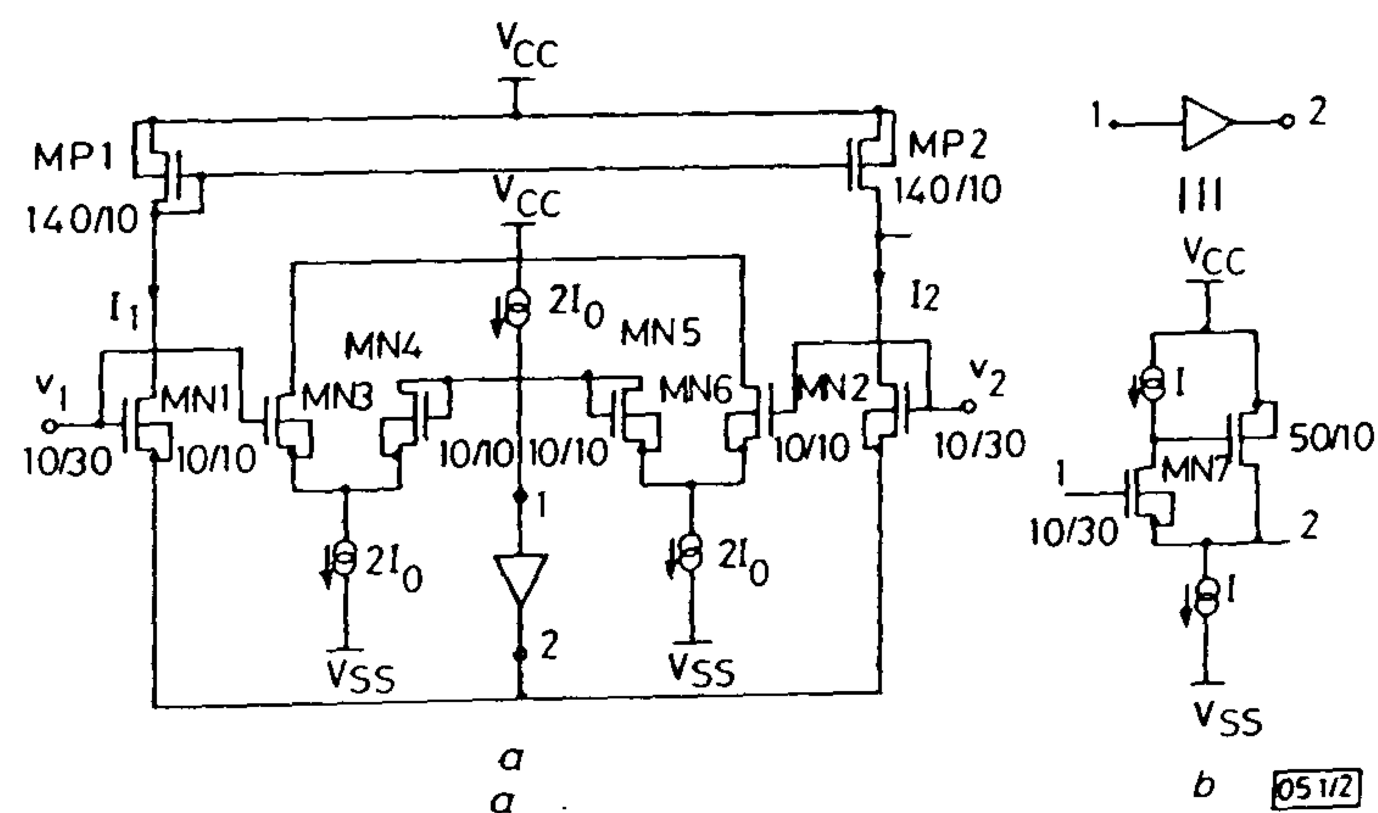

Fig. 2 *Proposed transconductor*
a Antiphase common source pair
b Shunt feedback buffer

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mode signal generated is coupled to the input pair through a source follower. The output of the source follower includes a quiescent drop V_Q formed by causing M7 to conduct with a bias current I. The buffer bias current I_B is generally chosen to ensure that M1 and M2 operate in the desired input range. The difference current $i_0 = I_1 - I_2$ can be generated using any suitable current mirror.

Simulation results: The ACSP of Fig. 2, together with an LTP and a representative CCP[4] have been simulated in SPICE using realistic level 3 transistor models. In all cases, μC_{ox} and V_T were set to $61{\cdot}3\,\mu A/V^2$ and 0·99 V, respectively. With $I = 32\,\mu A$ and $I_0 = I_B/8 = 35\,\mu A$, the ACSP uncompensated open-loop short-circuit 3 dB bandwidth was 6·7 MHz.

The DC transfer characteristics (nominally $26\,\mu A/V$) shown in Fig. 3 exemplify the signal handling capacity for the ACSP class of transconductor and can be seen to compare favourably with those of the LTP and CCP circuits. The predicted low-distortion input-signal range for the ACSP $-2(V_Q - V_T) < v < 2(V_Q - V_T)$ may not be fully realisable because of power supply limitations[5] and other circuit constraints. In the case of this ACSP implementation, the DC

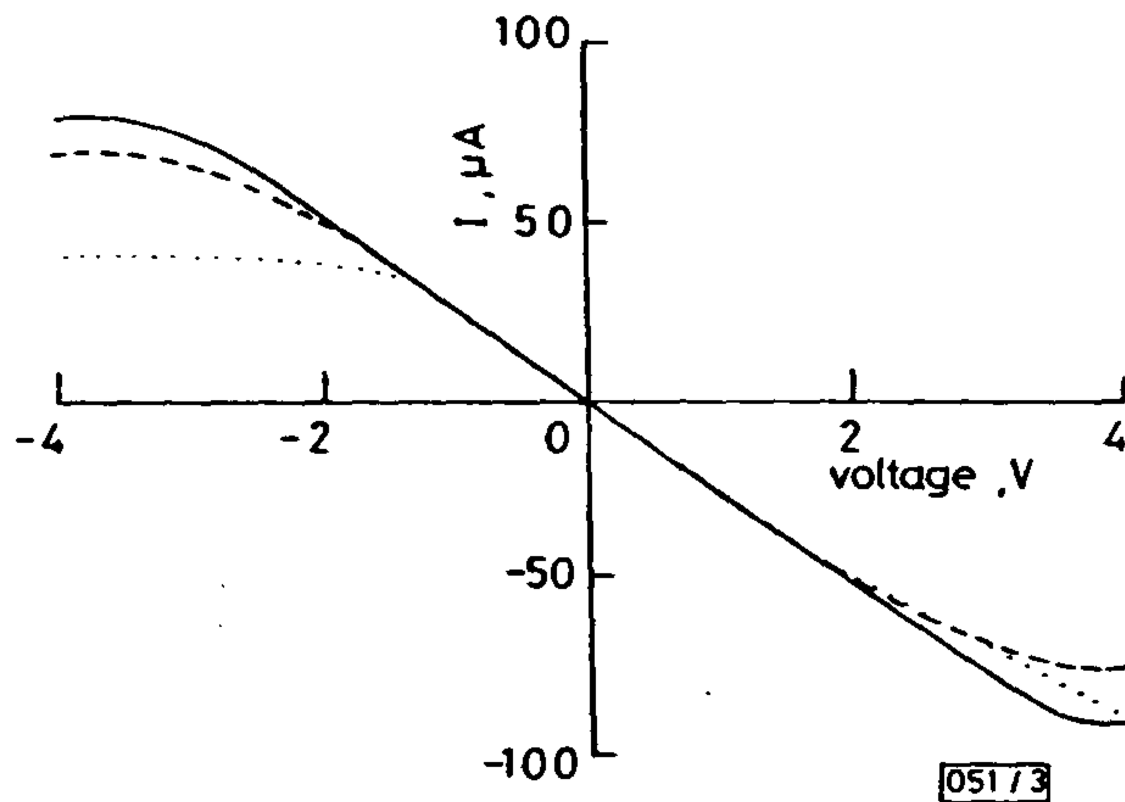

Fig. 3 *Static characteristics*

$g = 26\,\mu S$
——— ACSP
- - - - LTP
······· CCP

transfer curve indicates that although full positive signal swings are obtainable, negative swings are restricted. The asymmetry occurs because the common-mode generator cannot maintain the tail currents at $2I_0$ under large signal conditions.

Comparative THD results are given in Fig. 4. The ACSP distortion, predominantly third harmonic, remains under 1% for signals up to 5·7 and would be acceptable in many real time applications. The relatively poor performance of the CCP, which exhibits distortion levels higher than those of the basic LTP demonstrates the importance of mobility degradation.

Conclusions: A tunable transconductor based on a common source pair driven in an antiphase mode has been described

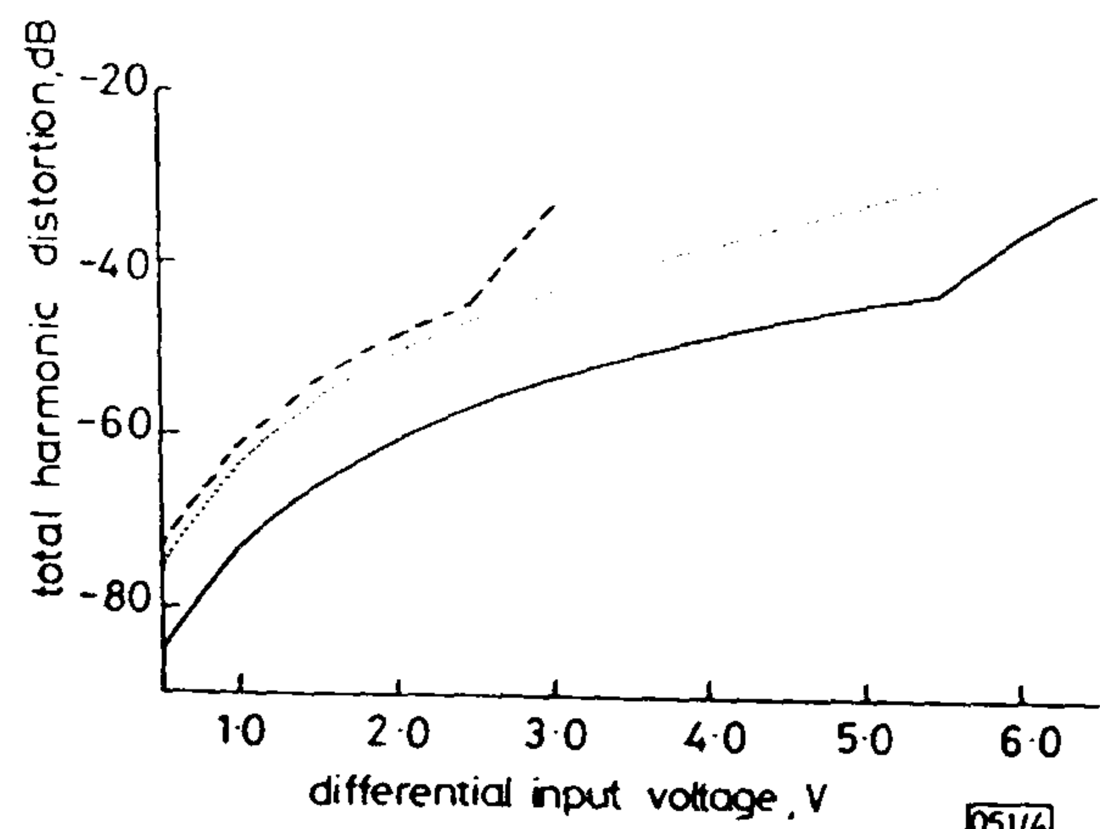

Fig. 4 *Total harmonic distortion*

$f_0 = 1$ kHz
——— ACSP
- - - - CCP
······· LTP

and simulation presented. The proposed network combines low distortion with large signal handling capacity and offers a single ended performance comparable with those of balanced structures. The proposed arrangement can be applied to integrated continuous-time filters and in applications requiring programmable amplification.

G. WILSON
P. K. CHAN

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School of Electronic, Communication and Electrical Engineering
Polytechnic South West
Drake Circus, Plymouth PL4 8AA, United Kingdom

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Fabry–Perot cavity, acting as a narrow band-pass filter, would be more appropriate. A Fabry–Perot structure might also find as an inline optical switching device, as high-finesse GaAs/AlGaAs étalons[7] have shown logic functions with very low switching energies. The use of lifted-off semiconductor films in inline components opens a wide variety of possibilities for active and passive devices not present in current inline device technology.

Conclusions: We have demonstrated a new type of inline optical filter incorporating a lifted-off epitaxial multilayer structure. A multilayer quarter-wave reflector, acting as a bandstop filter, was sandwiched between two gradient-index rod lenses. Better than 20 dB rejection was obtained, with a minimum insertion loss of less than 0·5 dB. The near-theoretical performance of the device confirms the quality of this type of material.

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J. M. DELL
G. W. YOFFE

Telecom Australia Research Laboratories
770 Blackburn Road, Clayton, Victoria 3168, Australia

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SATURATION-MODE CMOS TRANSCONDUCTOR WITH ENHANCED TUNABILITY AND LOW DISTORTION

Indexing terms: Circuit design, Coupled circuits

A new transconductor based on MOS transistors operating in saturation is presented. Linearisation is based on an offset biased pair in a cross-coupled configuration. Simulation results show that the proposed convertor combines excellent tuning characteristics with a large signal handling capability.

Introduction: The realisation of analogue filters in monolithic form using CMOS transconductor elements is of considerable interest. In practice, fabrication process tolerances and the effects of temperature variations are such that on-chip automatic tuning is essential. It is typically the case, however, that adjusting the quiescent drain current of devices in the saturation mode[1–3] significantly reduces the linear signal handling capability. With stacked structures[4–6] the problem can be particularly pronounced.

A recent solution to this problem uses an antiphase common-source pair (ACSP)[7] incorporating a shunt-feedback buffer and provides low distortion levels over a wide tuning range. The purpose of this Letter is to present an alternative structure based on cross-coupled devices which offers an enhanced tuning range with distortion levels comparable to or better than those predicted for the ACSP.

Offset-biased cross-coupled pair (OBCCP): The general arrangement of the proposed transconductor is illustrated in Fig. 1*a* and that of the basic cross-coupled pair (CCP) in Fig. 1*b*. It may be seen that the new network differs in the way the controlled transistors (MN1, 2) are coupled to the input signals (v_1, v_2) and in the biasing arrangement.

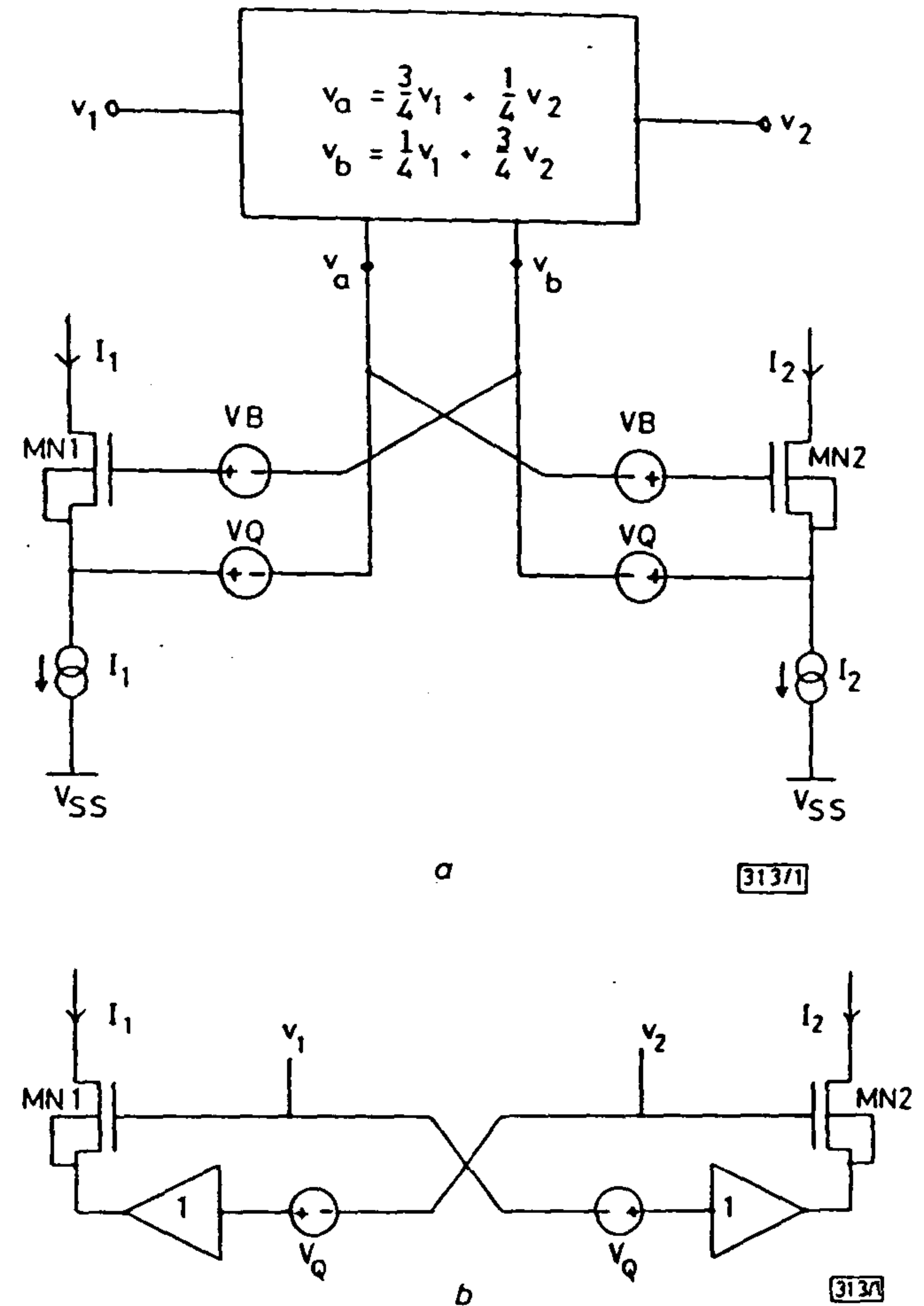

Fig. 1 *Conventional and proposed offset-biased cross-coupled transconductor schemes*
a Proposed offset-biased scheme
b Conventional arrangement

For the basic CCP the inputs v_1 and v_2 are directly coupled to the respective gates and, together with an appropriate DC offset (V_Q), are buffered onto the opposite source terminals. This arrangement results in an antiphase drive to each device equal to the full differential input ($v_1 - v_2$) with the sources offset by V_Q volts relative to signal ground.

In the new scheme the inputs are preprocessed (via two series-connected differential pairs) to form the weighted sums

$$v_a = \tfrac{3}{4}v_1 + \tfrac{1}{4}v_2 + n(v_1 - v_2) \tag{1}$$

$$v_b = \tfrac{1}{4}v_1 + \tfrac{3}{4}v_2 + n(v_1 - v_2) \tag{2}$$

where

$$n(v) = \sqrt{\left(\frac{I_t}{K}\right)}\left[1 - \sqrt{\left(1 - \frac{Kv^2}{8I_t}\right)}\right] \tag{3}$$

and I_t is the quiescent level of the differential pair bias currents and also serves to define the DC offset

$$V_Q = -\left[\sqrt{\left(\frac{I_t}{K}\right)} + V_T\right] \tag{4}$$

With v_a and v_b cross coupled to MN1 and MN2 as shown, the drain currents are independent of $n(v)$ and may be written as

$$I_1 = K[v_a - v_b + V_B - V_Q - V_T]^2 \tag{5}$$

$$I_2 = K[v_b - v_a + V_B - V_Q - V_T]^2 \tag{6}$$

The quiescent levels can therefore be controlled by an appropriate combination of gate and source DC offsets chosen to maximise the tuning range. Furthermore, since both junctions are driven in antiphase by $(v_1 - v_2)/2$ rather than the full difference signal, the signal range over which the currents maintain a specified linearity is significantly enhanced.

The difference current expression

$$I_0 = I_1 - I_2 = 2K\left[V_B + \sqrt{\left(\frac{I_t}{K}\right)}\right](v_1 - v_2) \qquad (7)$$

is in principle a purely linear function of the differential input and illustrates the dual tuning capability. In practice, however, mismatches, mobility modulation effects,[5,8] and other departures from the idealised square-law model will inevitably result in finite distortion levels.

Transconductor realisation: The transconductor is implemented as shown in Fig. 2. It consists of the controlled pair MN1–2, two series-connected differential pairs (MN3–4, MN5–6), and two *p*-channel buffers (MP1–2, MP3–4) together with associated mirror pairs. The signals generated at the source nodes of the differential pairs are cross-coupled by the buffers to the gates of the controlled pair. The resulting antiphase gate-to-source voltages produce drain currents I_1 and I_2 which are also drawn from the source nodes by means of a current loop-back technique. The output current is obtained by subtracting these two currents.

As previously noted, the transconductance can be tuned by two parameters I_t and V_B. In practice, I_t would be fixed in conjunction with the aspect ratio of the differential pairs so as to maximise the signal handling capability. The second tuning parameter V_B can be dynamically modulated by adjusting the bias current through the buffers with an external control voltage V_C. The use of *p–n* complementary DC coupling provides a bipolar range for V_B and significantly enhances the tuning characteristics.

Simulation results: SPICE simulations using realistic level-3 transistor models with gate voltage dependent mobility have been performed. The results generally show that the OBCCP compares favourably with the ACSP and offers a highly tunable transconductance with low distortion over a wide input signal range.

From the representative family of static characteristics shown in Fig. 3, it may be seen for example that the nominal transconductance (20 μA/V) is adjustable over a range of ±45% with minimal effect on either the linearity or symmetry of the input signal range.

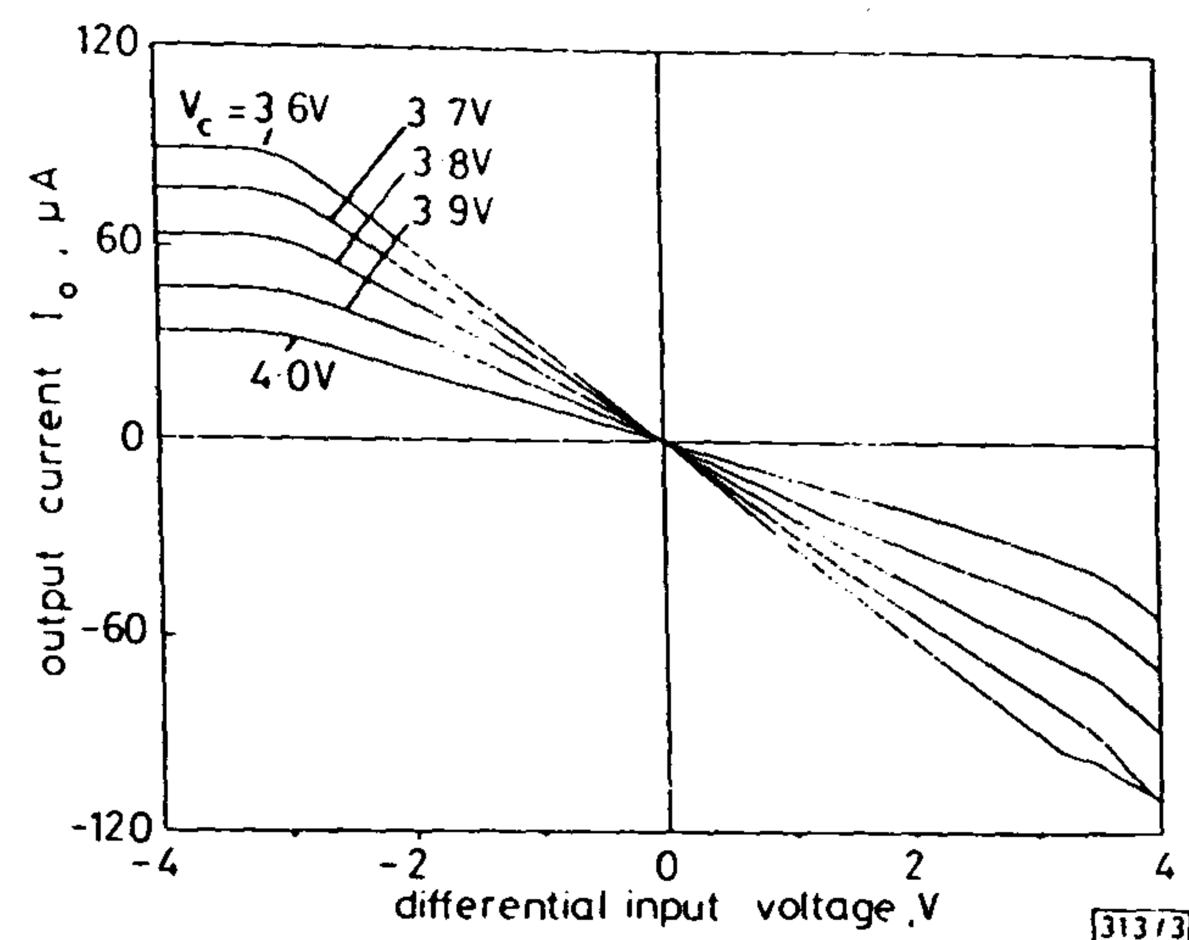

Fig. 3 *Simulated static characteristics for the OBCCP*
$I_t = 35\,\mu$A, ±5 V supplies

Fig. 4 details the variation of THD as a function of the nominal transconductance for the OBCCP and ACSP transconductors. It should be noted that these results are based on ±5 V supplies, a frequency of 1 kHz and relatively high values for both the mobility modulation factor θ (0·15 V^{-1}) and differential input voltage ($5V_{pp}$). It may be seen that the range of transconductance over which the distortion levels are better than −40 dB is considerably wider in the case of the OBCCP structure.

Conclusions: A voltage tunable transconductor based on an offset biased pair in a cross-coupled connection has been described and simulation results presented. It has been shown

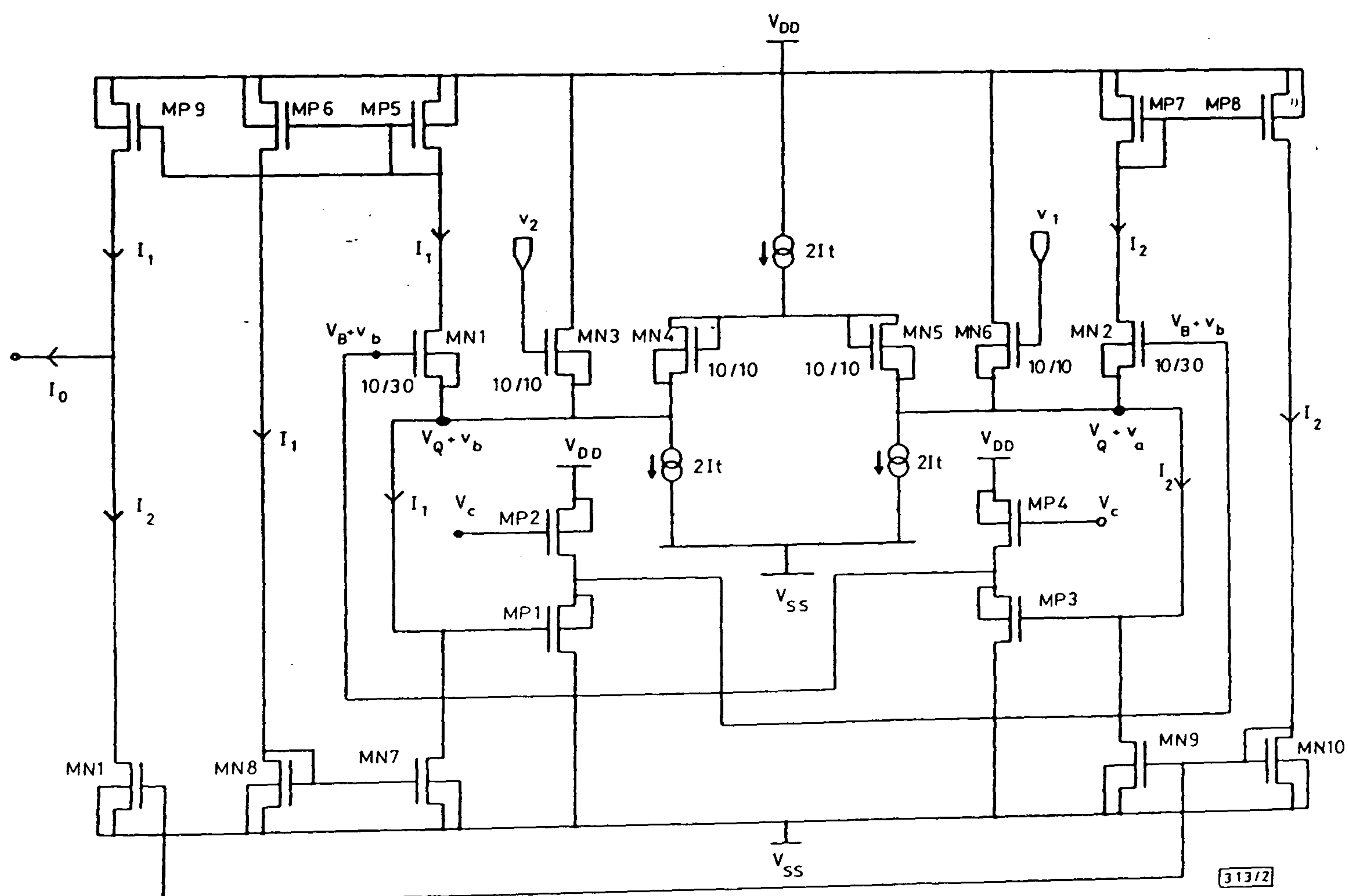

Fig. 2 *Implementation of offset biased cross-coupled pair (OBCCP) transconductor*

that the proposed convertor offers excellent tuning properties combined with low distortion for large signal drives. The network should be useful for voltage-controlled filters and other analogue signal processing applications.

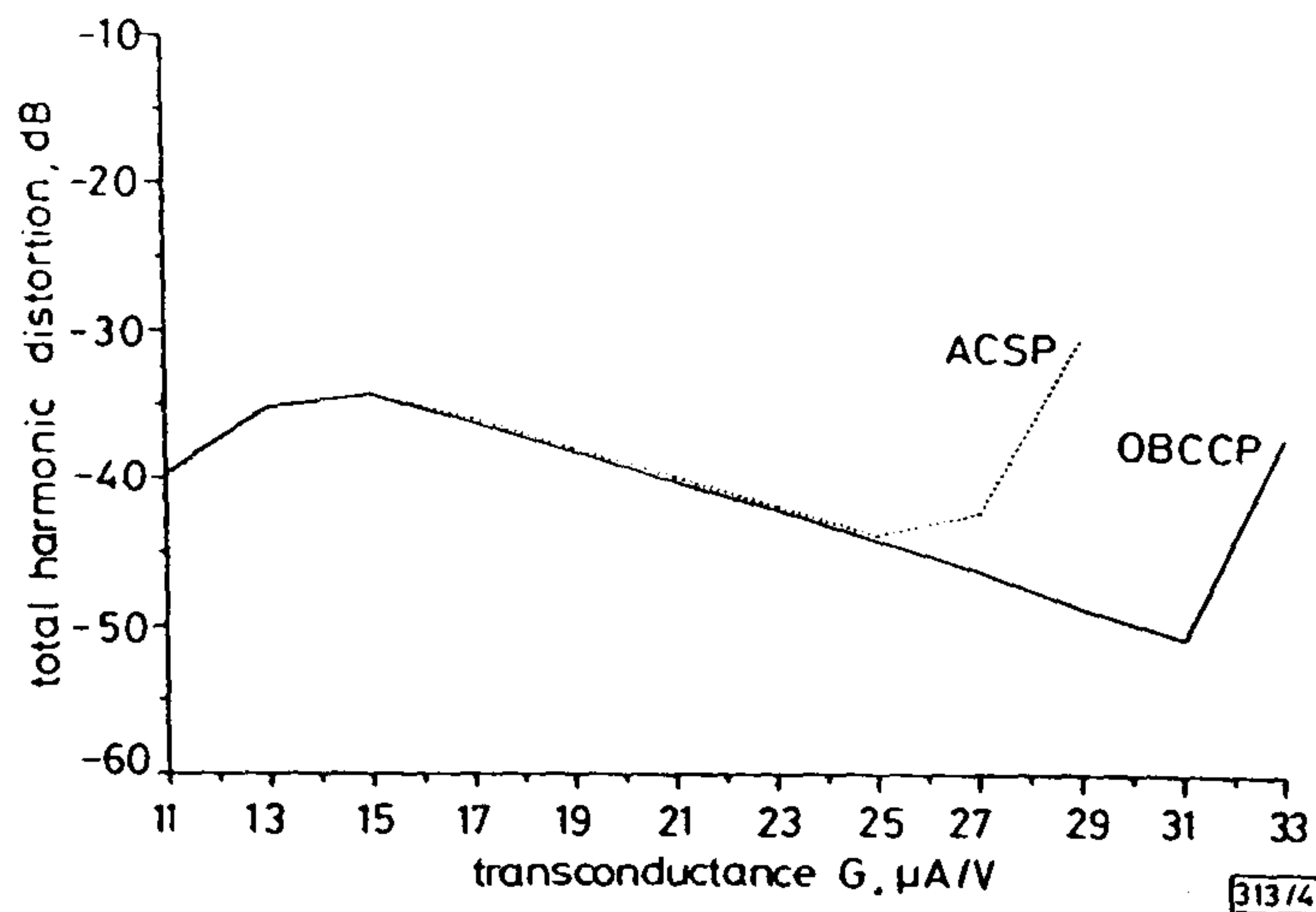

Fig. 4 *Variation of THD with transconductance for OBCCP and ACSP transconductors*

$f = 1$ kHz, $V_s = \pm 5$ V, $V_i = 5\,V_{pp}$, $\theta = 0{\cdot}15\,V^{-1}$

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G. WILSON
P. K. CHAN

5th October 1990

Polytechnic South West
School of Electronic Communication and Electrical Engineering
Drake Circus, Plymouth, Devon PL4 8AA, United Kingdom

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ANALYSIS OF ARBITRARILY SHAPED MULTIPLE-DIELECTRIC POSTS IN RECTANGULAR WAVEGUIDE BY METHOD OF LINES

Indexing terms: Electromagnetic field theory, Waveguides

The equivalent network of arbitrarily shaped multiple-dielectric posts in a rectangular waveguide is analysed by the method of lines and the equivalent parameters of three cylindrical dielectric posts in a rectangular waveguide are calculated as an example.

Introduction: Much attention has been paid to the study of dielectric posts in rectangular waveguides because of their practical significance in the design of microwave filters and highly stable microwave oscillators. The analysis is based on moment methods[1] and the combination of the finite and boundary element methods.[2] The derivation is rather complicated, especially when the number of posts increases. If the cross-section of the post is not circular, it is quite difficult to select an appropriate basis function for the post current. In this letter, the method of lines is used to analyse the scattering characteristics of arbitrarily shaped multiple-dielectric posts which are symmetrically located with respect to the xy plane. The advantages of using the method of lines are simpler derivation procedure, clear physical concept, high accuracy and no problem of convergence.

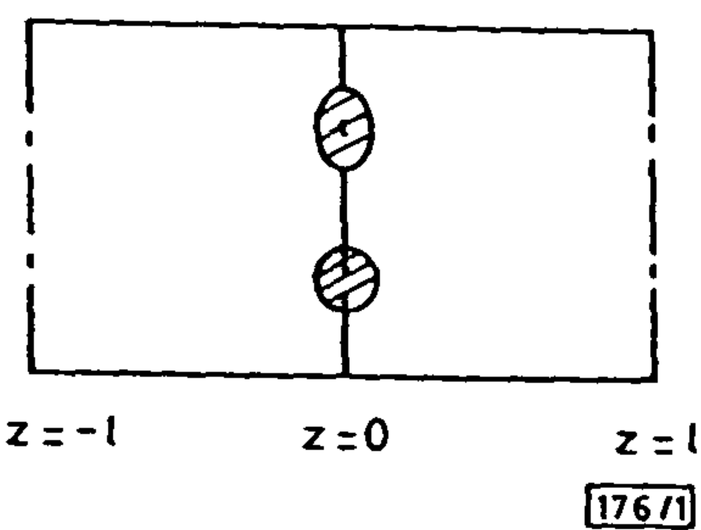

Fig. 1 *Dielectric posts*

Basic formulation: The resultant field of the TE_{10} incident wave and reflected waves from the dielectric posts is represented by a potential function. Fig. 1 shows the longitudinal cross-section of a rectangular waveguide having posts of arbitrary shape at $z = 0$. Fig. 2 shows its equivalent network. We

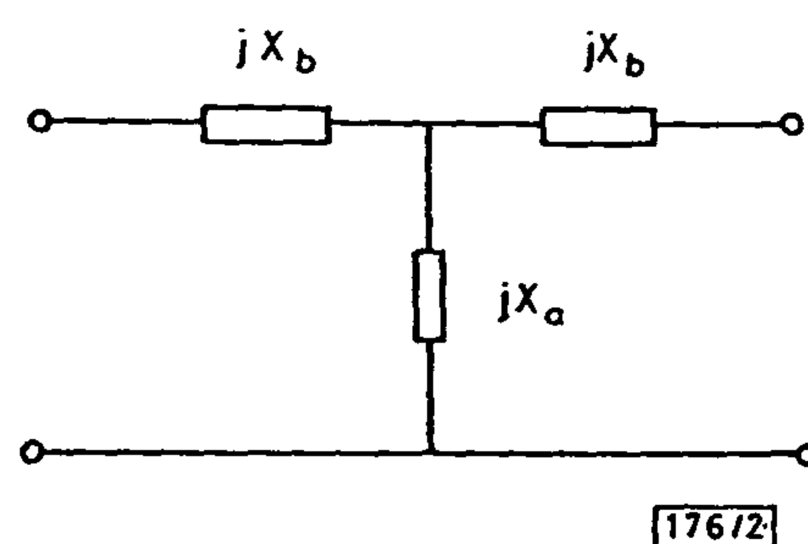

Fig. 2 *Equivalent circuit*

assume that only the dominant mode TE_{10} can propagate in the guide. The reference plane is chosen so that

$$l = n\lambda_g \tag{1}$$

where λ_g is the guide wavelength of the TE_{10} mode. The TE_{10} mode has an input impedance at $z = \pm l$, equal to that at $z = 0$. By means of the odd and even mode principle, we obtain

$$jX_b = Z_{odd}$$
$$jX_a = \tfrac{1}{2}(Z_{even} - Z_{odd}) \tag{2}$$

where Z_{even} and Z_{odd} are the input impedances of even and odd modes. Since the posts are uniform in y-direction, only TE_{m0} modes can be excited by posts. The field strength can be expressed by means of a potential function[3]

$$\bar{E} = -j\omega\mu\bar{\pi}$$
$$\bar{H} = \nabla \times \bar{\pi} \tag{3}$$
$$\bar{\pi} = \phi(x, z)\bar{u}_y$$

$\phi(x, z)$ satisfies the Helmholtz equation

$$\frac{\partial^2\phi}{\partial x^2} + \frac{\partial^2\phi}{\partial z^2} + \varepsilon_r k_0^2 \phi = 0 \tag{4}$$

where $k_0^2 = \omega^2\mu\varepsilon_0$. The input impedance at $z = -l$ is

$$Z_{in} = -j\omega\mu \left.\frac{\phi}{\partial\phi/\partial z}\right|_{z=-l} \tag{5}$$

Calculation of $\phi(x, z)$ by method of lines: The first step is to discretise the x-variable in eqn. 4. The potential ϕ can be replaced by a set $\phi = (\phi_1, \phi_2, \ldots, \phi_N)^t$ at the lines $x_i = ih$,

Comparison of four CMOS transconductors for fully integrated analogue filter applications

G. Wilson
P.K. Chan

Indexing terms: Analogue filters, Transconductors, Simulation

Abstract: An analysis of four transconductors based on CMOS transistors operating in saturation is presented and computer simulated performances are compared. It is shown that an antiphase source-coupled pair offers superior tuning characteristics and exhibits low distortion at large input drives.

1 Introduction

Monolithic filters in a MOS VLSI technology are available to integrated circuit designers in different forms. Although MOSFET-C approaches [1–3] have received much attention, they are not attractive at higher frequencies because of the effects of limited gain-bandwidth product [4]. The transconductor is capable of operating over a wide frequency range and also finds applications in programmable gain amplifiers [5], multipliers, oscillators and other nonlinear circuits [6].

Several MOS transconductors for voltage-controlled filter systems have been reported. Nedungadi [7, 8] described a compensated common source pair (CCSP). Viswanathan [9] proposed a cross-coupled structure (CCP). Other authors [10, 11] have adopted similar strategies but with differing implementations. A group of transconductors based on transistors operating in saturation are examined and their performances compared. The comparison will take account of factors such as signal handling capability, linearity and tunability.

The transconductor outputs are connected to identical differential-to-single ended current convertors to provide an equable basis for comparison (employing the two cascode mirror arrangement discussed in References 8 and 12) as illustrated in Fig. 1. The comparison is made on the basis that for all structures the transconductances are equal, the MOS models are identical, the power supplies are common, all devices are matched, and the transistors are sufficiently long to exclude channel-length modulation effect.

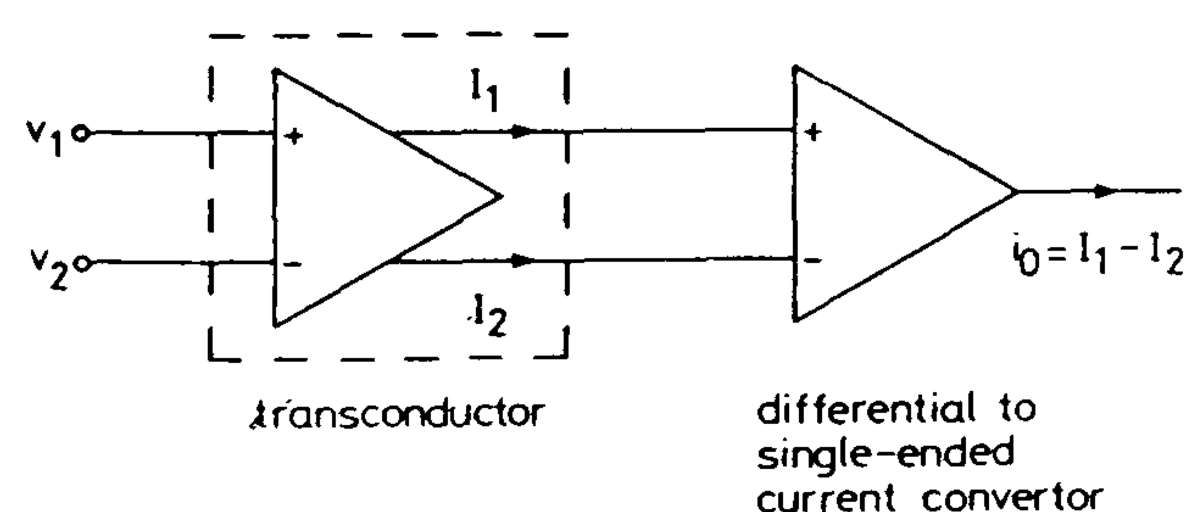

Fig. 1 *Transconductance structure*

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The authors are with the School of Electronic, Communication and Electrical Engineering, Plymouth Polytechnic of the South West, Drake Circus, Plymouth, Devon PL4 8AA, United Kingdom

The principle of operation for each transconductor type will be described, these are designated: long tail pair (LTP), compensated common source pair (CCSP), cross-coupled pair (CCP) and anti-phase common source pair (ACSP). Emphasis is placed on an analysis of nonlinearity and operating range. The problems of tuning are addressed and the characteristic of each transconductor is demonstrated and compared. The results of a comparative distortion analysis are discussed.

2 Circuit descriptions

2.1 Long tail differential pair (LTP)

From the standpoints of simplicity and high frequency response, the differential pair transconductor is quite attractive and forms a useful benchmark. Unfortunately, the nonlinearity generated by the constant current operation limits the signal handling capability and restricts the scope of this structure.

Consider the matched differential pair shown in Fig. 2*a*; the voltage v_M generated at the common source node consists of a DC bias component V_Q and an AC component $f(v)$

$$v_M = V_Q + f(v) \tag{1}$$

The drain currents for MA1 and MA2 are

$$I_1 = I + i = K[v_1 - V_Q - f(v) - V_T]^2 \tag{2}$$

$$I_2 = I - i = K[v_2 - V_Q - f(v) - V_T]^2 \tag{3}$$

where the gate overdrive

$$V_Q + V_T = -\sqrt{\left(\frac{I}{K}\right)} \tag{4}$$

defines the quiescent current I, V_T is the threshold voltage, $K = \mu C_{OX} W/2L$ is the transconductance parameter, μ is the effective carrier mobility, C_{OX} is the capacitance per unit gate area, W is the channel width and L is the channel length.

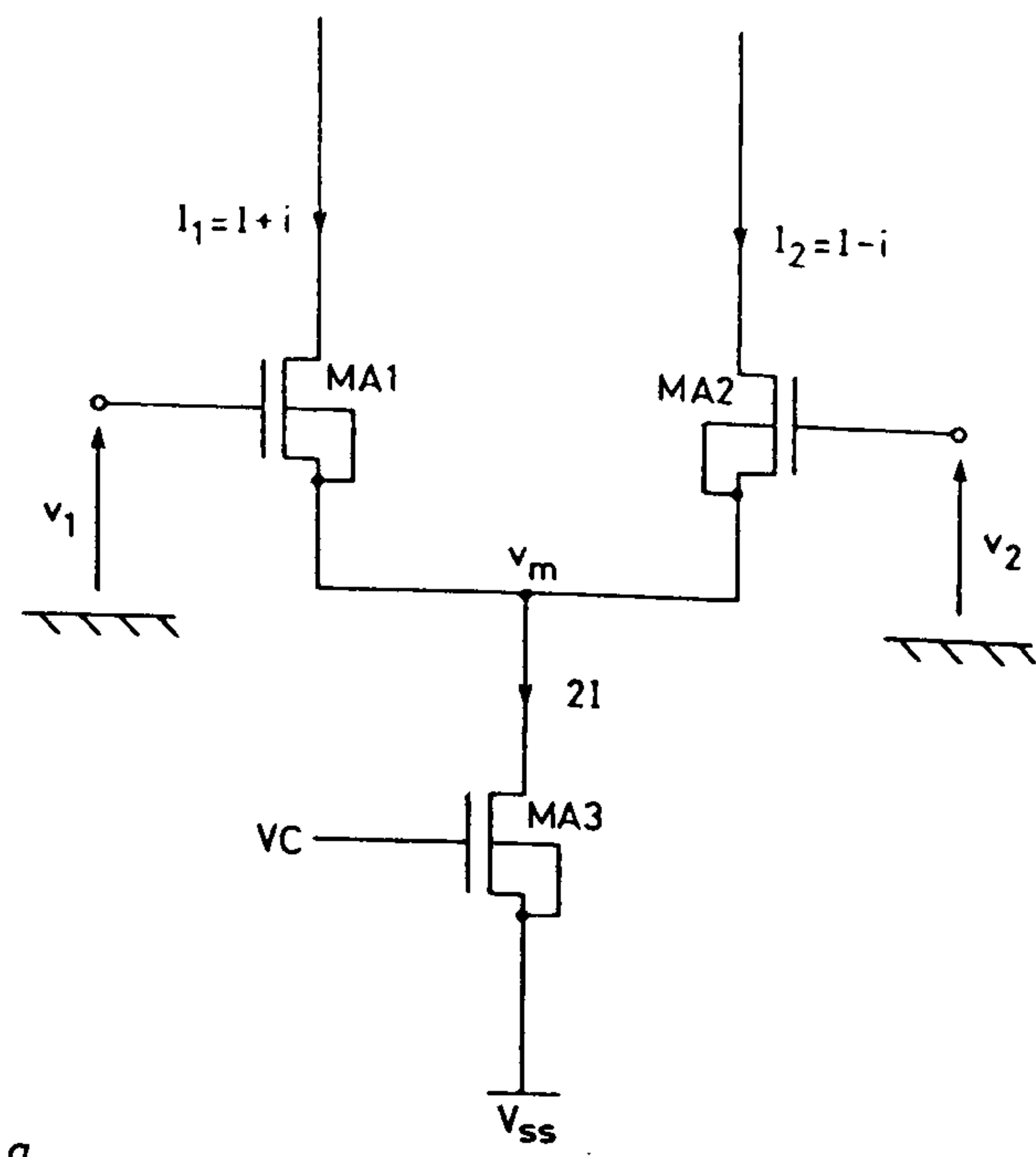
The transfer characteristic is also given by [15]

$$i_0 = I_1 - I_2 = 2i = Gv\sqrt{\left(1 - \frac{Kv^2}{4I}\right)} \tag{5}$$

where the ideal AC transconductance parameter G is defined as

$$G = 2\sqrt{(KI)} \tag{6}$$

and $v = v_1 - v_2$ is the differential input voltage.



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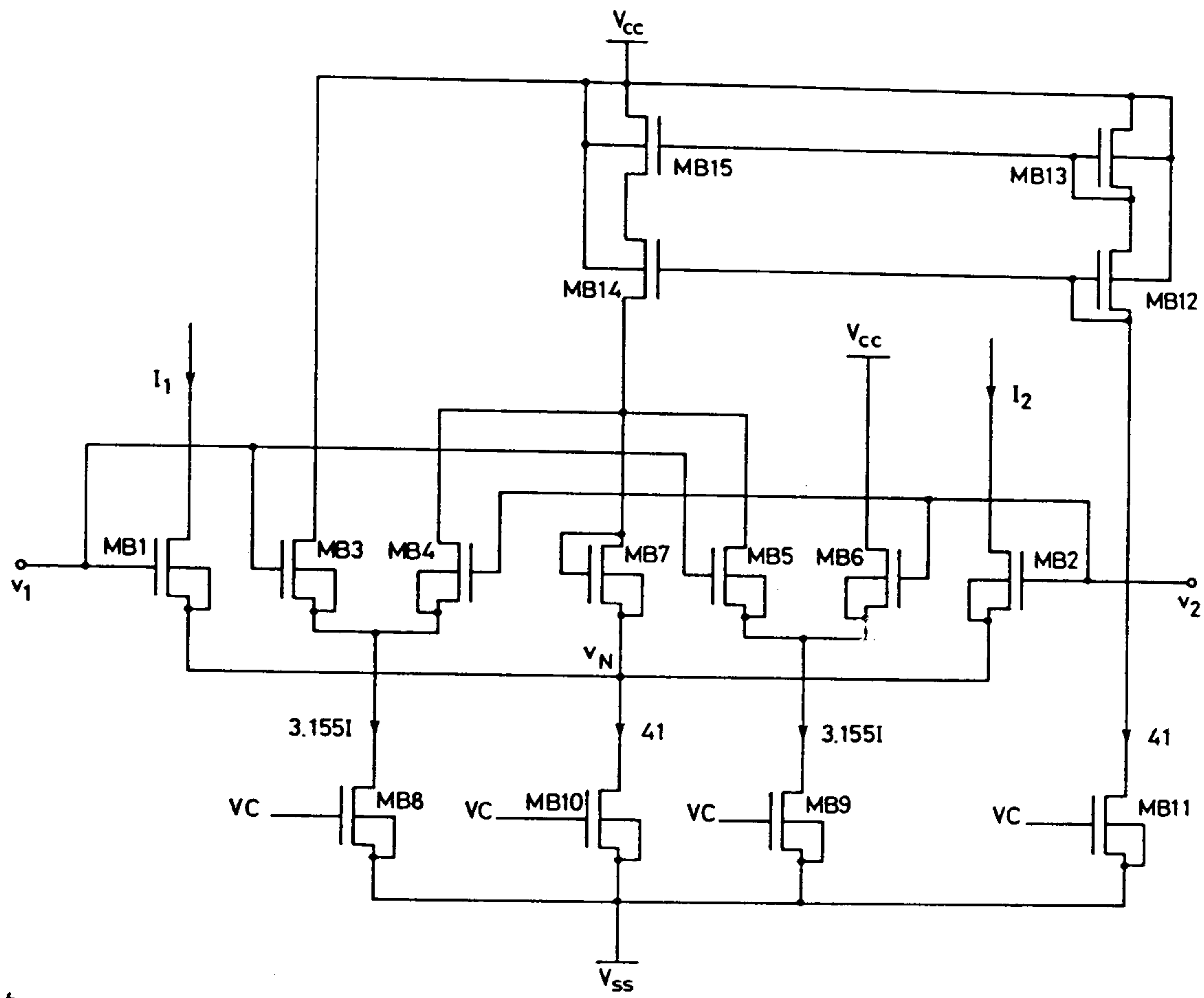

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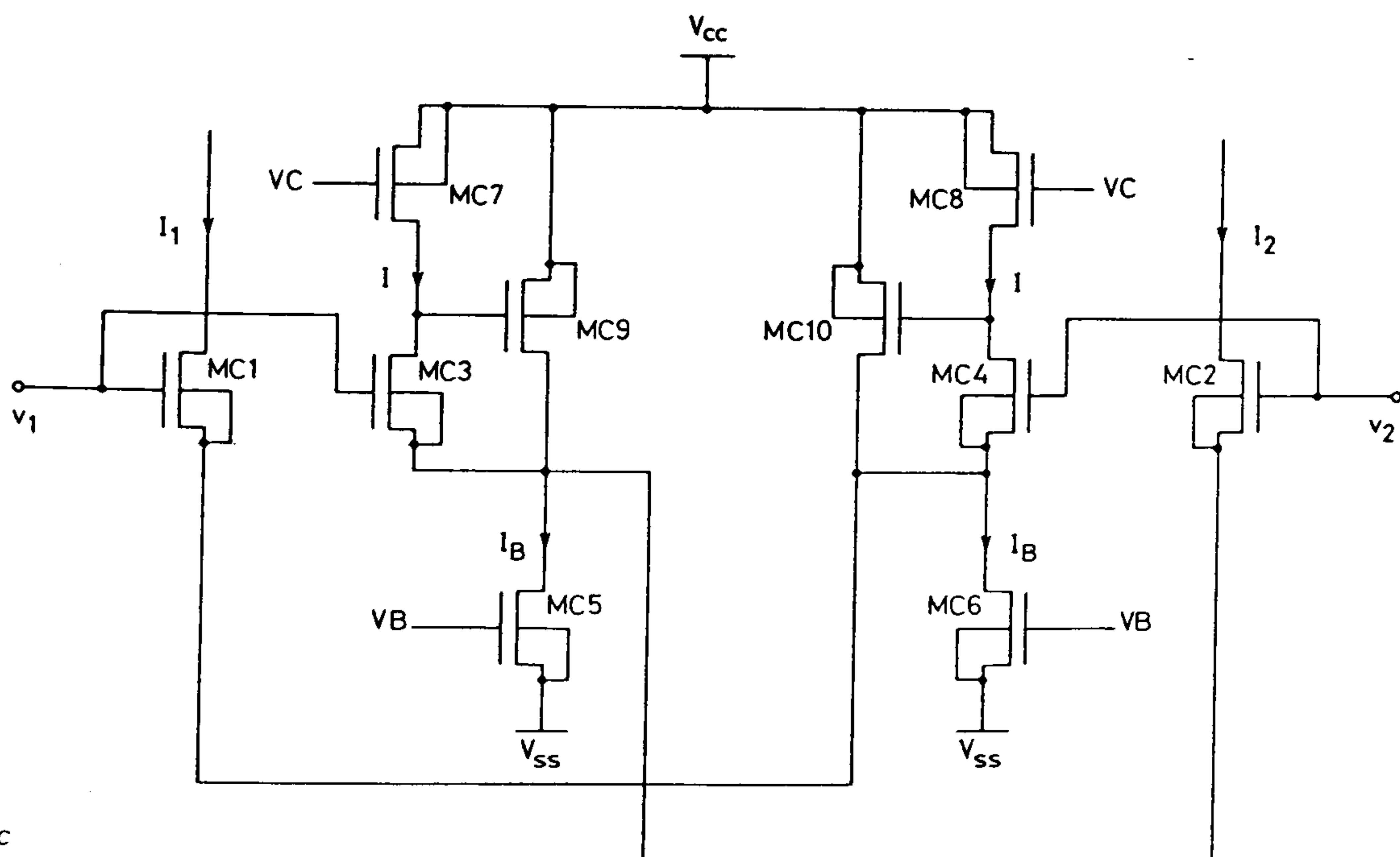

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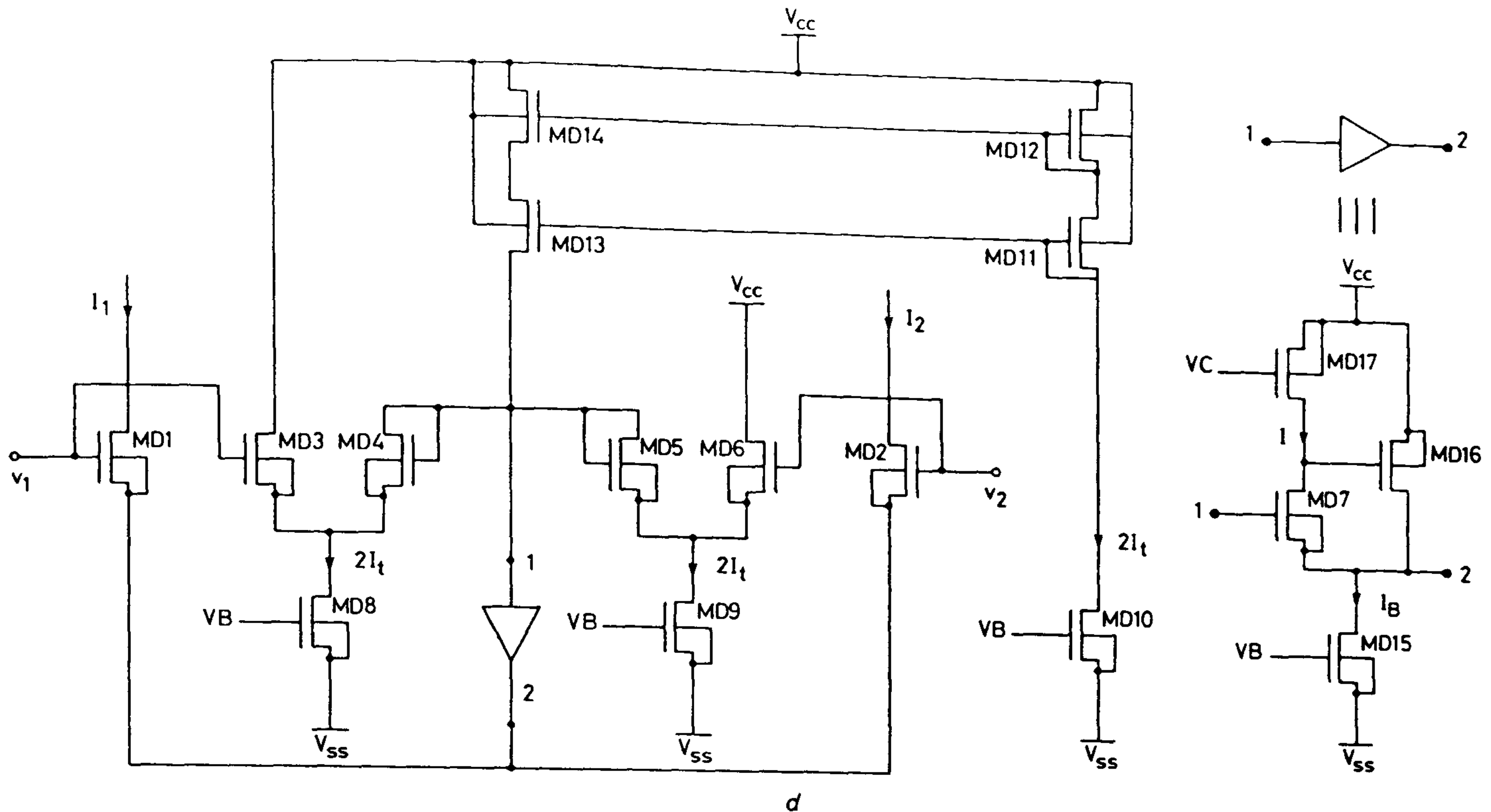

Fig. 2 *Transconductors*
a Long tail pair
b Compensated common source pair
c Cross coupled pair
d Anti-phase common source pair

It follows that for a given transconductance, the distortion can be reduced either by increasing the bias current or reducing the aspect ratio (W/L).

Subtracting eqn. 3 from eqn. 2 and equating to eqn. 5 yields

$$f(v) = \frac{v_1 + v_2}{2} + \sqrt{\left(\frac{I}{K}\right)}\left[1 - \sqrt{\left(1 - \frac{Kv^2}{4I}\right)}\right] \quad (7)$$

identifying $f(v)$ as the AC common mode signal plus a nonlinear signal, which it may be noted, is a direct consequence of the constant current biasing.

Substituting eqns. 5 and 6 into eqn. 2 and eqn. 3 gives

$$I_1 = K\left[\frac{v}{2} + \sqrt{\left(\frac{I}{K}\right)}\sqrt{\left(1 - \frac{Kv^2}{4I}\right)}\right]^2 \quad (8)$$

$$I_2 = K\left[-\frac{v}{2} + \sqrt{\left(\frac{I}{K}\right)}\sqrt{\left(1 - \frac{Kv^2}{4I}\right)}\right]^2 \quad (9)$$

from which an upper and lower limit to the operating range can be found by setting $I_1, I_2 = 0$. Thus

$$-\sqrt{(2)}\sqrt{\left(\frac{I}{K}\right)} < v < \sqrt{(2)}\sqrt{\left(\frac{I}{K}\right)} \quad (10)$$

2.2 Compensated common source pair (CCSP)

A linearised VI convertor has been described in Reference 7 and is shown in Fig. 2*b*. The linearisation process consists of generating a compensating tail current as a function of the differential input voltage from an auxiliary cross-coupled pair, which is subsequently passed to the source coupled pair.

With eqn. 5 rewritten as

$$i_0 = v\sqrt{[K(4I_t - Kv^2)]} \quad (11)$$

it can be seen that the output current is linearised by setting the tail current to

$$I_t = I + \frac{Kv^2}{4} \quad (12)$$

in which case $i_0 = Gv$.

It will be useful to examine the potential generated at the common source node under these conditions. Consider Fig. 2*b*, and let v_N be expressed as

$$v_N = V_Q + g(v) \quad (13)$$

The currents flowing through transistors MB1 and MB2 are

$$I_1 = K[v_1 - V_Q - g(v) - V_T]^2 \quad (14)$$

$$I_2 = K[v_2 - V_Q - g(v) - V_T]^2 \quad (15)$$

which with eqns. 11 and 12 yields

$$g(v) = \frac{v_1 + v_2}{2} \quad (16)$$

Thus $g(v)$ is a purely common mode signal and results in each input transistor being driven in an antiphase mode by the difference signal $v/2$. The ideal transconductance predicted by these relationships is not achieved in practice since unavoidable second order effects, amongst which mobility degradation [10, 13] has a dominant role, results in some degree of nonlinearity.

With the effective mobility expressed [14] as

$$\mu = \frac{\mu_0}{1 + \theta(v_{GS} - V_T)} \quad (17)$$

it can be shown that

$$I_1 - I_2 = G_0\left[1 - \frac{3}{2}\theta\sqrt{\left(\frac{I}{K_0}\right)} + 2\theta^2\frac{I}{K_0}\right]v - \frac{K_0}{4}\left[\theta - 4\theta^2\sqrt{\left(\frac{I}{K_0}\right)}\right]v^3 \quad (18)$$

where $G_0 = 2\sqrt{(K_0 I)}$ and $K_0 = \mu_0 C_{OX} W/2L$.

Thus mobility degradation not only reduces the transconductance, but also contributes to the generation of odd order distortion.

From eqns. 14 and 15, the operating range can be obtained as

$$-2\sqrt{\left(\frac{I}{K}\right)} < v < 2\sqrt{\left(\frac{I}{K}\right)} \quad (19)$$

and is a factor of $\surd(2)$ wider than that for the long-tailed pair.

2.3 *Cross-coupled pair (CCP)*

A cross-coupled linearisation technique has been proposed by Viswanathan [9]. The implementation employs two buffers to establish cross-coupling for the two-transistor cell as shown in Fig. 2*c*, and in principle also offers an ideal linear $v \sim i$ conversion. The drain currents are

$$I_1 = K'[v - (V'_Q + V_T)]^2 \tag{20}$$

$$I_2 = K'[-v - (V'_Q + V_T)]^2 \tag{21}$$

where $V'_Q + V_T = -\surd(I'/K')$.

The difference current output is

$$i_0 = I_1 - I_2 = 4\surd(K'I')v = G'v \tag{22}$$

To provide a proper basis for comparison, K' and I' are selected to set $G' = G$, and $V'_Q = V_Q$ which can only be satisfied when $K' = K/2$ and $I' = I/2$.

In this case

$$i_0 = G_0\left[1 - \frac{3}{2}\theta\sqrt{\left(\frac{I}{K_0}\right)} + 2\theta^2\frac{I}{K_0}\right]v - K_0\left[\theta - 4\theta^2\sqrt{\left(\frac{I}{K_0}\right)}\right]v^3 \tag{23}$$

from which it may be noted that the distortion coefficient is four times larger than that for the CCSP.

From eqns. 20 and 21, the operating range is

$$-\sqrt{\left(\frac{I}{K}\right)} < v < \sqrt{\left(\frac{I}{K}\right)} \tag{24}$$

and can be seen to be $\surd(2)$ times lower than that for the LTP.

2.4 *Anti-phase common source pair (ACSP)*

As previously noted, the LTP nonlinearity is a result of the constant current drive. It was also noted that the current mode compensation in the CCSP structure resulted in a purely differential drive to the input transistors. This can be achieved directly [20] by replacing the current drive with a common-mode voltage source. The implementation is shown in Fig. 2*d*, and comprises an AC common-mode signal generator [15], a shunt feedback buffer [9], together with a pair of common-source transistors. The generator is configured as two series-connected differential pairs (MD3 and MD4, MD5 and MD6) with tail currents equal to $2I_t$. The AC common-mode signal generated is coupled to the input pair through a source follower. The output of the source follower includes a quiescent drop V_Q formed by conducting MD7 with a bias current I. The buffer current I_B is chosen to ensure that MD1 and MD2 operate in the desired input voltage range and has been set at $8I_t\mu A$. The drain currents are

$$I_1 = K\left[\frac{v}{2} - (V_Q + V_T)\right]^2 \tag{25}$$

$$I_2 = K\left[-\frac{v}{2} - (V_Q + V_T)\right]^2 \tag{26}$$

giving a difference output current $i_0 = Gv$.

With mobility taken into account, the output current is as given by eqn. 18 for the CCSP transconductor. Equally, the input signal range is given by eqn. 19 and the signal swings required to drive the LTP, CCSP, CCP and ACSP structures into cut-off are therefore in the ratio: $\surd(2)$, 2, 1 and 2, respectively.

3 Tuning characteristics

In continuous-time transconductor-C filter applications, the cut-off frequency of the filter is dependent on the ratio of the transconductance G to the integrating capacitance C. However, the G/C ratios required cannot be obtained with sufficient accuracy because of unpredictable process and temperature variations. Several automatic tuning schemes [9, 15–18] have been suggested to obtain accurate filter performances.

A major problem in transconductor design is to guarantee reasonable signal handling capability when the transconductance is tuned by the on-chip automatic system. For the convertors under consideration [8, 12], the maximum value of input signal voltage is governed by the constraint that all the transistors must operate in their saturation region. Convertors with a stacked structure [10, 19] are subject to an even smaller tuning range if reasonable linearity is to be maintained. It should be noted that the saturation voltages for current sink transistors are changed in the course of automatic G tuning. As a consequence, correction for temperature changes and process tolerance may seriously degrade the signal handling capability, and cause loss of dynamic range. In the case of the ACSP structure, the key to alleviating this problem lies in making use of the shunt feedback buffer operating in a partial cancellation mode. Provided the current I_B is sufficiently large, transistor MD15 can operate well into the non-saturation region and even down to the negative supply rail without seriously affecting the operation of the controlled transistor MD17.

SPICE simulations using realistic level 3 transistor models with gate voltage dependent mobility have been performed. The appropriate process parameters and relevant device aspect ratios are given in Table 1 and Table 2, respectively.

Table 1: Appropriate process parameters

Parameter	NMOS	PMOS
VTO, V	0.99	−0.8
TOX, ×10⁻¹⁰ m	400	400
NSUB, ×10¹⁵ cm⁻³	7	4
XJ, ×10⁻⁶ m	0.18	0.21
LD, ×10⁻⁶ m	0.341	0.45
UO, cm²/Vs	710	300
VMAX, ×10⁵ m/s	1.5	3
DELTA	0.3	0.75
THETA, V⁻¹	0.15	0.4
ETA	0.15	0.15
KAPPA	0.6	1.5
TPG	1	−1
GAMMA, V⁰·⁵	0.65	0.46
NFS, ×10¹¹ cm⁻²	2.4	1.68
CGSO, ×10⁻¹⁰ F/m	0.87	1.24
CGDO, ×10⁻¹⁰ F/m	0.87	1.24
CGBO, ×10⁻¹¹ F/m	2.79	4.03
PB, V	0.6	0.6
CJ, ×10⁻⁴ F/m²	1.78	1.83
JS, ×10⁻⁸ A/m²	8.2	3.46
MJ	0.481	0.526
CJSW, ×10⁻¹⁰ F/m	3.58	2.29
MJSW	0.218	0.172

Fig. 3*a–d* detail the family of static characteristics obtained for each of the four transconductors at appropriate control voltage levels. It can be observed that although all four transconductors offer some degree of

tunability, the ACSP is the only structure which retains linearity over the tuning range.

Table 2: Device aspect ratios

Device	Aspect Ratio (μm)/(μm)
MA1–MA2	10/30
MA3	50/10
MB1–MB2, MB4–MB5, MB7	10/30
MB8–MB9	78.875/10
MB10–MB11	100/10
MB12–MB14	140/10
MC1–MC4	10/60
MC5–MC6	60/10
MC7–MC8	44/10
MC9–MC10	50/10
MD1–MD2, MD7	10/30
MD3–MD6	10/10
MD8–MD10	60/20
MD11–MD14	140/10
MD15	120/10
MD16–MD17	50/10

4 Distortion/dynamic range

The operating ranges quoted assumes that the controlled transistors obey the familiar square-law characteristic. Under large signal conditions, this assumption cannot be sustained and, to provide an assessment of the relative linearity for the group of transconductors, their simulated transfer characteristics (for a nominal transconductance of 26 μA/V) are collectively shown in Fig. 4*a*. It can be seen that although the CCSP has the largest linear range for positive excursions, nonlinearity occurs with relatively small negative swings. By contrast, the wide linear range for the ACSP extends to both quadrants.

The variations of THD as a function of differential input voltage are shown in Fig. 4*b*. It can be observed that for low signal levels the THD for CCSP and ACSP structures are similar as predicted by the mobility degradation analysis. However, for larger signals, the CCSP controlled transistors are driven into the Ohmic region of operation, resulting in a rapid departure from linearity. The signal handling capability of the ACSP is not similarly degraded, and linearity is maintained over a wide range of input voltages. In the case of the CCP, on the other hand, the effect of a high mobility degradation results in a generally inferior performance. It is clear that in general, distortion is critically dependent on the degree of mobility degradation.

In the cases of the CCP and ACSP transconductors, the operating range is dependent on the current buffers; however, their operation is different. As the summing currents $I_1 + I_2$ are combined into the output node of the buffer in the ACSP, they tend to cancel each other because I_1 is in anti-phase with I_2. This leads to very small voltage swings at the drain of transistor MD17 even under large signal drives. However, no partial cancellation occurs in the CCP as currents I_1 and I_2 flow into the corresponding buffers. Under these circum-

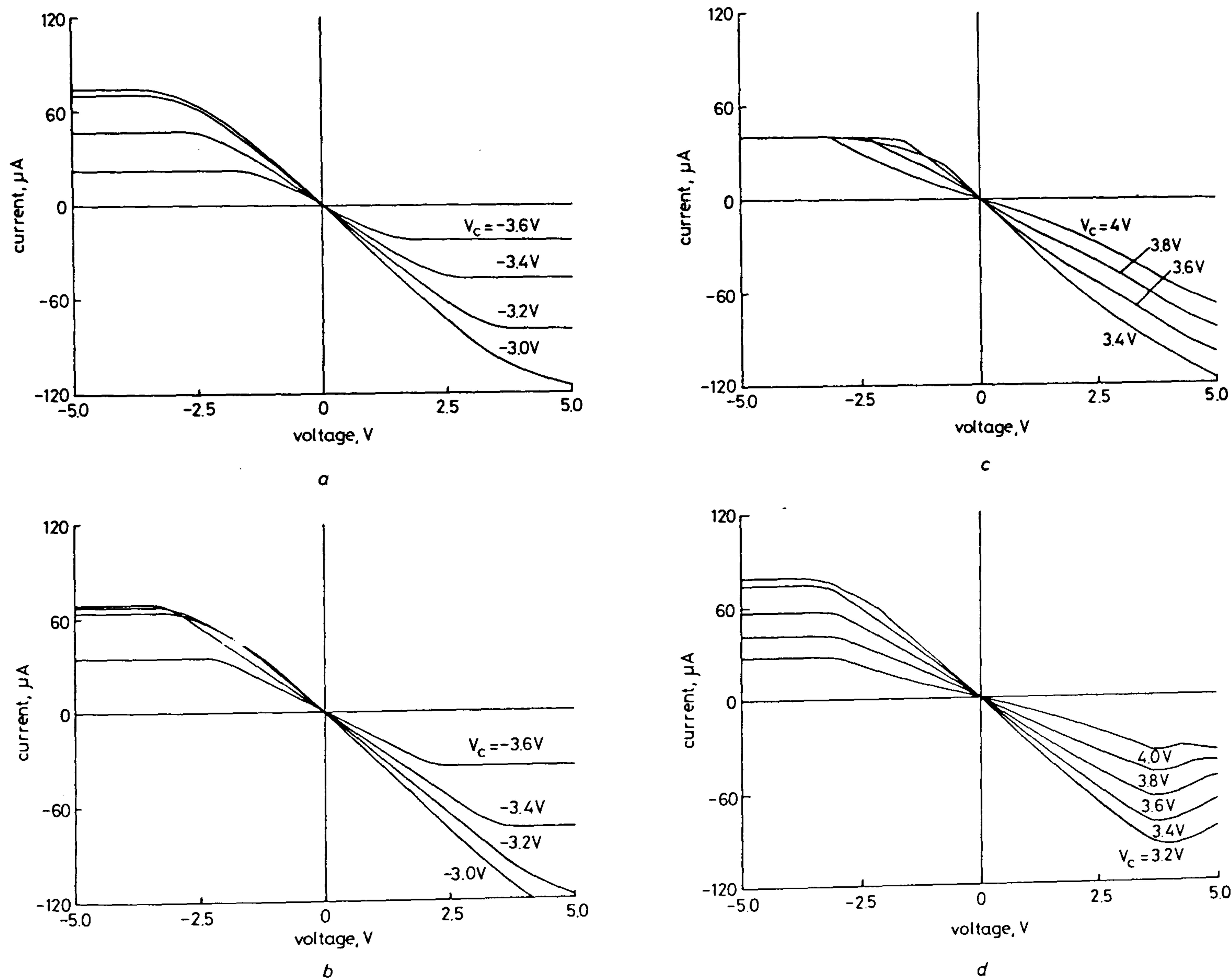

Fig. 3 *Control voltage tuning of static characteristics*
a Long tail pair
b Compensated common source pair
c Cross coupled pair
d Anti-phase common source pair

stances, transistors MC7 and MC8 cannot be maintained in saturation for large input signals. The insensitivity of the ACSP to this problem is largely responsible for its

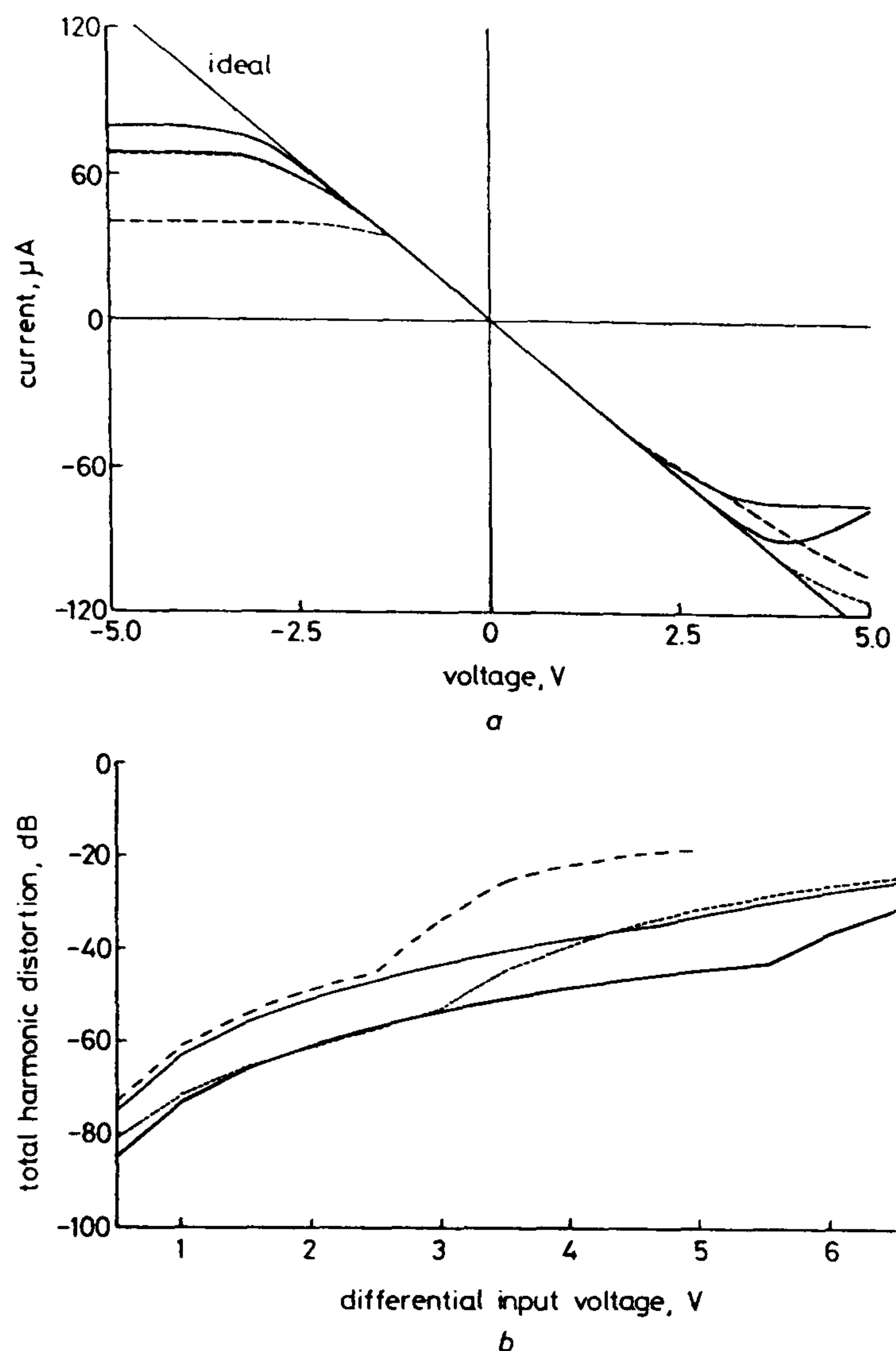

Fig. 4 *Characteristics of structures*
—— ACSP ------- CCSP
—— LTP - - - - CCP
a Group static for nominal transconductance (26 μA/V)
b Total harmonic distortion against signal level ($G = 26\ \mu s$)

superior performance. In fact, the actual performance limitation in the ACSP arises from cut-off in the AC common mode generator differential pairs. Since the DC bias voltage V_B is fixed, they can support a large input signal before cut-off occurs. Optimisation of the factor $\sqrt{(I_c/K)}$ in the differential pairs may be necessary to achieve maximum signal handling capability.

In addition to the mobility degradation effect which gives rise to both harmonic distortion and a reduction in the transconductance gain, other second order effects may be considered, e.g. channel-length modulation, body effect and device mismatching. In this study, the channel length of input devices was chosen to be greater than 10 μm, in which case, channel-length modulation can be neglected. The body effect it may be noted, can be minimised by placing the input device pairs in a common P-well. Since every device was assumed to be perfectly matched, the simulation results obtained illustrate the relative performance for the four types of transconductors. Although the symmetrical structures of convertors suppresses even order nonlinearities, in practice, device mismatching does give rise to additional even order distortion. The overall performance comparison is summarised in Table 3.

Table 3: Overall performance comparison

$G = 26\ \mu$A/V	LTP	CCSP	CCP	ACSP
Input for 1% THD (V_{pp})	3.6	3.9	2.9	5.7
Maximum linear range	±3.4	±3.5	±2.2	±3.7
Power consumption (mW)	1.48	6.19	3.23	5.69

5 Conclusions

A comparison of four CMOS transconductors based on devices operating in saturation has been presented. Practical limitations on their performances relating to signal range, linearity, tunability and total harmonic distortion have been discussed.

It has been shown that the combination of a wide dynamic range and tunability make the ACSP an attractive solution in voltage-controlled filter applications. However, the technique does demand higher power consumption and it may be necessary to compromise between power consumption and the extent to which the linearity to be maintained. This study has also shown that the basic long-tail pair presents an economical solution for applications where higher distortion levels can be accepted.

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CMOS SERIES/PARALLEL QUAD RESISTOR

G. Wilson and P. K. Chan

Indexing terms: Resistors, Integrated circuits, Circuit theory and design

A new CMOS floating resistor scheme based on a series/parallel connection of four identical devices operating in nonsaturation is described. The nominal resistance is independent of threshold parameter variations and comparative SPICE simulations have shown that the new structure offers improved distortion performance combined with excellent tunability.

Introduction: In CMOS technology the requirement for controllable resistors with low distortion has led to a wide range of structures, many of which use the MOSFET operating in nonsaturation [1–4]. Unfortunately, even after the dominant quadratic distortion terms have been eliminated, linearity can be significantly reduced by bulk modulation and mobility degradation effects.

The purpose of this Letter is to present a new structure which is insensitive to bulk modulation effects and combines low distortion with excellent tunability.

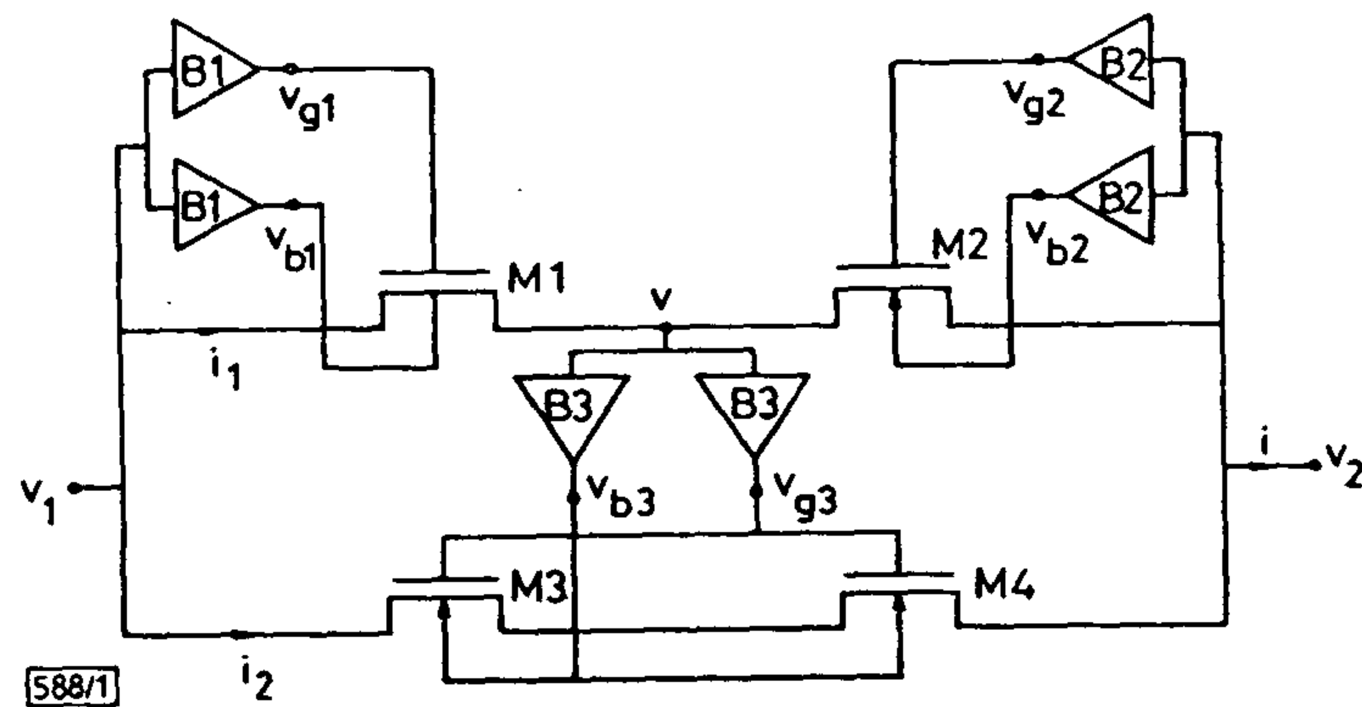

Fig. 1 *Series/parallel quad resistor (SPQR) structure*

Linearisation technique: The proposed floating resistor scheme is shown in Fig. 1 and consists of a matched quad of transistors with their gate and bulk terminals driven by matching buffers [5] of the type illustrated in Fig. 2.

The linearisation process can be appreciated by noting that the branch consisting of M1 and M2 together with buffers B1 and B2 is a transformation of the single-buffer series pair resistor (SPR) proposed by VanPeteghem and Rice [5] and as such, has identical terminal characteristics. Thus for this branch, the midpoint potential v takes on values which result in the complete suppression of the fundamental quadratic nonlinearity in the current i_1. Because the signal potential is distributed almost equally across the devices, the residual distortion (associated with bulk modulation and mobility degradation effects) could be expected to be lower than that in parallel schemes where individual devices support the full signed potential [1]. Unfortunately, in suppressing the quadratic distortion terms, a large cubic nonlinearity is generated and THD performance is significantly degraded. However, with the midpoint potential buffered to the commoned gates of the M3, M4 pair (electrically identical to a single device of length $2 \times L$), the dominant quadratic nonlinearity in the lower branch current is also suppressed but in this case, the concomitant cubic distortion component appears with reversed sign.

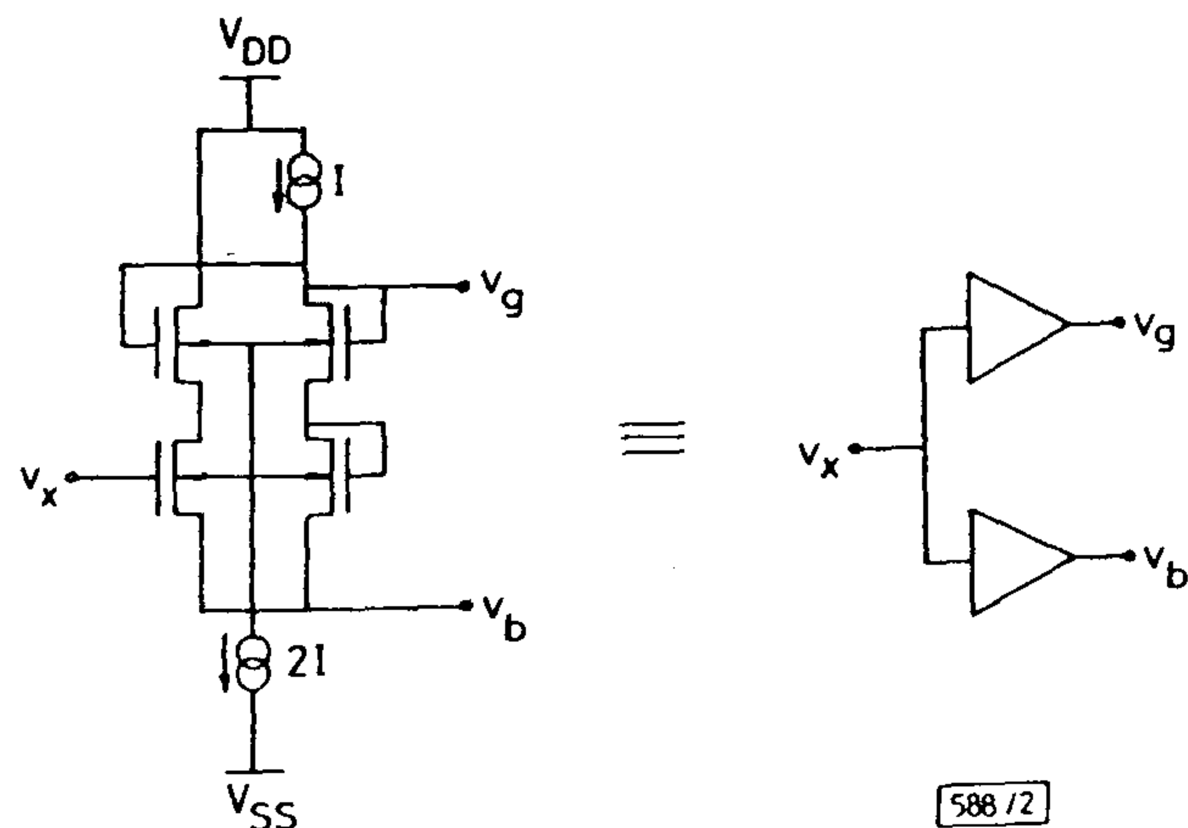

Fig. 2 *VanPeteghem–Rice level shifting buffer*

Linearisation in this series/parallel quad resistor (SPQR) configuration is therefore enhanced in relation to that of SPR structures by distributing the signal across pairs of devices without having the associated cubic nonlinearity appearing in the net terminal current.

An approximate expression for the signal current will now be developed in terms of the simplified long channel nonsaturation-mode drain current equation [7]

$$i_d = 2K\left\{v_{gs} - v_{th} - \frac{v_{ds}}{2}\left[1 + \frac{\gamma}{4\sqrt{(\phi_B + v_{sb})}}\right]\right\}v_{ds} \quad (1)$$

where the transconductance parameter $K = \mu C_{OX} W/2L$, the effective mobility $\mu = \mu_0/[1 + \theta(v_{gs} - v_{th})]$ and the threshold voltage $v_{th} = V_{TC} - \gamma\sqrt{(\phi_B)} + \gamma\sqrt{(\phi_B + v_{sb})}$.

The saturation-mode nMOS buffers in Fig. 2 (matching an nMOS quad of controlled devices) produce level shifted outputs

$$v_g = v_x + \sqrt{\left(\frac{I}{K'}\right)} + V_{TO} - \gamma\sqrt{(\phi_B)} + \gamma\sqrt{\left[\sqrt{\left(\frac{I}{K'}\right)} + V_{TO} + \phi_B\right]} \quad (2)$$

and

$$v_b = v_x - \sqrt{\left(\frac{I}{K'}\right)} - V_{TO} \quad (3)$$

where the DC bias current I is used to tune the nominal resistance level and K' is the transconductance parameter corresponding to an effective mobility $\mu' = \mu_0/[1 + \theta\sqrt{(I/K')}]$.

It can be shown that the midpoint potential in the upper branch can be approximated as

$$v = \frac{v_1 + v_2}{2} + \frac{(1 + 2\delta)}{8\sqrt{\left(\frac{I}{K'}\right)}}(v_1 - v_2)^2 \quad (4)$$

where

$$\delta = \frac{\gamma}{4\sqrt{\left(\frac{I}{K'} + V_{TO} + \phi_B\right)}} \ll 1$$

The resulting upper branch current is

$$i_1 \simeq 2K'\left\{\sqrt{\left(\frac{I}{K'}\right)}\frac{(v_1 - v_2)}{2} + \left[\delta - (1 + 2\delta)\theta'\sqrt{\left(\frac{I}{K'}\right)}\right] \times \frac{(v_1 - v_2)^2}{8} - \left\{(1 + \delta)(1 + 2\delta)\left[1 - \theta'\sqrt{\left(\frac{I}{K'}\right)}\right]\right\} \times \frac{(v_1 - v_2)^3}{16\sqrt{\left(\frac{I}{K'}\right)}}\right\} \quad (5)$$

with

$$\theta' = \theta\Big/\left[1 + \theta\sqrt{\left(\frac{I}{K'}\right)}\right]$$

This expression which is identical to that for the SPR, illustrates how the dependence of the linear and cubic terms on the gate overdrive $[\sqrt{(I/K')}]$ would result in increased distortion at lower bias current levels.

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With the midpoint potential buffered onto the common gate and bulk terminals of the M3, M4 pair, the lower branch current can be approximated as

$$i_2 \simeq 2K'\left\{\sqrt{\left(\frac{I}{K'}\right)}\frac{(v_1 - v_2)}{2} + \left[\delta - (1 + 2\delta)\theta'\sqrt{\left(\frac{I}{K'}\right)}\right]\frac{(v_1 - v_2)^2}{8} + \left\{(1 + \delta)(1 + 2\delta)\left[1 - \theta'\sqrt{\left(\frac{I}{K'}\right)}\right]\right\} \times \frac{(v_1 - v_2)^3}{16\sqrt{\left(\frac{I}{K'}\right)}} - (1 + 2\delta)(1 + 3\delta)\theta'\frac{(v_1 - v_2)^3}{16}\right\} \quad (6)$$

As predicted, the dominant bias dependent cubic distortion term appears with opposite polarity to that in eqn. 5. Thus when the branch currents are summed to give

$$i = i_1 + i_2 = 2K'\left\{\sqrt{\left(\frac{I}{K'}\right)}(v_1 - v_2) + \left[\delta - (1 + 2\delta)\theta'\sqrt{\left(\frac{I}{K'}\right)}\right]\frac{(v_1 - v_2)^2}{4} - (1 + 2\delta)(1 + 3\delta)\theta'\frac{(v_1 - v_2)^3}{16}\right\} \quad (7)$$

the linear and quadratic terms are doubled, but cancellation reduces the cubic term to a form which is no longer strongly dependent on the bias level.

Simulation results: Distortion characteristics for SPQR and SPR networks have been assessed using Level 3 SPICE device models [7] with mobility factor $\theta = 0{\cdot}15\,\mathrm{V}^{-1}$ and bulk modulation parameter $\gamma = 0{\cdot}65\,\mathrm{V}^{1/2}$. For both cases, the channel lengths and bias currents were chosen so as to equalise the nominal resistance values and quiescent buffer voltage levels.

The distortion curves given in Fig. 3 are based on ± 5 V supplies and were obtained by holding the aspect ratios constant at $W/L = 10/50$, and 10/25 for the SPQR and SPR structures, respectively, and controlling the resistance levels via the bias currents. The simulation results predict that THD levels in the SPQR network would be significantly lower than those for the SPR structure across the entire tuning range. It is interesting to note that some cancellation of mobility and bulk modulation related distortion terms occur in the SPQR network producing a distortion minimum of -67 dB.

As the levels of distortion indicated in Fig. 3 rely on cancellation of large cubic contributions in the case of the SPQR network, the effect of device mismatching could be critical. However, simulation studies have shown that in the face of worst case geometrical mismatches of 2%, distortion levels in the SPQR would increase by around 7 dB to a mean of -55 dB representing an improvement over the SPR of approximately 15 dB.

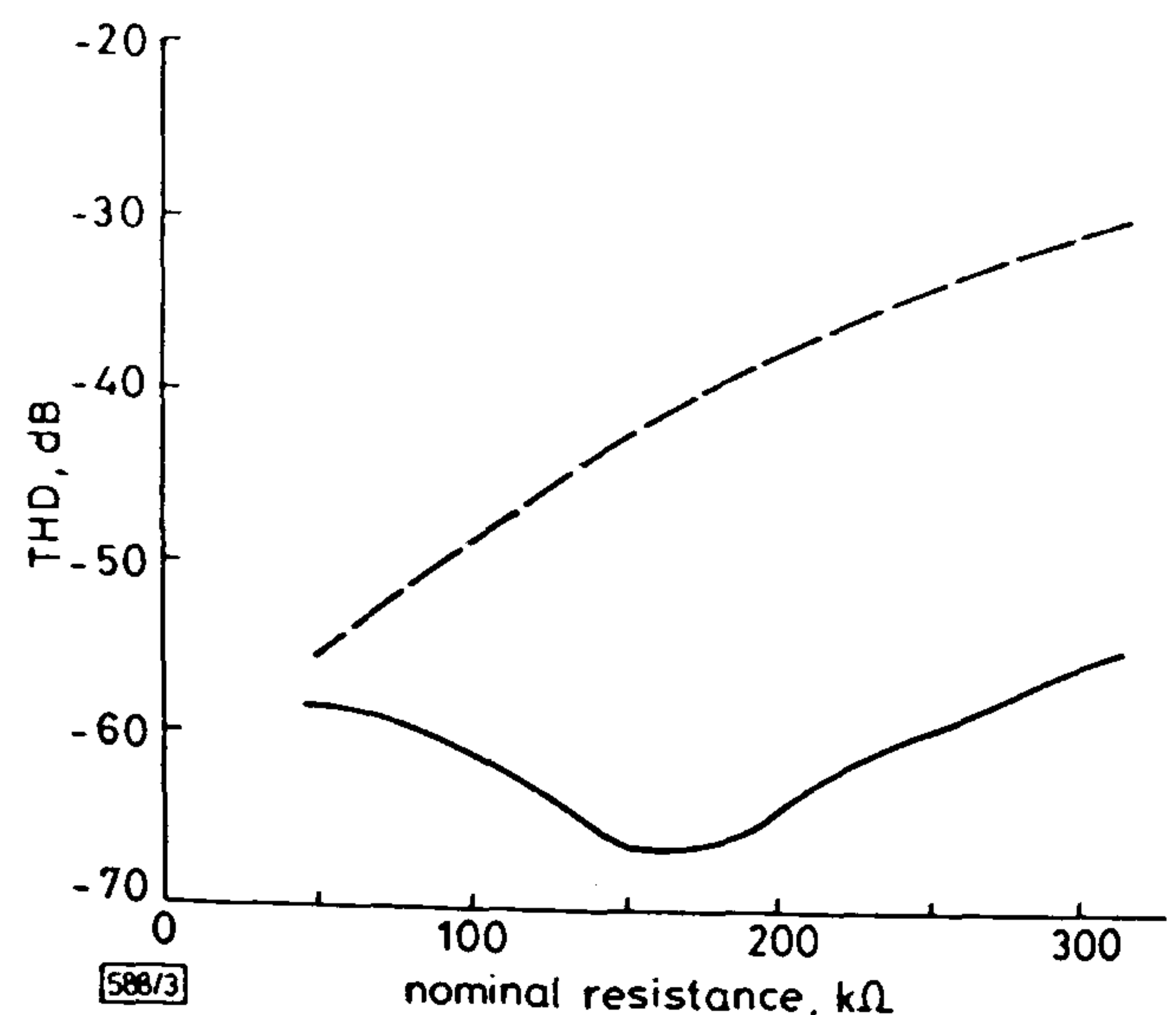

Fig. 3 *Variation of THD with nominal resistance*
$f_0 = 1$ kHz, $v = 0{\cdot}5$ V peak to peak
– – – – series pair
—— series/parallel quad

With the channel lengths in a 1 : 2 ratio the SPR and SPQR silicon area ratio (based on 1 and 3 matched buffers, respectively) is approximately 3 : 16. It will be appreciated therefore that although the SPQR offers low distortion, the SPR enjoys an area advantage which could also reflect in a potential for operation at higher frequencies.

Conclusions: A new CMOS floating resistor scheme has been described which is insensitive to threshold and bulk modulation parameters and features very low distortion levels. The resistor which is easy to design, can be tuned over a wide range of resistance values and should prove attractive in single ended applications.

13th December 1991

G. Wilson and P. K. Chan (*Polytechnic South West, School of Electronic, Communication and Electrical Engineering, Plymouth, Devon PL4 8AA, United Kingdom*)

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Mobility Degradation Effects in CMOS Differential Pair Transconductors

P.K. CHAN AND G. WILSON
School of Electronic Communication and Electrical Engineering, Polytechnic South West, Plymouth, Devon, UK

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Abstract. The influence of the mobility reduction factor on the dominant third-harmonic distortion and effective transconductance in CMOS differential pair transconductors is examined. Analytical expressions are developed which are suitable for hand calculation and generate realistic estimates for distortion and transconductance. The results produced have been tested against SPICE simulations over a wide range of parameter values and show excellent agreement. The analysis highlights the importance of mobility degradation and reveals that the linearity of the source-coupled differential pair is actually improved as the mobility reduction factor increases. This surprising finding suggests that where $\theta \geq 0.15$, for example, acceptably low distortion levels (< 60 dB for $V_i = 1\ V_{pp}$) should be achievable with the basic long-tailed pair and that complex linearization schemes may be unnecessary.

1. Introduction

It is generally recognized that harmonic distortion is one of the key factors influencing the exploitation of CMOS devices in analog circuit applications. The distortion characteristics for the classical differential pair transconductor of figure 1, a key component in many systems, are therefore not only of considerable intrinsic interest but serve a useful benchmark role. In general, the symmetry of the long-tailed pair normally ensures sufficient rejection of even-order distortion terms, and attention can be focused on the dominant third-order contributions. It is found, however, that distortion estimates based on standard analyses [1-3] often correlate poorly with the levels predicted by SPICE simulations, which usually though not always [4], offer a reliable basis for comparative performance studies. The purpose of this paper is to show that the principal reason for the overly pessimistic estimates lies with the assumption that carrier mobility is constant and that the reduction in mobility, due to its gate field dependence, not only reduces the transconductance but actually plays an important role in suppressing third-harmonic distortion. This, it may be noted, is in sharp contrast with other well-known linearized transconductors [5-9], where mobility degradation is a fundamental cause of odd-order distortion.

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In Section 2, we present an analysis of the differential pair with mobility reduction taken into account and produce expressions for third-harmonic distortion and effective transconductance which are suitable for hand calculation. Section 3 compares the results from a series of SPICE simulations with the theoretical predictions and considers the implications for transconductor design.

2. Differential Pair Analysis

Consider the matched differential pair with constant current sink shown in figure 1. In the following analysis it will be assumed that the output current mirror is ideal, and effects such as channel length modulation, bulk modulation, and velocity saturation, etc., are negligible. With the devices operating in saturation, the adoption of a square-law model, which includes mobility degradation, leads to expressions which are suitable for hand analysis and for design purposes.

It will be shown that the constant-current biasing has the equivalent voltage-source-based representation shown in figure 2. The dc source V_Q models the quiescent bias of the differential pair, while the pair of ac voltage sources defines the complex signal appearing at node P consisting of the common-mode ac component $v_c = (v_1 + v_2)/2$ and a nonlinear generator v_n. The common-mode component results from the symmetry and source-follower-like structure of the differential

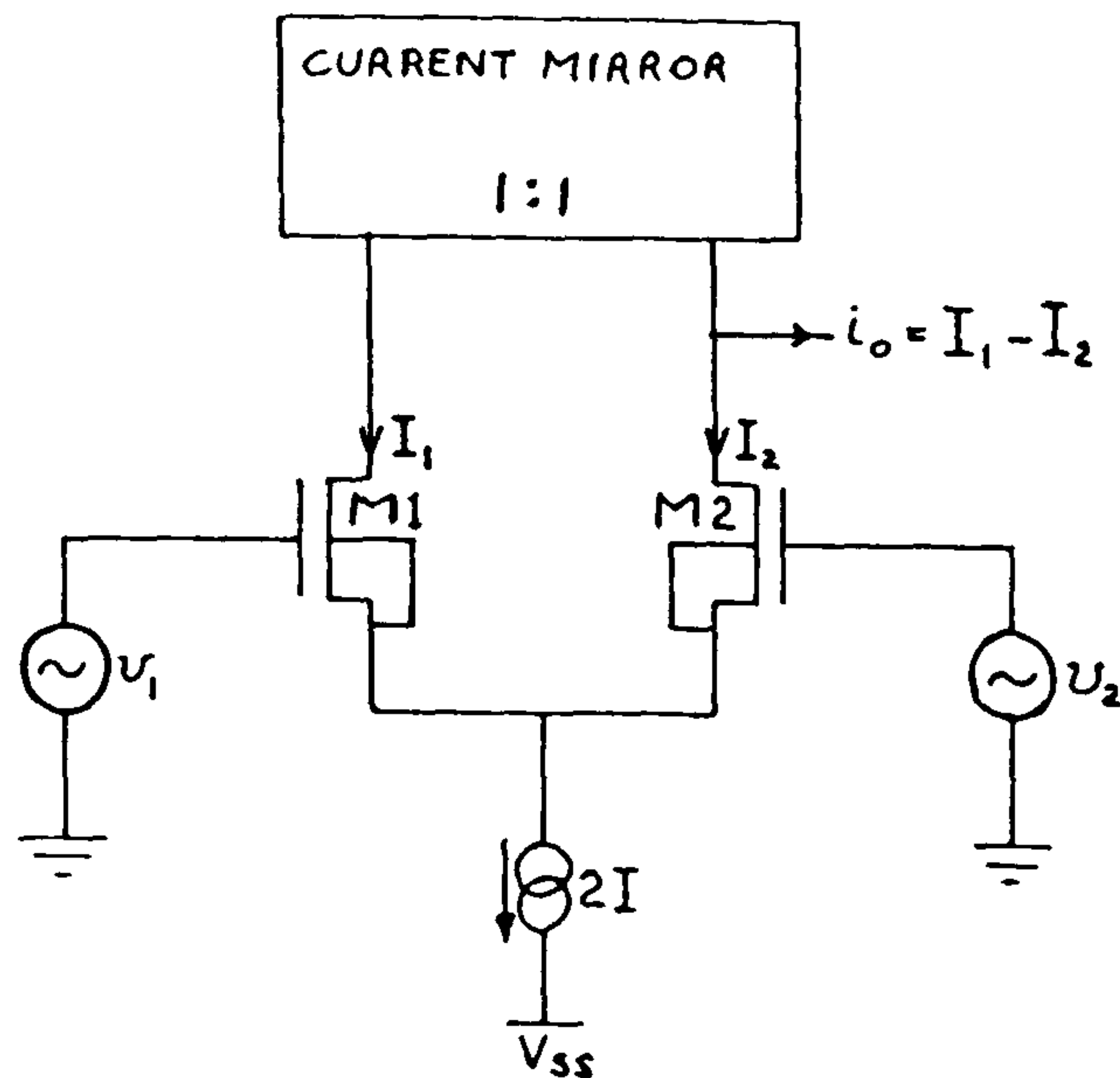

Fig. 1. The differential pair transconductor with constant-current biasing.

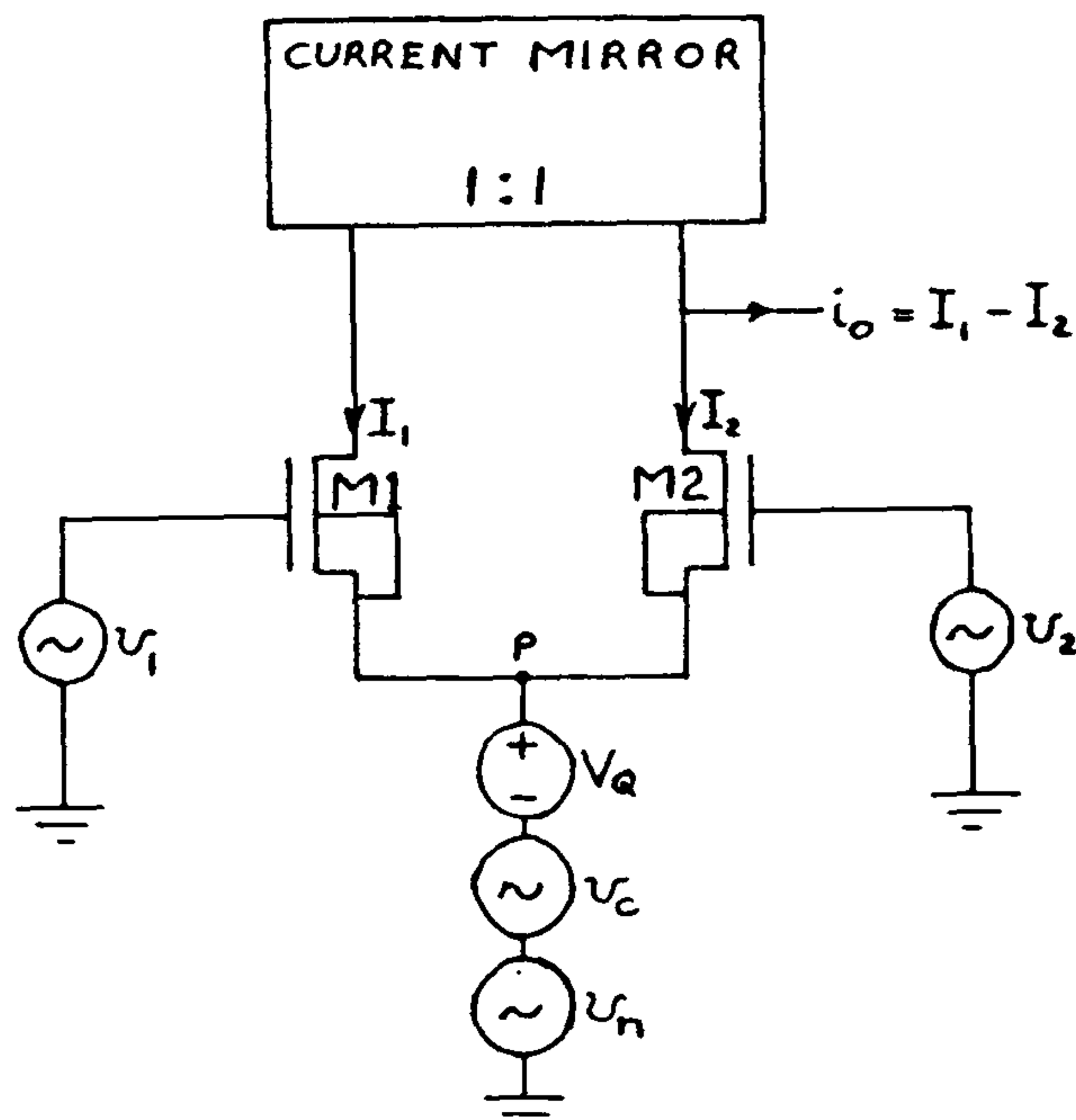

Fig. 2. The differential pair under equivalent voltage source excitation.

pair, whereas the nonlinearity is due to the absence of even-order distortion terms in the drain currents. Expressions for V_Q and v_n can be developed as follows.

Consider the differential pair under steady-state conditions; the quiescent drain current for the transistors can be expressed as

$$I = \frac{K_{oc}}{1 + \theta(V_{GS} - V_T)} (V_{GS} - V_T)^2 \quad (1)$$

where

$$K_{oc} = \frac{K_o}{1 + \delta} \quad (2)$$

is the effective transconductance parameter and $\delta = \gamma/4\sqrt{\phi - V_{BS}}$ is the drain current correction factor, γ is the body factor, ϕ is the surface potential, V_{BS} is the body-to-source voltage, $K_o = \mu_o C_{OX} W/2L$ is the transconductance parameter under zero-gate-field conditions, μ_o is the corresponding carrier mobility, C_{OX} is the oxide capacitance per unit gate area, W is the channel width, L is the channel length, V_{GS} is the quiescent gate-to-source voltage, V_T is the device threshold voltage, and θ is the gate-field-dependent mobility reduction factor.

Equation (1) can be solved for the quiescent gate-to-source overdrive as

$$V_b = V_{GS} - V_T = \frac{\theta I}{2K_{oc}} + \sqrt{\frac{I}{K_{oc}}(1 + \frac{\theta^2 I}{4K_{oc}})} \quad (3)$$

in which case

$$V_Q = -V_{GS} = -(V_b + V_T) \quad (4)$$

To quantify the nonlinearity v_n, consider the drain currents under ac conditions; they are

$$I_1 = \frac{K_{oc}}{1 + \theta(v_{gs1} - V_T)} (v_{gs1} - V_T)^2 \quad (5)$$

$$I_2 = \frac{K_{oc}}{1 + \theta(v_{gs2} - V_T)} (v_{gs2} - V_T)^2 \quad (6)$$

where

$$v_{gs1} = v_1 - v_c - V_Q - v_n = \frac{v_i}{2} + V_b - v_n + V_T \quad (7)$$

$$v_{gs2} = v_2 - v_c - V_Q - v_n = -\frac{v_i}{2} + V_b - v_n + V_T \quad (8)$$

with

$$v_i = v_1 - v_2. \quad (9)$$

Given

$$I_1 + I_2 = 2I \quad (10)$$

an approximation to v_n can be obtained as

$$v_n \approx \frac{1}{4V_b(1 + \theta V_b)(2 + \theta V_b)} v_i^2 + \textit{higher order terms in } v_i^2 \quad (11)$$

Thus, the constant sum nature of the drain currents is reflected in the generation of a nonlinear potential v_n comprising an infinite series of terms in v_i^2, of which we retain only the first.

Subtracting (6) from (5) and solving for the signal current gives

$$i_o = I_1 - I_2 = g_1 v_i + g_3 v_i^3 \quad (12)$$

where

$$g_1 = \frac{(2 + \theta V_b)}{(1 + \theta V_b)^2} K_{oc} V_b \quad (13)$$

and

$$g_3 = -\frac{1 + (1 + \theta V_b)^2}{(2 + \theta V_b)(1 + \theta V_b)^4} \frac{K_{oc}}{4V_b} \quad (14)$$

Since the quiescent gate overdrive V_b increases monotonically with θ, it can be seen that mobility degradation has a pronounced effect on the relative magnitude of the nonlinear term g_3 and, in consequence, on the harmonic distortion. The influence of θ on V_b, g_1, and g_3 (normalized with respect to their $\theta = 0$ values) is illustrated in figure 3 for $I = 25\ \mu A$ and $K_{oc} = 8.53\ \mu A/V^2$. It is particularly noteworthy that over the range $0 < \theta \leq 0.25$, V_b increases by around 26%, whereas the linear transconductance falls by 35%; the g_3 coefficient, on the other hand, reduces by a factor of 6!

The resulting harmonic distortion, which can be defined[1] for the sinusoidal signal $v_i = V_p \sin \omega t$ as

$$HD3 = \frac{1}{4}\left|\frac{g_3}{g_1}\right| V_p^2 \times 100\% \quad (15)$$

can be written in the form

$$HD3 = \frac{1 + 1/(1 + \theta V_b)^2}{(2 + \theta V_b)^2} \left[\frac{V_p}{4V_b}\right]^2 \times 100\% \quad (16)$$

and reduces to the "standard" [1-3] estimate:

$$HD3 = \frac{K_o}{32I} V_p^2 \times 100\% \quad (17)$$

on setting θ and δ to 0.

3. Results and Discussion

A series of SPICE simulations using level 3 device models have been made, and the validity of the equivalent voltage source model adopted in the forgoing analysis has been established. Simulation predictions for the transconductance coefficient g_1 are shown superimposed on the computed result in figure 3, and demonstrate a remarkable concurrence.

The variation of third harmonic distortion as a function of the quiescent drain current is illustrated in figure 4. The figure shows the estimates given by SPICE

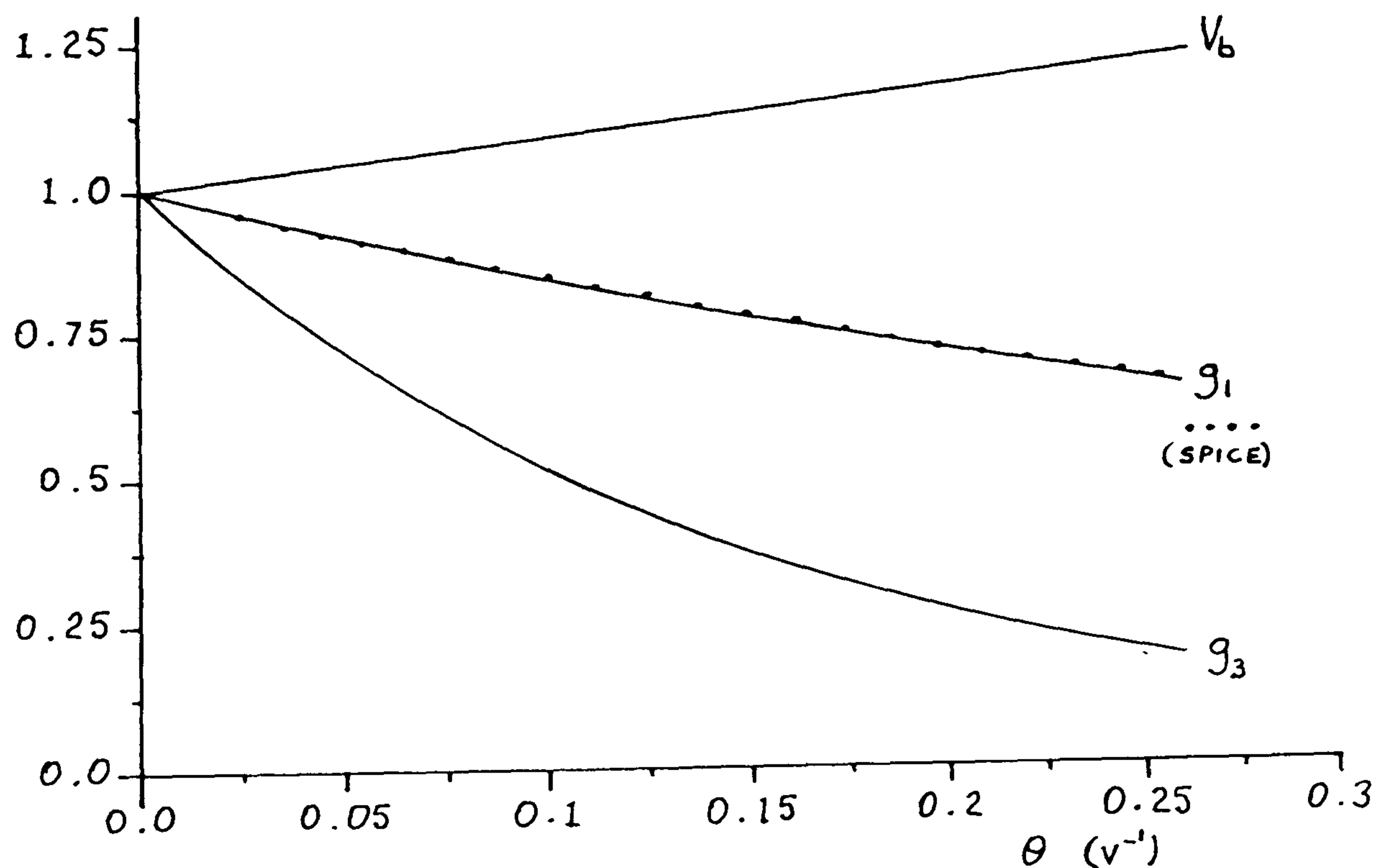

Fig. 3. Variation of quiescent gate overdrive and transconduction coefficients (normalized with respect to their $\theta = 0$ values) with mobility reduction factor.

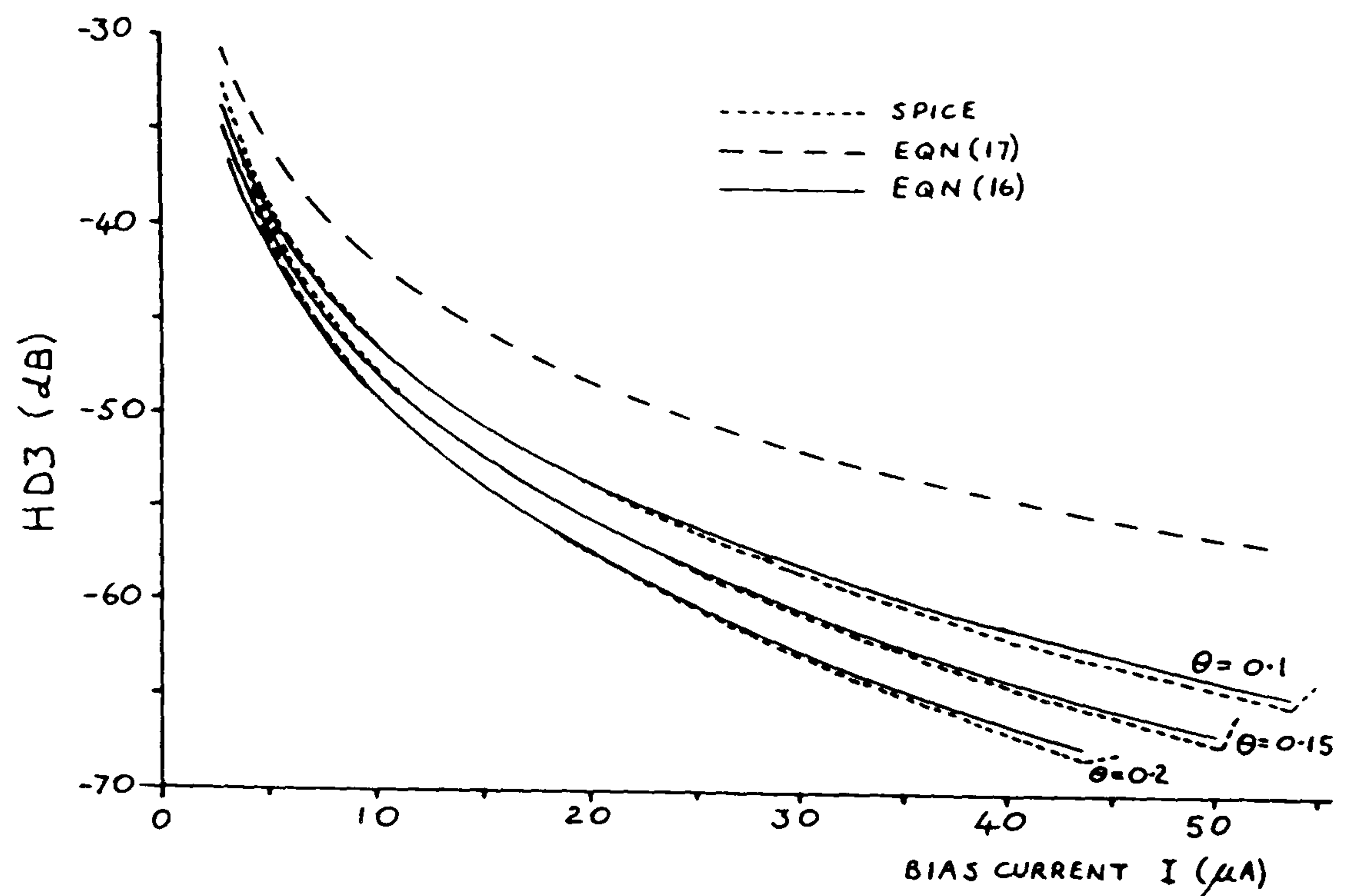

Fig. 4. Third harmonic distortion versus bias current at 1 kHz with a 1 V_{pp} input signal and a 10 μm/30 μm aspect ratio.

together with those from equations (16) and (17) for three values of the mobility degradation factor. Although equation (17) indicates a reduction of distortion with increasing bias current, the constant-mobility assumption produces results which are significantly pessimistic and unreliable for design purposes. In contrast, however, the distortion estimates from equation (16) are in excellent agreement with the SPICE simulations. The agreement has been found to hold over a wide range of design parameter values, and, in general, equation (16) is reliable provided that the differential pair elements are not driven into cutoff and the current mirror/sink devices remain in saturation.

It may be noted that at higher bias current levels the computed distortion results are marginally pessimistic. This discrepancy is largely due to the exclusion of velocity saturation effect and channel length modulation from the analysis. However, as figure 4 suggests, these effects are small, and equation (16) should prove sufficiently accurate for long-channel devices.

The observation that distortion reduces as mobility degradation increases is at variance with the behavior of some other linearized saturation-mode or non-saturation-mode transconductors where distortion increases with the mobility reduction factor. This raises the interesting question as to whether differential-pair-based transconductors can be designed with acceptable distortion without resorting to linearization. The simulation studies have shown that linearity can be improved by 10 dB or more by employing processes with higher θ levels together with an appropriate choice of bias current and aspect ratios.

Although mobility factor is a technology-dependent constant and cannot be modified by the circuit designer, where several process options are available the simplicity and low power consumption of the differential pair could make it an attractive candidate for a silicon efficient transconductor design. However, as can be inferred from figure 4, the lower distortion levels are associated with a reduction in tunability for a given transconductance. This aspect could be critical as for example, in OTA-C filter applications where the designer must ensure an adequate tuning facility to compensate for fabrication tolerance and temperature variations.

4. Conclusions

The effect of mobility degradation on transconductance and harmonic distortion in long-tailed pair transconductors has been examined, and analytic expressions have been developed which are amenable to hand calculation and produce results which agree with SPICE

simulations. The analytic expressions clarify the effects of mobility degradation and suggest that higher levels may be advantageous in lowering third-harmonic distortion. Extensive comparison with SPICE simulation studies have shown that the derived expressions provide a quick and effective means for estimating circuit performance. The expressions can be easily extended to differential pairs driving nonideal loads such as depletion load transistors with body effect.

Notes

1. This definition ignores the relatively small contribution to the fundamental from the expansion of the cubic term.

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George Wilson received the B.Sc. and Ph.D. degrees in electrical engineering from Sunderland Polytechnic in 1970 and 1973, respectively. From 1974 to 1983 he was an academic staff member at James Cook University (North Queensland, Australia) and took up a lecturing position in the Department of Electronics and Information Engineering at Southampton University (UK). He joined the Department of Electrical and Electronic Engineering as reader in electronics in 1987. His research interests include circuit theory, electronic filters and solid state circuits. Dr. Wilson is a member of the IEE and senior member of the IEEE.

P.K. Chan received the B.Sc. degree from the University of Essex, in 1987, and the M.Sc. degree from the University of Manchester Institute of Science and Technology (UMIST) in 1988. Since 1989 he has been a research assistant with the Polytechnic South West, and is studying toward the Ph.D. degree in the area of MOS continuous-time filters. His research interests include analog integrated circuit design and circuit theory.

IEE Colloquium, Sept., 1992

A FAMILY OF CMOS LINEAR RESISTORS

P K Chan and G Wilson

1. Introduction

It is known that quadratic distortion in the drain current for MOSFET devices operating in the so-called linear region can be suppressed either by applying suitably scaled terminal signals to the gate (with the bulk node held at an appropriate dc bias level; usually V_{DD} or V_{SS}) or by driving **both** the gate and bulk nodes with unscaled signals. This contribution describes a range of CMOS resistor structures based on a building blocks consisting of buffered linear-mode transistors in which the gates and bulks are simultaneously modulated.
The n-channel buffered resistor (BR) in Fig.1 comprises a single transistor having its gate and bulk nodes driven by a buffer [1] constructed from identical devices. With a common input v, the buffer provides outputs: $v_g = v + V_G$ and $v_b = v - V_B$ where:

$$V_G = \sqrt{\frac{I}{K}} + V_T\,, \quad V_B = \sqrt{\frac{I}{K}} + V_{TO} \text{ and } V_T = V_{TO} - \gamma\sqrt{\phi_B} + \gamma\sqrt{\phi_B + V_B}\,.$$

2. Buffered-resistor analysis.

A third-order approximation to the drain current can be written as:

$$I_d = 2K\left[\left(v_{gs} - V_t\right)v_{ds} - \left(1 + \frac{\gamma}{2\sqrt{\phi_B + v_{sb}}}\right)\frac{v_{ds}^2}{2} + \frac{\gamma v_{ds}^3}{24\sqrt{\left(\phi_B + v_{sb}\right)^3}}\right] \quad ...(1)$$

where $V_t = V_{TO} - \gamma\sqrt{\phi_B} + \gamma\sqrt{\phi_B + v_{sb}}$ is the threshold potential, $K = \frac{\mu C_{ox} W}{2L}$ with $\mu = \frac{\mu_o}{1 + \theta\left(v_{gs} - V_t\right)}$. γ and θ are the body-effect coefficient and mobility-degradation factors respectively. When potentials: $v_g = v + V_G$ and $v_b = v - V_B$ are applied to the gate and bulk terminals, the transconductance factor becomes:

$$K = \frac{K_o'}{1 + \theta'[m(v - v_s) + \frac{\gamma(v - v_s)^2}{8\sqrt{\left(\phi_B + V_B\right)^3}}]} \quad ...(2)$$

P K Chan and G Wilson are with the School of Electronic, Communication & Electrical Engineering, University of Plymouth, Devon.

with: $K_o' = \frac{\mu_o' C_{ox} W}{2L}$, $\mu o' = \frac{\mu_o}{1+\theta\sqrt{\frac{I}{K}}}$, $\theta' = \frac{\theta}{1+\theta\sqrt{\frac{I}{K}}}$ and $m = 1 + \frac{\gamma}{2\sqrt{\phi_B + V_B}}$.

The cubic approximation for I_d can subsequently be expressed as:

$$I_d = 2\sqrt{\frac{I}{K}} K_o' \left\{ \begin{array}{c} \left(v_d - v_s\right) - \frac{m}{2\sqrt{\frac{I}{K}}}\left(v_d + v_s - 2v\right)\left(v_d - v_s\right) - \theta' m (v - v_s)\left(v_d - v_s\right) \\ + \frac{\gamma}{24\sqrt{\frac{I}{K}}\sqrt{\left(\phi_B + V_B\right)^3}}\left[\left(v_d - v\right)^3 - (v_s - v)^3\right] + \frac{m^2\theta'}{2\sqrt{\frac{I}{K}}}(v - v_s)\left(v_d + v_s - 2v\right)\left(v_d - v_s\right) \\ + \frac{\theta'\gamma}{8\sqrt{\left(\phi_B + V_B\right)^3}}(v - v_s)^2\left(v_d - v_s\right) \end{array} \right\} \quad ...(3)$$

3 Parallel Form Resistor (PFR)

The parallel connection of a BR pair as shown in Fig.2 takes the terminal potentials as the buffer inputs [2]. For the BR.1 block the relevant potentials are : $v = v_d = v_1$, $v_s = v_2$ and by substitution into Eq.3 the current is:

$$I_1 = 2\sqrt{\frac{I}{K}} K_o' \left[\begin{array}{c} (v_1 - v_2) + \left[\frac{m}{2\sqrt{\frac{I}{K}}} - \theta' m\right](v_1 - v_2)^2 \\ + \left[\frac{\gamma}{24\sqrt{\frac{I}{K}}\sqrt{\left(\phi_B + V_B\right)^3}} - \frac{m^2\theta'}{2\sqrt{\frac{I}{K}}} + \frac{\theta'\gamma}{8\sqrt{\left(\phi_B + V_B\right)^3}}\right](v_1 - v_2)^3 \end{array} \right] \quad ...(4)$$

For the BR.2 block the potentials are: $v = v_s = v_2$ and $v_d = v_1$ in which case:

$$I_2 = 2\sqrt{\frac{I}{K}} K_o' \left[(v_1 - v_2) - \frac{m}{2\sqrt{\frac{I}{K}}}(v_1 - v_2)^2 + \frac{\gamma}{24\sqrt{\frac{I}{K}}\sqrt{\left(\phi_B + V_B\right)^3}}(v_1 - v_2)^3 \right] \quad ...(5)$$

Several interesting features can be seen in these expressions including, the absence of mobility degradation in BR.2. It can also be seen that the quadratic distortion term in I_2 appears in I_1 but with reversed sign and it follows that this major distortion source will be absent in the sum current:

$$I = I_1 + I_2 = 4\sqrt{\frac{I}{K}} K_o' \left[\begin{array}{c} (v_1 - v_2) - \frac{\theta' m}{2}(v_1 - v_2)^2 + \\ \left[\frac{\gamma}{24\sqrt{\frac{I}{K}}\sqrt{\left(\phi_B + V_B\right)^3}} - \frac{m^2\theta'}{4\sqrt{\frac{I}{K}}} + \frac{\theta'\gamma}{16\sqrt{\left(\phi_B + V_B\right)^3}}\right](v_1 - v_2)^3 \end{array} \right] \quad ...(6)$$

This result shows that the linearization process completely suppresses the quadratic distortion due to **body effect** but that a **mobility** dependent term will remain. Given that the nominal resistance would be tuned by adjusting the buffer current I, it will be seen that the quadratic distortion is unaffected by the tuning process but that the cubic nonlinearity will increase as the PFR is tuned for higher resistance levels.

4. Series Form Resistor (SFR)

Series form resistors can be configured as a series connection of BR's with the buffer inputs connected to the external terminals as in Fig.3(a) or commoned to the mid-point node [1] shown as Fig.3(b). We will refer to the latter form which requires only a single buffer as SFR-1 and the double-buffer resistor as SFR-2. It will be appreciated that since the alternative arrangements are a simple juxtaposition of electrically identical blocks, their small-signal terminal characteristics are identical. The SFR current can be found as:

$$i=\sqrt{\frac{I}{K}}K_o'\left\{\left(v_1-v_2\right)-\frac{m\theta'}{4}\left(v_1-v_2\right)^2-\left[\frac{m^2}{8\frac{I}{K}}\left\{1-\theta'\sqrt{\frac{I}{K}}\right\}-\frac{\gamma}{96\sqrt{\frac{I}{K}}\sqrt{\left(\phi_B+V_B\right)}}\right]\left(v_1-v_2\right)^3\right\} \quad ...(7)$$

By comparison with the PFR expression it can be seen that the quadratic (mobility related) distortion term is halved in the SFR. More importantly however, the SFR has a cubic term inversely proportional to the bias current and simulation studies have shown that this component is large enough to dominate the distortion performance over much of the tuning range and particularly at higher resistance values. It will be appreciated that the reduced mobility effect arises from the distribution of the signal over the pair of BR's. Thus with the mid-point potential approximately equal to the common-mode level, v_{gs} is half the terminal difference as compared with the full terminal voltage in the PFR.

5 Series-Parallel Form Resistors (SPFR's)

We have noted that the SFR offers reduced mobility-related distortion but suffers from a large cubic nonlinearity. The obvious method of reducing mobility-related distortion is to form a series connection of a pair of identical PFR's as shown in Fig.4(a). The terminal potential would therefore be distributed equally across each PFR with a corresponding reduction in distortion. Similarly, as shown in Fig.4(b), parallelling series pairs of identical BR's would achieve the same end. As the mid-point potentials are the common-mode signal, replacing the difference: $(v_1- v_2)$ in Eq.6 with $(v_1-v_2)/2$ gives the SPFR current as:

$$I=2\sqrt{\frac{I}{K}}K_o'\left[\begin{array}{c}(v_1-v_2)-\frac{\theta' m}{4}(v_1-v_2)^2+\\ \left[\frac{\gamma}{96\sqrt{\frac{I}{K}}\sqrt{\left(\phi_B+V_B\right)^3}}-\frac{m^2\theta'}{16\sqrt{\frac{I}{K}}}+\frac{\theta'\gamma}{64\sqrt{\left(\phi_B+V_B\right)^3}}\right](v_1-v_2)^3\end{array}\right] \quad ...(8)$$

Comparison with Eq.6 shows that for these structures, the quadratic term is halved, and the cubic terms reduced by a factor of four. Although these low-distortion resistors would appear to require a total of four buffers, this number can be reduced to three since a single buffer can drive the pair of transistors buffered from the mid-point node. The optimized networks are shown as Fig.4(c) and Fig.4(d) and differ only in that the mid-point nodes are ohmically connected in Fig.4(c).

The fifth member of the family [3] shown as Fig.4(e), is particularly interesting in that its upper section is identical to SFR-2 and therefore generates a potentially large bias-dependent cubic nonlinearity. However, the lower branch current contains an identical cubic term **but with reversed sign** and the total SPFR current is:

$$i = 2\sqrt{\frac{I}{K}}K'_o \left\{ \begin{array}{c} (v_1 - v_2) - \frac{m\theta'}{4}(v_1 - v_2)^2 - \frac{\theta' m^2}{8\sqrt{\frac{I}{K}}}\left\{1 - \theta'\sqrt{\frac{I}{K}}\right\}(v_1 - v_2)^3 \\ + \frac{\gamma}{96\sqrt{\frac{I}{K}}\sqrt{(\phi_B + V_B)}}(v_1 - v_2)^3 \end{array} \right\} \quad ...(9)$$

A comparison with Eq.6 shows that the quadratic distortion coefficients for this SPFR are reduced by a factor of two relative to those of the PFR; a direct result of lowering the potential across individual transistors.

6 Summary.

The preceding analyses have shown that several structures offer reduced distortion by suppressing or cancelling the major quadratic components and that the quadratic nonlinearity due to mobility degradation can be minimized by distributing the external signal across two (or more) devices. The results are based on matched devices and in practice the distortion levels achieved will be degraded due to imperfect cancellation. In the case of the SFR's however, the increased distortion levels at low bias currents will mask increases due to small mismatches. At the lower distortion levels achieved by the other members of the family, mismatching can be a significant problem.

[1] P M Vanpeteghem & P L Rice, "New CMOS resistor implementation for linear IC applications", Elec. Lett., vol.24, no. 5, pp 288-290 march 1989.

[2] M Banu & Y Tsividis, "Fully integrated active RC filters", Proc. Int Symp. Circuits & Syst., pp 602-605, 1983.

[3] G Wilson & P K Chan, "CMOS series/parallel quad resistor", Elec. Lett., vol.28, pp 335-336, Jan. 1992

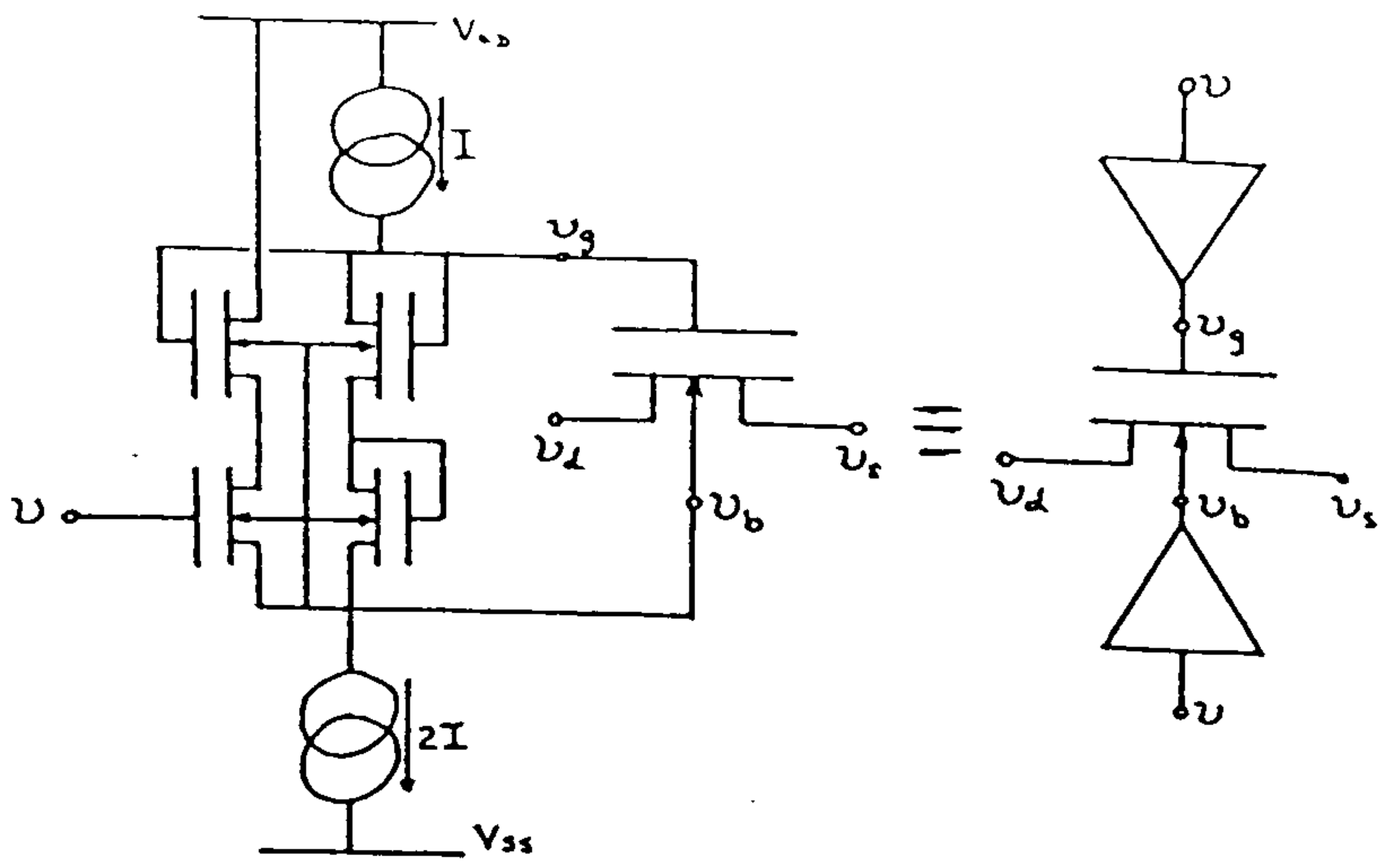

Fig. 1 Buffered Resistor

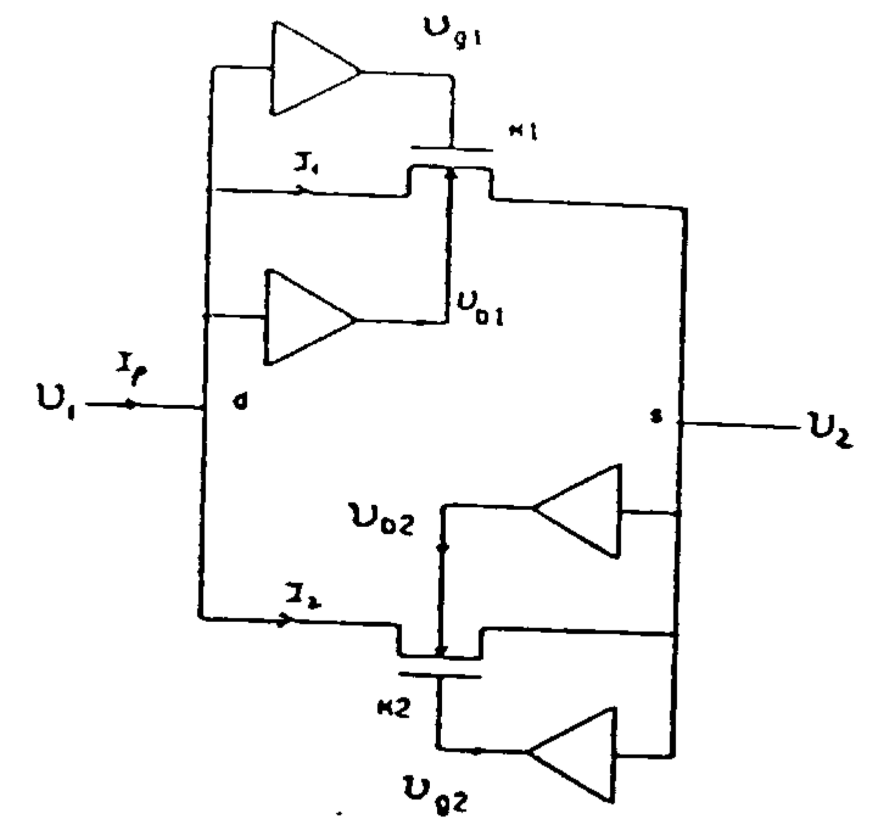

Fig. 2 Parallel Form Resistor (PFR)

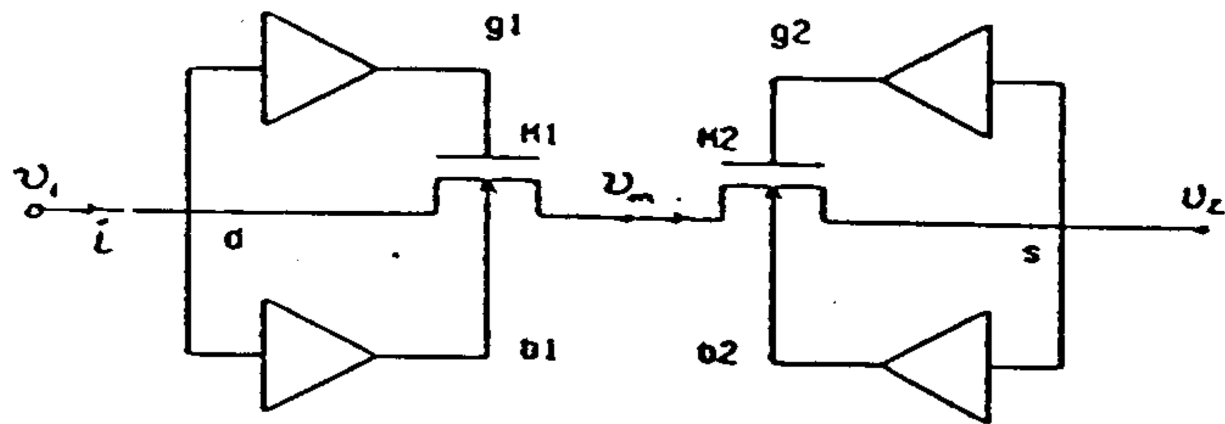

Fig. 3(a) Series Form Resistor (SFR-2).

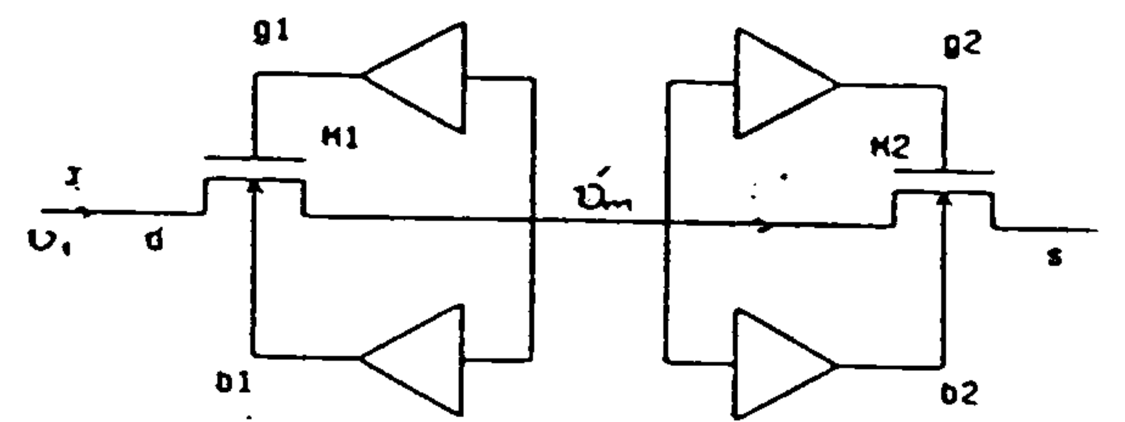

Fig. 3(b) Series Form Resistor (SFR-1).

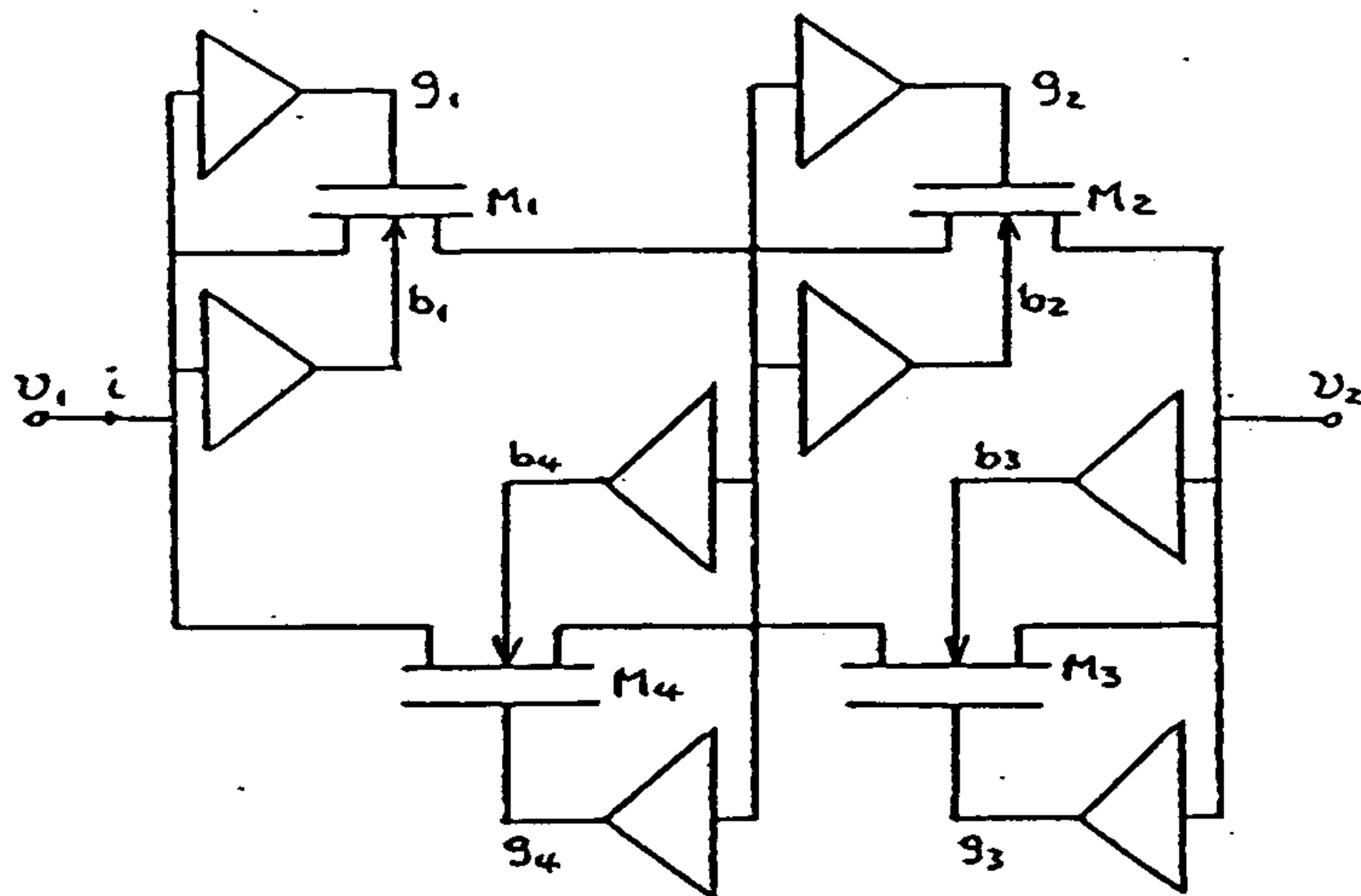

Fig. 4(a) Series-parallel Form Resistor (SPFR-1).

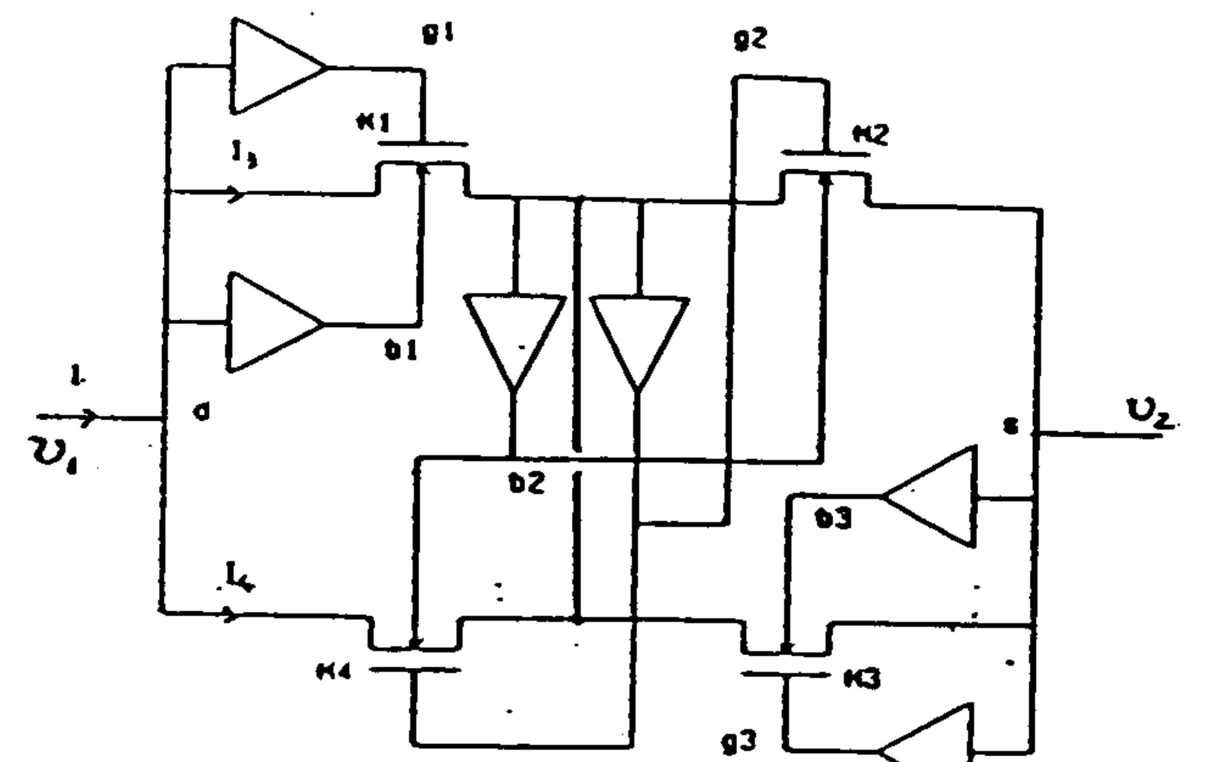

Fig. 4(c) Series-parallel Form Resistor (SPFR-3).

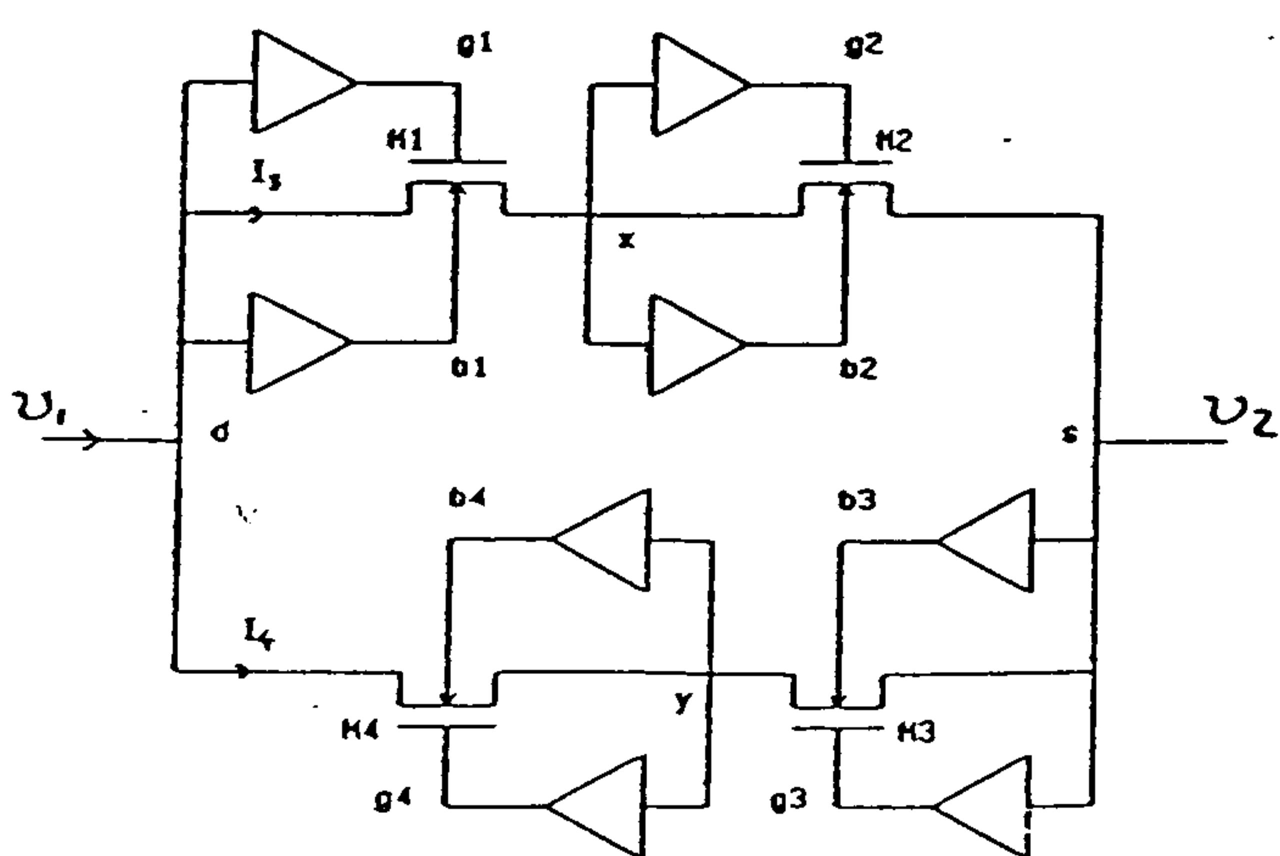

Fig. 4(b) Series-parallel Form Resistor (SPFR-2).

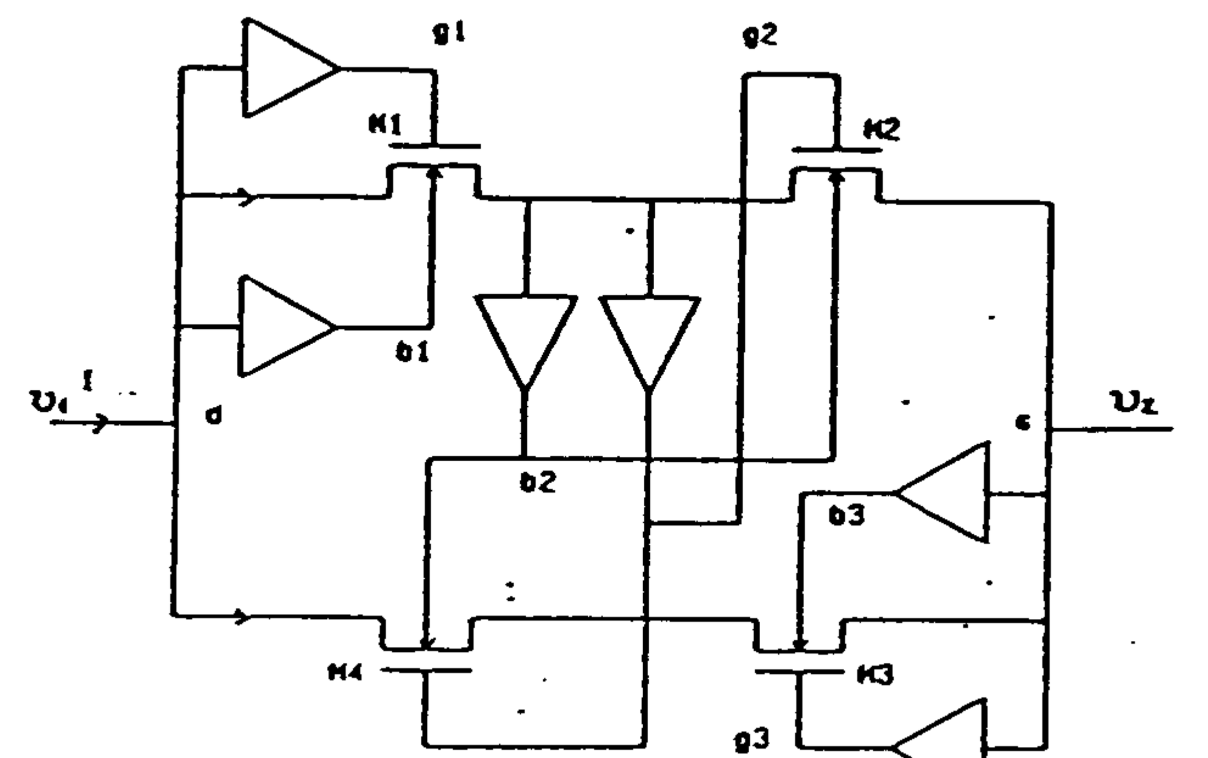

Fig. 4(d) Series-parallel Form Resistor (SPFR-4).

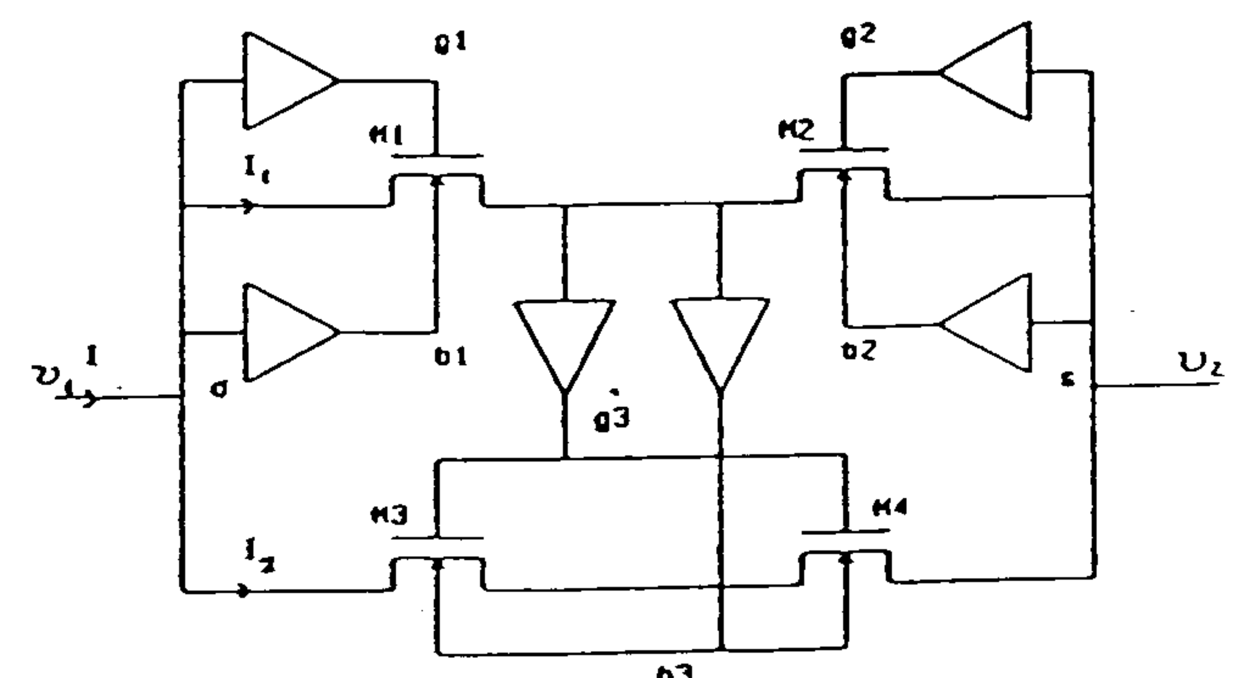

Fig. 4(e) Series-parallel Form Resistor (SPFR-5).