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A Novel Power Conversion Approach for Single Phase Systems

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A Novel Power Conversion Approach for Single Phase Systems

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This thesis is dedicated to

My mother, who sacrificed a lot for me and inspired me the meaning of sacrifice and success

The memory of my father, who taught me the truth of life

My wife, who is the source of happiness in my life and my companion to the way of success

My children, who make my life full of beauty

To all people who I love

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Author's Declaration

At no time during the registration for the degree of Doctor of Philosophy has the author been registered for any other university award without prior agreement of the Graduate Sub-Committee.

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A Novel Power Conversion Approach for Single Phase Systems

Saif AL-Zubaidi

Abstract

A novel single phase rectification technique with a new architecture and control scheme is proposed. The new rectifier consists of switched capacitor branch in parallel with the diode bridge rectifier. The switched capacitor branch includes a capacitor and a bidirectional switch arranged in series so the switch can control the charging and discharging of the capacitor. The control strategy is carefully designed to ensure the output voltage of the rectifier is above a chosen threshold level and to maintain high input power factor with reduced line current harmonics. Circuit configuration, design parameters, principles of operation and the mathematical analysis are presented. The new architecture provides a reduction in the size of the DC side capacitor. This reduction can be as low as less than 10% of the size of the typical smoothing capacitor in the conventional single phase rectifier. The proposed concept is verified by the experimental results over a range of case studies.

A novel buck-boost DC-DC converter architecture is also proposed. This converter utilises the close inversely-coupled inductors topology in both its conversion stages (buck and boost). The new converter aims to reduce the switching noise that usually accompanies the buck and boost circuits. This can be done by maintaining a continuous flow of current in both converter stages which results in a large reduction in the back e.m.f induced in the main inductor and thus reduces the switching noise. The new converter architecture also provides a unique design of the passive clamped circuit. This circuit is used to recycle the leakage energies of the coupled inductors which results in an efficiency improvement of the converter and to limit the voltage stress on the power switches. Circuit configuration, principles of operation and the transfer function are presented. The proposed concept is verified by the experimental and the simulated results of a range of case studies. The highest achieved efficiency observed in the experiments was 97.7%.

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Abbreviations

CCM	Continuous Conduction Mode
$disp_f$	Displacement Factor
$dist_f$	Distortion Factor
e.m.f	Electromotive Force
EMI	Electromagnetic Interference
PF	Power Factor
PFC	Power Factor Correction
PWM	Pulse Width Modulation
rms	Root Mean Square
THD	Total Harmonics Distortion
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

The demand for energy, particularly in electrical form is ever increasing in order to improve the standard of the modern life. Power electronics has already found an important place in modern technology and been used in wide range of applications.

Power electronics can be defined as the application of solid-state electronics for the control and conversion of electric power [1]. Power electronic systems convert electrical energy from the form supplied by a source to the form required by a load. For example, the part of a computer that takes the AC mains voltage and changes it into the 5 V DC required by the logic chip is a power electronic circuit [2].

The main objectives of the power electronics is to process and control the flow of electrical power between a source and a load by supplying an optimally suited voltages and currents for the connected loads [3].

This control involve not just changing the amount of the transmitted power, but it may include changing the nature of the delivered power to the load as in AC to DC or DC to AC conversion processes, or changing the frequency of the AC power as required by the load. [4].

Power electronics has developed rapidly in recent years due to the development of the solid-state electronics devices that are able to switch large currents and withstand large voltages [5].

As the voltage and current ratings and switching characteristics of power semiconductor devices keep improving, the range of applications continue to expand in different areas from hundreds of megawatts down to a few watts for domestics applications. lamp controls; power supplies; industrial drives; transportation; energy storage and electric power transmission and distribution are some of these applications [1, 3].

In any power conversion process the small energy loss and hence high efficiency power conversion is important because of the extra cost of supplying lost energy and the difficulty to get rid of the generated heat by dissipation to air [3]. Although the cost of energy is subject of interest, the most unpleasant consequence of heat generation is that, it must be removed from the system. This consideration imposes the size and weight limits on the power electronic equipment [2].

A power electronic system consists of much more than a power circuit. The block diagram of a typical system is shown in figure 1.1.

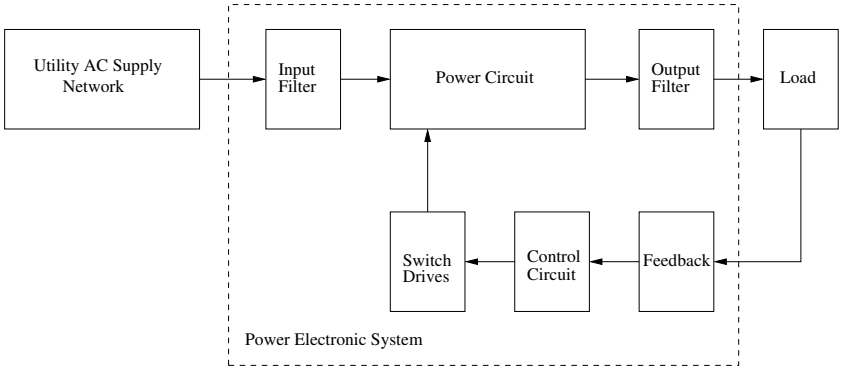


Figure 1.1: Block Diagram of Power Electronic System

Switching may create waveforms with harmonics that may be undesirable because they interfere with proper operation of the load or other equipment, so filters are often employed at the inputs and outputs of the power circuit. The system load which may be electrical or electromechanical is controlled via the feedback signal to the control circuit. The control circuit processes the feedback signal and drives the switches in the power circuit according to the demand of the load [2].

1.1 Definitions

Some definitions widely used in power electronics are listed below

Peak

This is the maximum value attained by any waveform (voltage, current or power) [6].

Average

This is the DC component in the waveform and is described by the following equation for a periodic waveform $v(t)$ of period T.

$$V_{av} = \frac{1}{T}\int_0^T v(t)\ dt \tag{1.1}$$

Root Mean Square (rms)

The rms value is the effective value of a waveform and relates to the power in the waveform. The rms value for a wave $v(t)$ with a period of T is given by equation (1.2).

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T (v(t))^2\ dt} \tag{1.2}$$

Ripple Factor

This is the ratio of the rms value to the absolute value of the DC component of a waveform [6].

$$r_f = \frac{\sqrt{(V_{rms}^2 - V_{av}^2)}}{V_{av}} \tag{1.3}$$

Form Factor

This is the ratio of the rms value to the average value of a waveform [6].

$$f_f = \frac{V_{rms}}{V_{av}} \tag{1.4}$$

Crest Factor

This is the ratio of the peak value to the rms value of a waveform [6].

$$c_f = \frac{V_{peak}}{V_{rms}} \tag{1.5}$$

Total Harmonic Distortion THD

It is normally defined for current and it is the ratio of the sum of the rms values of all harmonics components to the rms value of the current at the fundamental frequency [6].

$$THD = \frac{\sum I_{rms} Harmonics}{I_{rms} Fundamental} \tag{1.6}$$

Power

It is the rate of flow of the energy and normally refers to the average or real power. It can be defined for a given voltage $v(t)$ and current $i(t)$ as

$$P_{av} = \frac{1}{T} \int_0^T v(t) \cdot i(t)\ dt \tag{1.7}$$

Apparent Power or Volt-Amperes

This is the product of the rms voltage and the rms current [6].

$$P_{va} = V_{rms} \cdot I_{rms} \tag{1.8}$$

Power Factor

This is the ratio of the average power flowing to the load, to the apparent power in the circuit [6].

$$pf = \frac{P_{av}}{P_{va}} \tag{1.9}$$

Volt-Ampere Reactive

This is the power flowing into the reactive loads [6].

$$Q_{va} = \sqrt{P_{va}^2 - P_{av}^2} \tag{1.10}$$

Displacement Angle

This is the angle between the fundamental component of the input current and the input voltage [6]. It can be denoted by ϕ_d.

Displacement Factor

This is the cosine of the displacement angle [6].

$$disp_f = cos(\phi_d) \tag{1.11}$$

Distortion Factor

This is the ratio of the power factor to the displacement factor [6].

$$dist_f = \frac{pf}{disp_f} \tag{1.12}$$

1.2 Introduction to Rectifier Circuits

The rectifier circuit is the workhorse of the power electronic circuits, it links an AC supply to a DC load by converting an alternating voltage from the supply to a direct voltage to the load [7]. The obtained DC voltage is not normally level as from a battery, it contains an alternating ripple component imposed on the mean level [4]. The type of load connected to the rectifier terminals has an important effect on the behaviour of the circuit and on the imposed duty of the rectifier elements. For example, the load may be a pure resistive, capacitive or inductive, or it may consist of combination of resistance, inductance and capacitance. Each type of load provides different requirements in the application of the rectifier circuit. A study of the relations between the current and voltage waveforms in typical rectifier circuits with different loading conditions is demonstrated in many handbook of power electronics. This study leads to more understanding of the circuits behaviour [1,3,8].

Various circuit architectures are described in this section, although all give a DC output, but they differ in regards to the AC ripple at the output, the average voltage level, efficiency and their loading effects on the AC supply [2,4].

Rectifiers are usually considered in two groups, half-wave rectifiers where current is drawn from the supply during one half of the cycle and full-wave rectifiers where both positive and negative half cycles are utilised. The basic single phase half wave rectifier circuit is shown in figure 1.2.

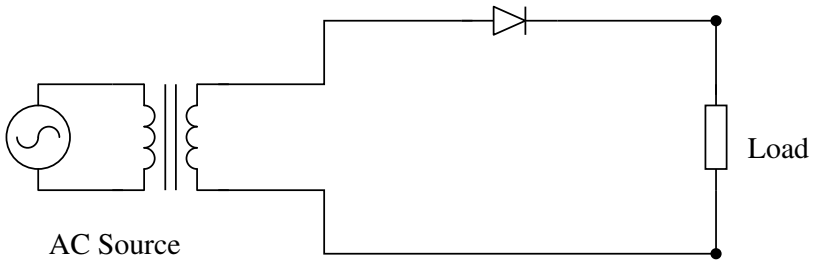


Figure 1.2: A Single Phase Half-Wave Rectifier

However, except at very low power levels, half wave rectifiers are very rarely used [5]. This is to some extent because its output voltage contains ripple at the AC input frequency, which makes filtering more difficult than for other circuits having ripple frequen-

cies that are multiples of the input frequency, but more seriously, the DC load current flows in the secondary of the input transformer. Unless this transformer is designed to carry DC, which is unusual, this may cause saturation of the transformer core with associated power loss and distortion of the voltage waveform. Hence, half wave rectifier will be not considered any further [2, 5].

There are two basic full-wave rectifier circuits, the tapped transformer and the bridge rectifier [1]. The circuit diagram of both circuits are shown in figures 1.3 and 1.4 respectively.

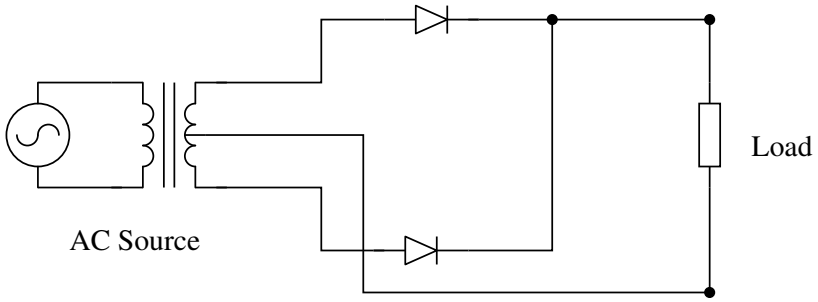


Figure 1.3: A Single Phase Centre-Tapped Transformer Full-Wave Rectifier

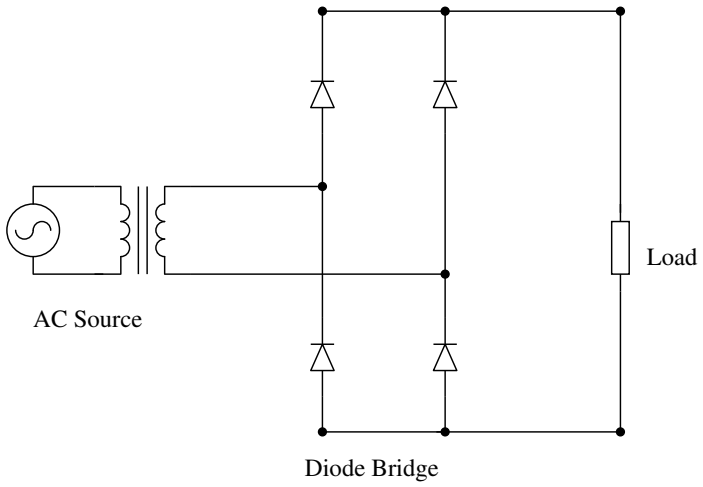


Figure 1.4: A Single Phase Full-Wave Bridge Rectifier

The two circuits will produce the same voltage and current waveforms, but there are two differences. For the bridge rectifier circuit which is commonly used in industrial applications, the load current always flows through two diodes effectively in series.

The load voltage will therefore be less than the source voltage by the voltage lost across the two forward-biased diodes. The maximum inverse voltage applied to the

reverse biased diodes is the peak applied voltage [9]. This will reduce the efficiency particularly at low voltage purposes. The tapped transformer rectifier has only one diode carrying current during either half cycle, but the maximum reverse voltage across the reverse biased diode (the diode not carrying current), will be a value of twice the peak load voltage [5]. The single phase full-wave rectifier with a sinusoidal voltage source will produce a load voltage like a train of positive sinusoidal half cycles waveform while what's required is a level voltage. To achieve this, the ripple energy must be stored in a filter between the rectifier and the load. This can be implemented by using an energy storage device which is often a capacitor. The circuit diagram of single phase full-wave bridge rectifier with a capacitor at the load side is shown in figure 1.5. The capacitor stores energy while the rectifier voltage is near its peak and then supplies the load current for the rest of the cycle. For this reason it is usually called a $reservoir - capacitor$.

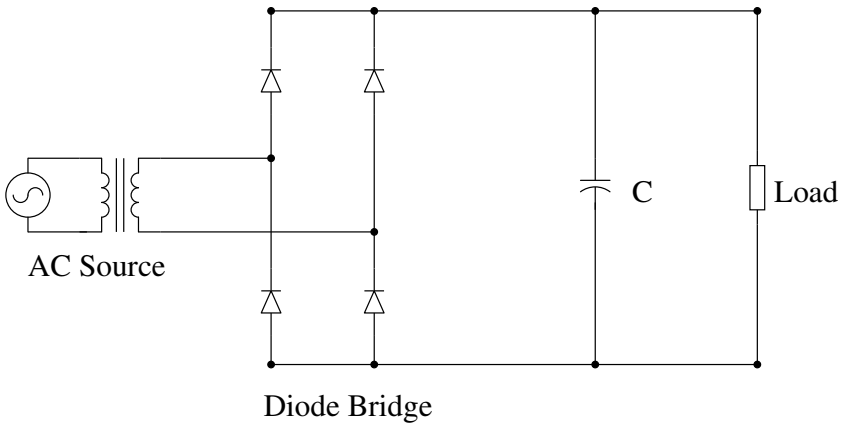


Figure 1.5: A Single Phase Full-Wave Bridge Rectifier with Capacitor Filter

The simplicity in construction, low cost, and the reliability of this rectifier makes it widespread and widely used in domestic and industrial applications.

The main drawback of this design is the pulsating line current, which has a small duration, with a surge value. This current results in a large harmonics injected to the utility AC networks. The high content of harmonics in the line current of the rectifier is responsible for exposing the utility AC networks to a poor power factor and significant increase in losses and thus reduces the power networks efficiency.

To clarify, the work of full-wave rectifier with capacitor filter, consider the following full-wave rectifier with an AC supply voltage of $220V$ and transformer winding ratio of

18 : 1. The load voltage waveform for this rectifier without capacitor is shown in figures 1.6, while load voltage waveform with a capacitor is shown in figure1.7.

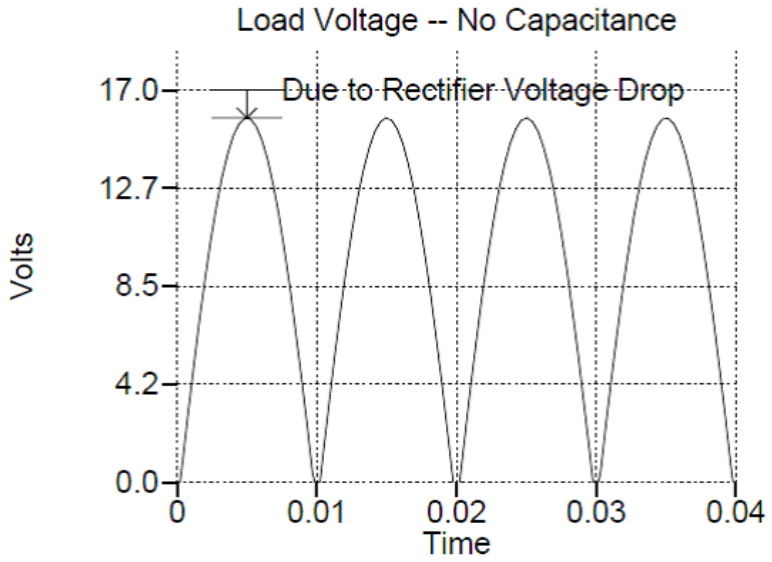


Figure 1.6: Load Voltage without DC Side Capacitor

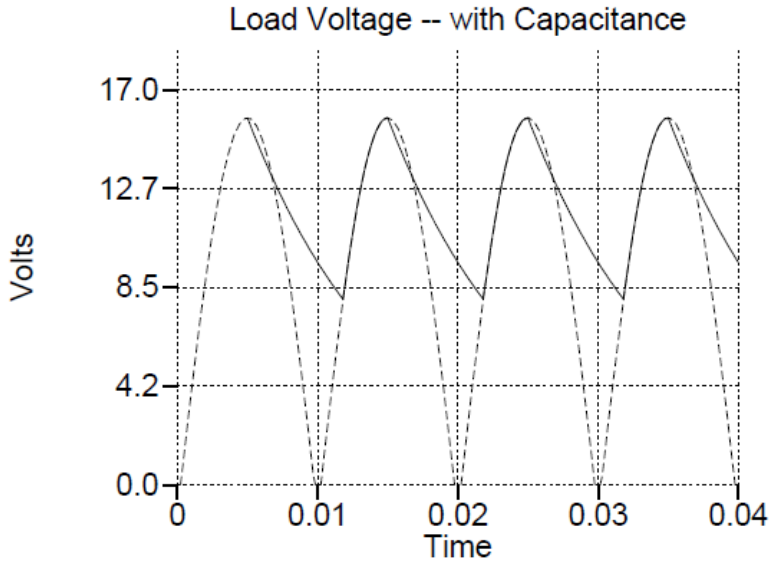


Figure 1.7: Load Voltage with DC Side Capacitor

In order to calculate where the exponential waveform ($Me^{-\frac{x}{\tau}}$) intersects the sinusoidal waveform with amplitude of M, the following equation needs to be solved. Where $\tau = C \cdot R$ is the time constant of the CR network.

$$Me^{-\frac{x}{\tau}} = -Mcos(2\pi fx) \tag{1.13}$$

Or

$$e^{-\frac{x}{\tau}} + cos(2\pi f x) = 0 \tag{1.14}$$

This equation can be sketched with an amplitude of M as shown in figure 1.8

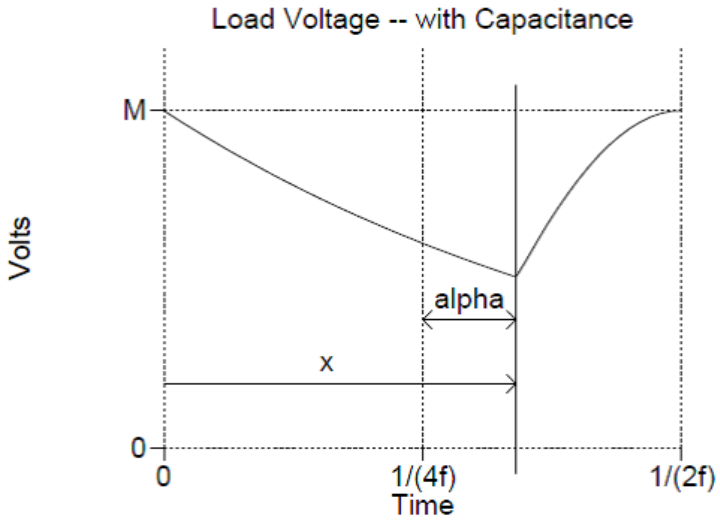


Figure 1.8: Sketch of Equation (1.14)

Where, α is normally specified as the conduction angle. In this figure, α can be obtained from the location of intersect of two curves and then can be derived from x. However the solution of x results in the value of α being in a time quantity (α_{time}), this can be converted eventually to an angle using the following relationships.

$$\alpha_{time} = x - \frac{1}{4f} \tag{1.15}$$

$$\alpha = \alpha_{time} 2\pi f \tag{1.16}$$

An analytical solution for equation (1.14) is done as a part of teaching [6] in Plymouth university is shown in figure 1.9.

Thus for a given C, R and f, the conduction angle α can be derived. This conduction angle determines the average DC voltage across the load; the ripple and the input current.

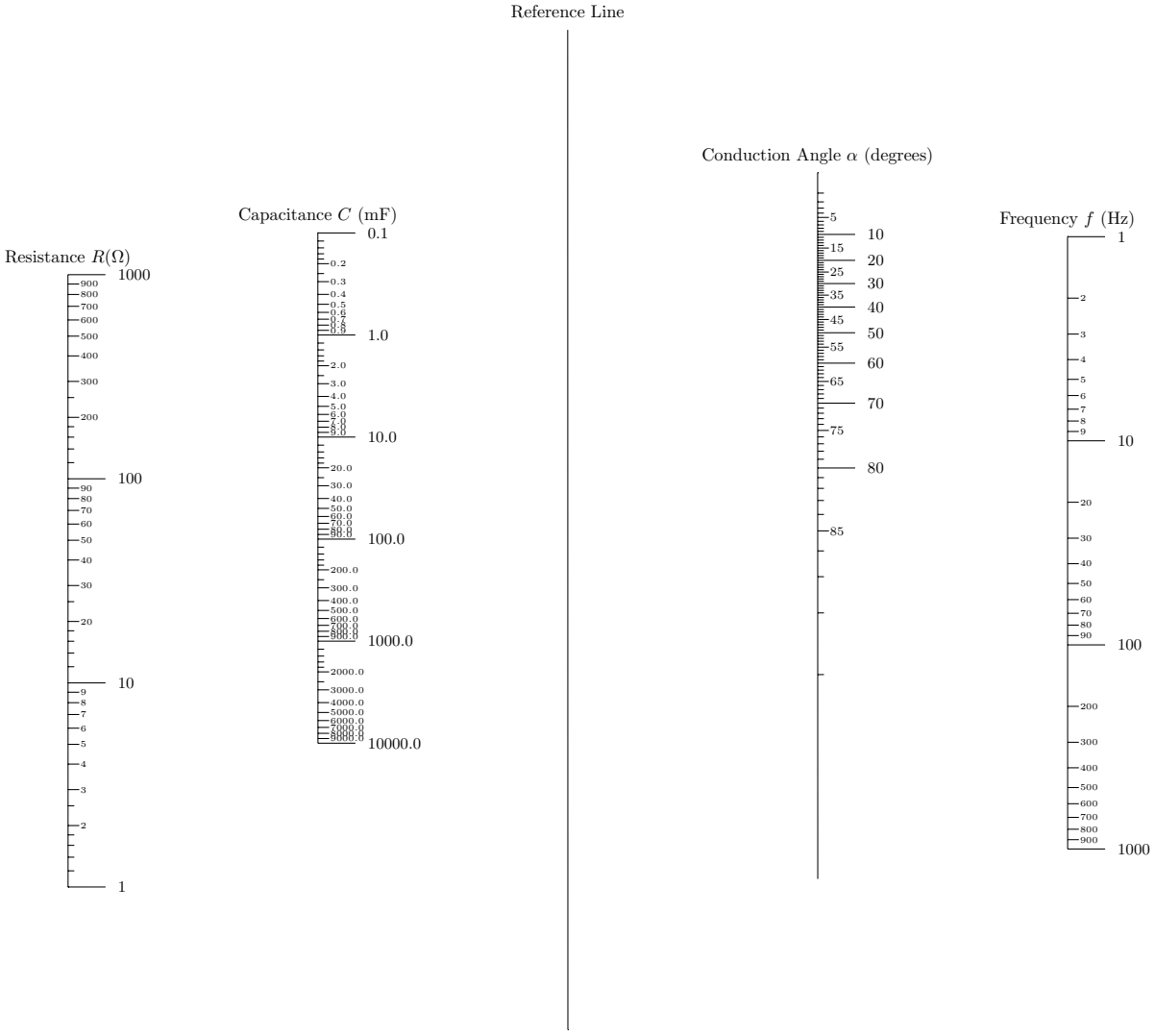


Figure 1.9: Nomogram for Solving Equation (1.14)

The average value of the load voltage can be obtained from figure 1.8 and applying the definition of average which is given in equation (1.1). The exact solution can be obtained as follows

$$V_{average} = \frac{1}{Period}\int_0^{Period} v(t)\ dt \tag{1.17}$$

$$= \frac{1}{\frac{1}{2f}}\left[\int_0^{\frac{\alpha}{4\pi f}+\frac{1}{4f}} Me^{-\frac{t}{\tau}}\ dt - \int_{\frac{\alpha}{4\pi f}}^{\frac{1}{2f}} Mcos(2\pi ft)\ dt\right] \tag{1.18}$$

$$= 2fM\left[-\tau\left[e^{-\frac{t}{\tau}}\right]_0^{\frac{\alpha}{4\pi f}+\frac{1}{4f}} - \frac{1}{2\pi f}\left[sin(2\pi ft)\right]_{\frac{\alpha}{4\pi f}+\frac{1}{4f}}^{\frac{1}{2f}}\right] \tag{1.19}$$

$$V_{average} = M\left[2f\tau(1-e^{-(\frac{\alpha}{4\pi f}+\frac{1}{4f})/\tau}) + \frac{cos(\alpha)}{\pi}\right] \tag{1.20}$$

For most practical systems a straight line approximation is used to calculate the value of the average voltage. Figure 1.10 shows the sketch of equation (1.14) with straight line approximation.

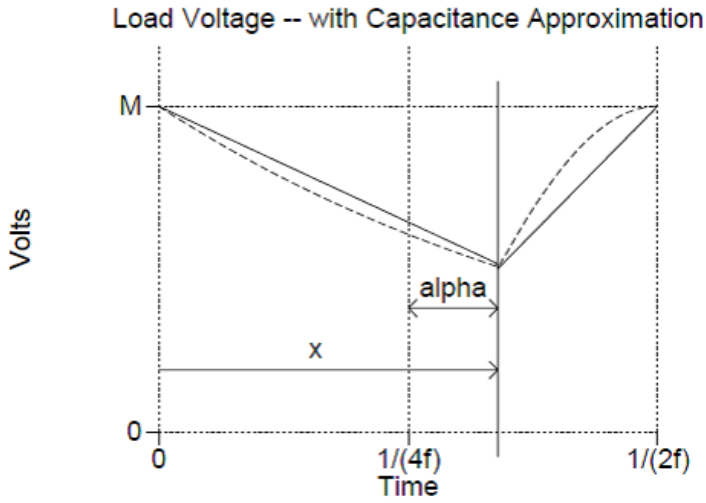


Figure 1.10: Sketch of Equation (1.14) with Straight Line Approximation

This results in

$$V_{average} = \frac{1}{2}(M + Me^{-x/\tau}) \quad (1.21)$$
$$= \frac{M}{2}(1 + e^{-x/\tau}) \quad (1.22)$$
$$x = \frac{\alpha}{2\pi f} + \frac{1}{4f} \quad (1.23)$$

Or

$$V_{average} = \frac{1}{2}(M - Mcos(2\pi f x)) \quad (1.24)$$
$$= \frac{M}{2}(1 + sin(\alpha)) \quad (1.25)$$

For the above example, let $\tau = 0.01s$, $f = 50Hz$, $M = 15.8V$. For a given values of M, C, R and f, the value of α can be determined and it was 30° in this case. Using the exact expression of $V_{average}$ in (1.20), the value of the average voltage is found $12.01V$, while with the approximation expression (1.25) is found $V_{average} = 11.85V$.

AC Side Current Analysis

Once the diodes of the bridge rectifier start conducting, the mains current starts flowing in the circuit and the transformer output connected to the load via the DC side of the rectifier. For the case of pure resistive load connected to the bridge rectifier with a reservoir capacitor, this load actually consists of a resistor (load) in parallel with a capacitor (reservoir capacitor). Thus the current drawn from the transformer is given by (1.26).

$$i_{load} = \frac{Mcos(2\pi f t)}{Z_{load}} \quad (1.26)$$

$$Z_{load} = \frac{R\frac{1}{j2\pi fC}}{R + \frac{1}{j2\pi fC}} = \frac{R}{1 + j2\pi fCR} \tag{1.27}$$

The load current results in a complex quantity, this current waveform is normally approximated as a square waveform with an amplitude equal to the average of the wave described by equation (1.26).

The capacitor of capacitance C charging from $V_{min} = MSin(\alpha)$ to $V_{max} = M$, results in a charge of $C \cdot (V_{max} - V_{min})$. The charge accumulated by the capacitor divided by the time it takes for the capacitor voltage to rise, gives the capacitor charge current. From figure 1.10, the time taken by the capacitor to charge t_c is given by (1.28).

$$t_c = \frac{1}{4f} - \frac{\alpha}{2\pi f} \tag{1.28}$$

Where, α is in radians. If α is in degree, then replace 2π with 360.

Thus the capacitor charging current is approximately given by (1.29).

$$I_{charge} = \frac{C(V_{max} - V_{min})}{t_c} \tag{1.29}$$

The amplitude of the square current waveform is the sum of the capacitor charging current and the average load current.

Thus the amplitude of the square current waveform taken from the transformer (I_s) is given by the below expression.

$$I_s = \frac{C(V_{max} - V_{min})}{t_c} + \frac{V_{average}}{R} \tag{1.30}$$

$$I_{mains} = \frac{I_s}{N} \tag{1.31}$$

This equation is based on the straight line approximation of the charging phase. The current taken from the mains I_{mains} is a square waveform with peak amplitude smaller than the transformer current I_s by a factor equal to the transformer turns ratio N.

The generic waveforms of the supply voltage and the line current of the single phase rectifier system with a capacitor filter on the DC side are shown in figure 1.11.

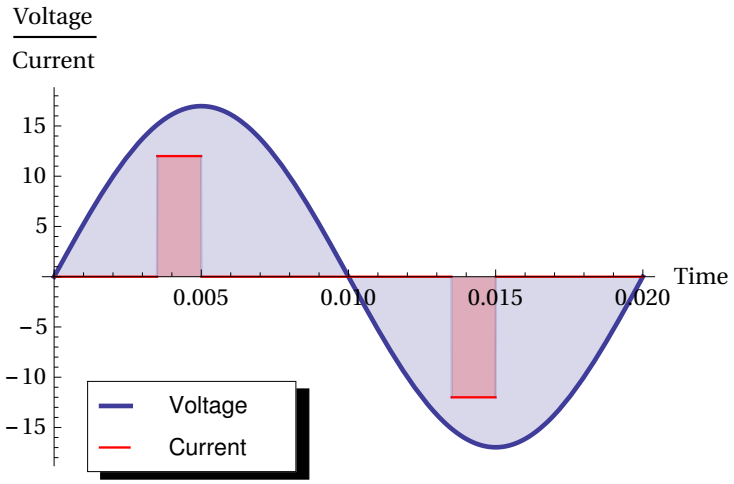


Figure 1.11: Generic Supply Voltage and the Line Current Waveforms of the Single Phase Bridge Rectifier with Capacitor Filter

This current and through its surge value can result in a large amount of harmonics on the AC side of the rectifier and thus reducing the power networks capability to manage loads. It is likely, particularly for medium and high power applications, the summation of these surge currents (non-linear loads) for a specific load zone causes a system failure and service interruption due to the actions of protection circuits. This current also can lead to the unbalancing situation in three-phase systems, which is considered to be one of the most serious cases facing the power networks.

Harmonics are considered the source of many problems facing the safe and stable operation of the AC networks. They are responsible for a significant increase of losses in the transmission and distribution power networks due to the harmonic currents. Harmonic currents in this design can reach a considerable values from the fundamental component of the rectifier current (specifically for the low order harmonic components) and thus exposing the utility AC networks to low input power factor due to the large harmonic distortion.

Harmonics produce an EMI which is detrimental for the communications systems and radio signal control networks.

Harmonics play a key role in determining the validity of any system in terms of the harmonics content, and how much matching the harmonics content of any system to the standard harmonics restrictions at a certain power level. they are also specified in immunity standards and their reduction is a key to reduce noise in the power networks.

1.3 Introduction to Power Supplies

The simple rectifier circuits presented in section 1.2 are examples for unregulated power supplies. The load voltage will change in accordance to the changes in supply voltage or the load current. In order to stabilise the load voltage, another set of arrangement has to be added between the rectification stage and the load. The function of the new configuration is to keep the load voltage constant at a desired level with a small margin of voltage ripple across the load. Normally this task can be done either with a linear regulator or with a DC-DC converter depending on the kind of the application. In case of the linear regulator has been used then the power supply known as a linear power supply. When a DC-DC converter is used to regulate the voltage then the power supply known as switching power supply (or commonly known as switched-mode power supply). In both cases the function of the power supply is to convert an AC power to a DC power at a desired output level.

1.3.1 Linear Power Supplies

Linear power supplies consist of a rectifier and linear regulator. Linear regulator is an electronic regulator in which the voltage or current is controlled using transistors and other active devices as variable impedance elements. Usually regulators are designed to provide a constant load voltage as this is required for most electronic equipment. Regulators may also be used to stabilize the current where this is required by the load [5].

Regulators can be divided into two groups, shunt and series. The shunt regulator has a variable impedance element in parallel with the load. The circuit diagram of the shunt regulator is shown in 1.12. The element diverts current from the load and the load

voltage then can be controlled by varying the amount of the diverted current. The series regulator has a variable impedance element connected in series between the supply and the load. The circuit diagram of the series regulator is shown in 1.13. The voltage across the load is sensed and the impedance of the series element varied in accordance to keep the load voltage constant.

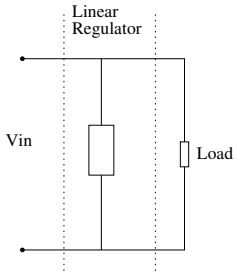


Figure 1.12: Shunt Regulator

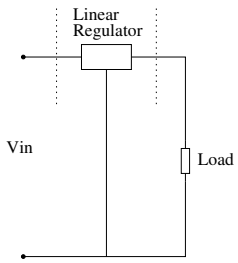


Figure 1.13: Series Regulator

This kind of power supplies provide only a step-down DC voltage from the average input voltage. There is always a voltage drop across the linear regulator and a power loss associated with this voltage drop. The loss of energy in the regulator becomes very significant when a lot of current is drawn from the power supply and thus the switching power supply becomes the better choice [6].

Linear supplies have the following advantages over switching power supplies [10].

- Linear supplies provide a smoother output and they are cheap for low power applications.
- Simpler in design and circuit complexity is low.
- Linear supplies are produce less electrical and electromagnetic interferences, as there is no high frequency switching noise or EMI.

However, except where power is low and efficiency is not important, or where low rate of noise and high stability are required, there is limited use of these kind of power supplies.

1.3.2 Switching Mode Power Supplies

Switching power supplies consist of a rectifier and a DC-DC converter. The input into the DC-DC converter is an unregulated DC power which is the output of the rectifier circuit. The function of the converter is to convert the unregulated DC input into a regulated DC output at a desired output level [3].

DC-DC converters utilize one or more switches to transform DC voltage from one level to another and they are more efficient compared to the linear regulators. They are observing the voltage at the load side and switch in the rectifier if the voltage drops below a lower threshold and switch out the rectifier when the voltage exceeds an upper threshold [6]. They can provide outputs which they are equal to; lower than; higher than or with reversed polarity to the inputs [11]. These converters have many circuit configurations and thus it is not possible to consider all of these circuits in this section. There are three basic types of converters, step-down mode (buck); step-up mode (boost) and the step-up-down mode (buck-boost). They differ in the way that the magnetic elements are operated and each of them has its own unique features.

Step-Down or Buck Converter

As the name implies, a step-down converter produces a lower average output voltage than the average input voltage [3]. The circuit configuration of the step-down converter is shown in figure 1.14.

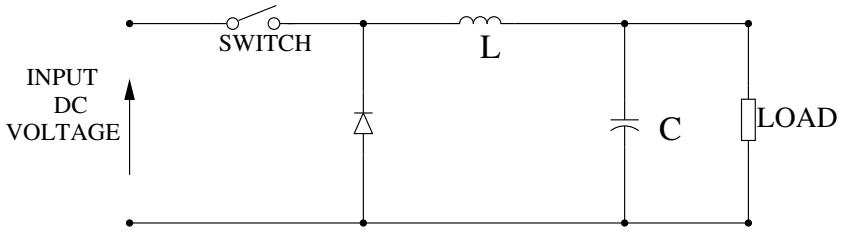


Figure 1.14: Step-Down or Buck Converter

The series switch S is turned on and off within a switching period of T and duty ratio of D. The free-wheeling diode provides an alternative path for the current in the inductor L when the switch is turned off. The capacitor C across the load ensures that the load

voltage is relatively constant [5]. In order to clarify the operation of this converter, the following assumptions have been made

1. The input voltage is always higher the output voltage ($V_{in} > V_{out}$), and V_{in} is the average rectified voltage.
2. The output voltage V_{out} is not isolated from the input voltage V_{in}.
3. The inductor current does not fall to zero (the operation of the converter is in CCM only).
4. The magnetic field in the inductor does not saturate.
5. The capacitor current rises and falls in order to balance the difference between the inductor current and the load current.

The principle of operation of the buck converter can be divided into two states with two periods.

These periods can be defined as t_{on} when the switch is turned on and t_{off} when the switch is off. The sum of these two periods referred to the switching period T. Then the duty cycle (D) of the switch which controls the average output voltage can be defined as

$$T = t_{on} + t_{off} \tag{1.32}$$

$$D = \frac{t_{on}}{T} \tag{1.33}$$

- **On State** ($0 < t \leq t_{on}$)

  This state begins when the switch is turned on at $t = 0$. The input current with ascending tendency flows through the inductor L and supplies the load and the capacitor C. During this period, the energy is stored as an increase in the magnetic field of the inductor L. The capacitor C cannot store the energy as the output voltage is relatively constant.

Since the switch S is turned off for a very short time, then the input voltage can be assumed as a DC voltage of value V_{in}, while the output voltage across the load can be denoted as V_{out}. The voltage and current through the inductor L are related by the following equation

$$V_{inductor} = L\frac{di}{dt} \tag{1.34}$$

This means that,

$$V_{in} - V_{out} = L\frac{di}{dt} \tag{1.35}$$

The inductor current changes from i_{min} to i_{max} in the time period from $t = 0$ to $t = t_{on}$ and then the differential equation of (1.35) can be replaced with an approximation as follows:

$$V_{in} - V_{out} = L\frac{(i_{max} - i_{min})}{t_{on}} \tag{1.36}$$

This results in

$$(i_{max} - i_{min}) = \frac{(V_{in} - V_{out})}{L}\ t_{on} \tag{1.37}$$

- **Off State** $(t_{on} < t \leq (T - t_{on}))$

  When the switch is turned off, the voltage at the input of the inductor L tries to fall below zero (very large reverse voltage is induced in order to keep the current flow) and as a consequences of that, the diode is turned on and the input voltage of the inductor is connected to ground assuming the voltage drop across the forward biased diode is zero. This leads to the output voltage of the inductor L is V_{out} and the inductor current decreases from its value of i_{max} to i_{min} at the end of t_{off}.

$$-V_{out} = L\,\frac{(i_{min} - i_{max})}{t_{off}} \tag{1.38}$$

$$(i_{max} - i_{min}) \;=\; \frac{V_{out}}{L}\,t_{off} \tag{1.39}$$

For CCM of operation and at steady state conditions, the rise in inductor current during the on state should equal to the fall in current during the off state. From (1.37) and (1.39) can get

$$\frac{(V_{in} - V_{out})}{L}\,t_{on} \;=\; \frac{V_{out}}{L}\,t_{off} \tag{1.40}$$

This results in

$$V_{out} \;=\; \frac{t_{on}}{(t_{on} + t_{off})}\,V_{in} \;=\; D\,V_{in} \tag{1.41}$$

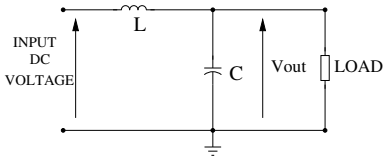


Figure 1.15: On State Circuit Diagram

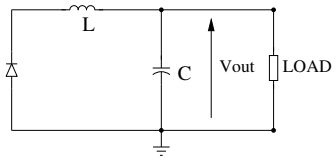


Figure 1.16: Off State Circuit Diagram

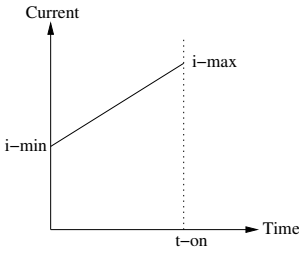


Figure 1.17: Inductor Current at On State

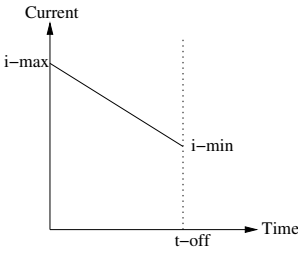


Figure 1.18: Inductor Current at Off State

The ripple voltage can be determined by assuming the load current is constant and the variation in the inductor current is balanced by the capacitor. The ripple voltage can be obtained using the relationship between the voltage across the capacitor V_{PP}

and the capacitor current i_c. Where, V_{pp} is the peak to peak ripple voltage across the capacitor [6].

$$i_c = C \frac{dV_{pp}}{dt} \tag{1.42}$$

$$V_{pp} = \frac{1}{C} \int i_c \, dt \tag{1.43}$$

The peak of the capacitor current i_{cmax} is the average of the of the inductor current.

$$i_{cmax} = \frac{(i_{max} - i_{min})}{2} \tag{1.44}$$

By the substitution in equations (1.32), (1.33) and (1.39), results

$$i_{cmax} = \frac{1}{2} \frac{V_{out}}{L} (1 - D) \, T \tag{1.45}$$

The approximate capacitor ripple voltage and current with the inductor current are all shown in figure 1.19.

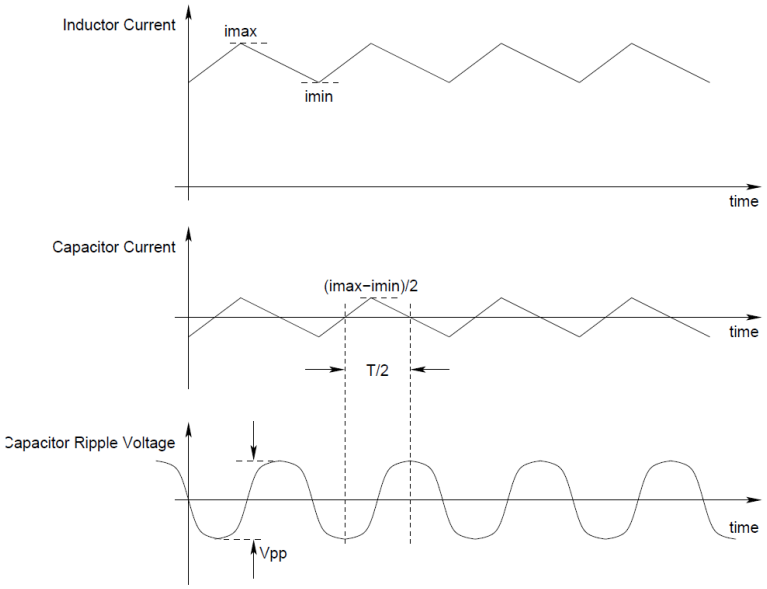


Figure 1.19: An Approximate Capacitor Ripple Voltage and Current with the Inductor Current

The integral of the current waveform (the area under the curve) is the area of a triangle with base of $T/2$ and height of i_{cmax}.

$$V_{pp} = \frac{1}{C} \cdot \frac{1}{2} \cdot \frac{T}{2} \cdot i_{cmax} \quad (1.46)$$

$$= \frac{1}{4C} \cdot \frac{V_{out}}{2L} \cdot (1-D)\ T^2 \quad (1.47)$$

$$= \frac{1}{8} \cdot \frac{1}{LC} \cdot V_{out}\ (1-D)\ T^2 \quad (1.48)$$

$$= V_{out} \cdot \frac{(1-D)}{8LC}\ T^2 \quad (1.49)$$

Using the following definitions

$$f_s = \frac{1}{T} \quad (1.50)$$

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (1.51)$$

Where, f_s is the switching frequency, f_c is the cut-off frequency of the chosen values of L and C.

$$V_{pp} = V_{out}\ (1-D)\ \frac{\pi^2}{2}\ \left(\frac{f_c}{f_s}\right)^2 \quad (1.52)$$

From (1.52), it is clear that the load voltage ripple is independent of the load current and it is determined by the output voltage; duty cycle; switching frequency and the chosen values of L and C.

Boost Mode or Step-Up Converter

It is clear from the name of this converter, the output voltage is always higher than the average input voltage [1].

The circuit configuration of the step-up converter is shown in figure 1.20.

The operation of this converter can be also divided into two states (on and off state). When the switch is closed (on state), the diode is being reversed biased and the load is supplied completely from the capacitor. The current in the inductor increases and thus the stored energy in the inductor is increased. When the switch is opened (off state), the load receives the energy from the inductor and as well as from the supply [12].

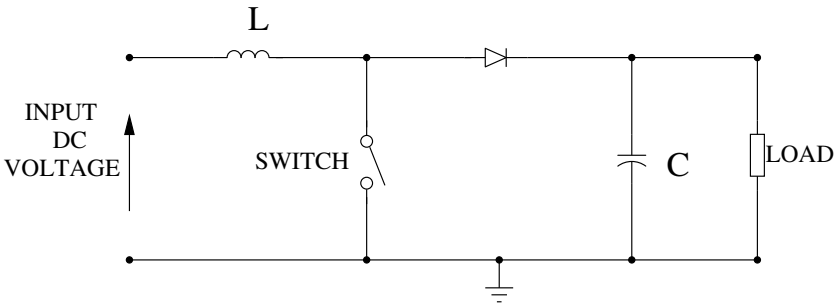


Figure 1.20: Step-Up or Boost Converter

Using similar way of analysis as in the buck converter, the output voltage can be obtained as follows

$$V_{out} = \frac{1}{(1-D)} V_{in} \tag{1.53}$$

Where, D is the duty cycle of the switch.

The output voltage ripple can be determined by computing the voltage drop of the CR network when the switch is on. This is identical to the set-up described in section 1.2. The following assumption can be made [6].

$$V_{out} \approx V_{max}\ e^{-\frac{\frac{t_{on}}{2}}{CR}} \tag{1.54}$$

$$V_{min} = V_{max}\ e^{-\frac{t_{on}}{CR}} \tag{1.55}$$

$$V_{pp} = V_{max} - V_{min} \tag{1.56}$$

$$V_{pp} = V_{out}\ \frac{(1 - e^{-\frac{t_{on}}{CR}})}{e^{-\frac{t_{on}}{2CR}}} \tag{1.57}$$

Under the assumption $t_{on} << CR$, and using the mathematical series expansion of the exponential function, the final expression of the peak to peak ripple voltage V_{pp} can be found as

$$V_{pp} \approx V_{out} \frac{t_{on}}{CR} \tag{1.58}$$

Buck-Boost or Step-Up-Down Converter

The third type of the basic converter circuits is the buck-boost circuit. The main application of this kind of converter is where a negative polarity output may be desired with respect to the common terminal of the input voltage. The output voltage can be either higher or lower than the input voltage [3]. The circuit configuration is show in figure 1.21.

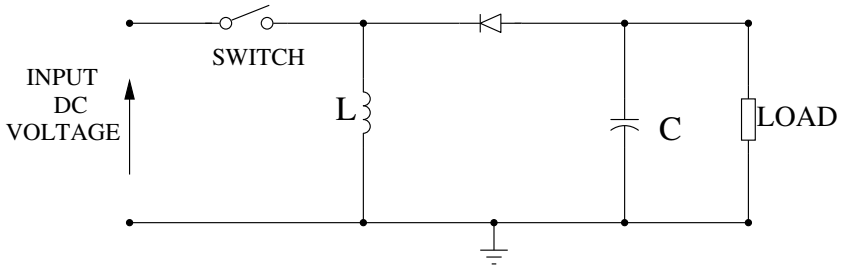


Figure 1.21: Step-Up-Down Converter

In this converter, while the switch is turned on, the inductor current increases and the energy is being stored in the inductor until the switch is turned off. When the switch is turned off, the voltage across the inductor is reversed and the current in the inductor continues to flow. As a results of that the diode being forward biased and the the inductor current is transferred to the load [5]. Using similar way of analysis as in the buck and boost converters, the output voltage can be obtained as follows

$$V_{out} = \frac{D}{(1-D)} V_{in} \tag{1.59}$$

Where, D is the duty cycle of the switch.

Weinberg Boost Converter

Weinberg topology was invented in 1974. This boost converter is configured as a high power and high efficiency for space applications [13]. It was designed essentially for satellite power systems when battery power storage is required to supply a regulated mains voltage. The circuit configuration of Weinberg converter is shown in figure 1.22.

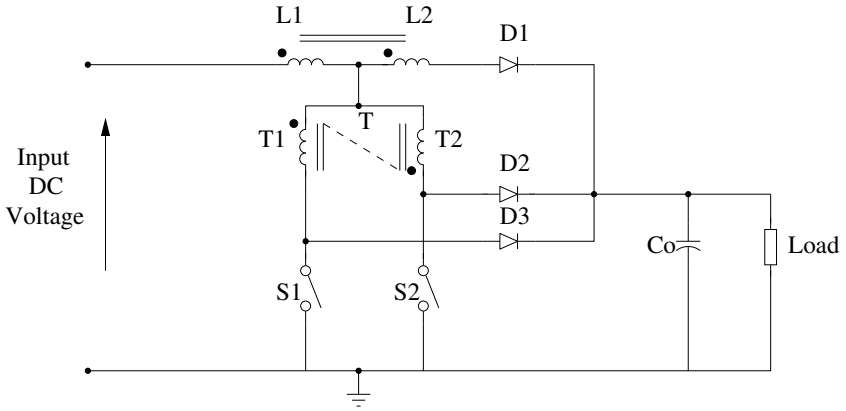


Figure 1.22: Weinberg Converter

Weinberg converter utilises the close-coupled inductors topology with a main inductor which is divided into two identical parts before and after the common point of the closed coupled inductors. This converter is designed to ensure a continuous output current by providing an alternative (parallel) path for energy to flow into the load side. The principle of operation of this converter has two states:

- S_1 or S_2 switched On, forcing D_2 or D_3 respectively to be also On, while D_1 is Off.
- S_1 and S_2 switched both Off, and D_1 is On.

By control the operation of switches S_1 and S_2, the output voltage of the converter can be controlled. The output voltage of Weinberg converter can be expressed as in (1.60).

$$V_{out} = (1 + D)\ V_{in} \tag{1.60}$$

Where, D is the duty cycle of switches S_1 and S_2.

It is clear that the output voltage can reach any possible value between the input voltage and twice the input voltage. This converter showed a reasonable performance with respect to efficiency; reduced mass and power handling capability. A superior power density with a high efficiency of more than 97% on the 100 kW class close-coupled converter is demonstrated in [14].

1.4 Thesis Aims and Organisation

This thesis investigates the A.C to D.C power conversion in single phase systems. The research consists mainly of two phases. The first phase is focused on the investigations to find a new approach of rectification in single phase systems. A novel single phase rectification technique with a new architecture and control strategy is proposed. The new technique aims to increase the low input power factor in the conventional single phase rectifier system (typically between 0.3-0.6) and thus higher efficiency can be achieved. The new rectifier architecture also aims to provide a reduction in the size of the DC side capacitor which results in lower content of harmonic in the rectifier line current. The presence of the large smoothing capacitor in the conventional rectifier system results in the generation of a considerable line current harmonics to be injected into the utility AC supply networks.

The second phase of this research is focused on the DC-DC conversion. A novel buck-boost DC-DC converter architecture using close-coupled inductors with its transfer function is proposed. The new topology aims to reduce the switching noise and thus the switching losses that usually accompanies the conventional buck and boost converter circuits. The reduction in the system losses leads to higher power conversion efficiency for this kind of converters dealing with a wide range of supply voltages and serves a wide variety of applications.

This thesis is organised into five chapters as follows: Chapter 2, is the literature review of research in AC-DC power conversion for single phase systems. This literature review has been classified into two parts. The first part is interested in research which is

concerned with the new rectification techniques and methods to improve the performance of the conventional single phase rectifier system. The second part of the literature review is focused on research which is concerned with the new DC-DC conversion architectures.

Chapter 3, presented a novel single phase rectification technique with a new architecture and control strategy. The circuit configuration of the new rectifier and the principles of operation are presented. The AC side analysis of the rectifier line current is done using Woodward's notations applied to chopped waveforms. The prototype circuits of the proposed and the conventional single phase rectifiers have been designed, fabricated and tested. A comparison between the performances of the two rectifiers by conducting two case studies has been done. The performance analysis of the proposed rectification technique is demonstrated with a wide range of case studies and different sets of design parameters have been undertaken.

In chapter 4, a novel buck-boost DC-DC converter architecture with its transfer function is presented. The circuit configuration of the proposed converter and the principles of operation are presented. This converter utilises the close inversely-coupled inductors topology in both its conversion stages (buck and boost). The transfer function of the buck-boost converter in CCM of operation and steady state conditions is given. The prototype circuit of the proposed converter has been fabricated and tested. The practical results of a range of case studies are included in this work. A simulation model for the converter circuit is also done using LT spice IV4.22. The simulation model has been examined with the same case studies that been conducted in the practical part.

In Chapter 5, the work presented in this thesis is concluded and some suggestions for future work in this area are given.

1.5 Contribution to Knowledge

The following list summarises the main contributions of the dissertation.

- **A novel single phase rectification technique with a new architecture and control scheme.**

  The new rectifier allows to obtain high input power factor and thus higher efficiency to be achieved. The current harmonics generation in the proposed technique can be suppressed which results in lower content of harmonic in the line current of the rectifier. Woodward's notation is used in the AC side analysis of the proposed and the conventional rectifiers, which is considered a new method of signal analysing in this field. The rectifier architecture provides a reduction in the size of the DC side capacitor. This reduction can be as low as less than 10% of the size of the typical smoothing capacitor in the conventional single phase rectifier. The size of smoothing capacitor restricts the power density of the conventional system. The new rectifier now allows the possibility to increase the power rating of such rectifiers to a higher values. **This contribution is presented by the author and published in:**

  - **S. Al-Zubaidi; M.Z.Ahmed; P.Davey , "Design of Single Bidirectional Switch Single Phase Rectifier with Reduced Size DC Side Capacitor," IEEE Conference, The First International Future Energy Electronics Conference (IFEEC), Tainan, Taiwan, Nov. 2013.**
  - **S. Al-Zubaidi; M.Z.Ahmed; P.Davey , "High Power Factor Single Phase Rectification Technique with Reduced Line Current Harmonics," IEEE Workshop, The Fifteenth IEEE Workshop on Control and Modelling for Power Electronics (COMPEL), Santander, Spain, June 2014.**

  This contribution also has been published in:

WIPO - World Intellectual Property Organization, Publication No.: WO/2015/008039, Publication Date: 22.01.2015.

- **A novel buck-boost DC-DC converter architecture using close-coupled inductors with its transfer function.**

  Converters utilise the coupled inductor topology can achieve a higher power densities with better performance. The new converter architecture strongly reduces the switching noise and thus reduces the switching losses that usually accompanies the conventional converter circuits. Switching noise is considered as a major drawback in the typical buck and boost converter circuits which causes a significant switching losses and results in high voltage stress on the power switches.

  The new architecture ensures the maintaining of continuous flow of current in both converter stages (buck and boost), which results in large reduction in the back e.m.f induced in the main inductor and thus reduces the switching noise. As a consequences of that higher power conversion efficiency with less switching noise can be achieved with the proposed converter.

  The new converter architecture also provides a unique design of the passive clamped circuit. The function of the proposed clamped circuit is to recycle the leakage energies of the coupled inductors which results in an efficiency improvement of the power conversion process. Also, this circuit is used to clamp the large voltage spikes (due to the impedance buffer provided by the coupled inductors) in order to limit the voltage stress on the power switches.

  This contribution is presented by the author and published in:

  - **S. Al-Zubaidi; M.Z.Ahmed; P.Davey , "A Novel Buck-Boost DC-DC Converter Using Close-Coupled Inductors," IEEE Symposium, The Sixth International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Aachen, Germany, June 2015.**

Chapter 2

Literature Review

2.1 Single Phase Rectifier

The enormous increase in non-linear loads connected to the utility AC supply represent a serious challenge because of the pulsating current. This current has a small duration with a surge value can result in large harmonics injected to the utility AC supply. The high content of harmonic currents in the AC side of these non-linear loads is responsible for exposing the utility AC networks to poor power factor and a significant increase in losses and thus reduces the power networks efficiency. The harmonic currents produced by non-linear loads tends to produce a voltage harmonics to the mains. These voltage harmonics or voltage distortion in the mains, have an effect on the harmonic characteristics of the input current of these non-linear loads. The harmonic characteristics of the input current are dependent not only on the magnitude of the supply voltage harmonics but also on their phase angles [15].

The reason behind this current harmonic phenomenon is the large smoothing capacitor (reservoir capacitor) required to reduce the ripple power in the DC side of the rectifier. The size of this capacitor restricts the capability of increasing the power density of such loads.

From the above it seems that there is a need for a new rectification technique for single phase system. This technique should meet the following fundamental requirements:

1. High input power factor with low harmonic content in the line current of the rectifier.

2. Simplicity and reliability with low component count.

3. The capability of increasing power density and simple control scheme.

High input power factor with reduced line current harmonics ensures a significant reduction in the total system losses and provides an efficient, safe and reliable operation of the utility AC supply networks.

Simplicity in design and control scheme of any proposed architecture enables increasing the power density and provides a high level of reliability for the system which makes it popular for a wide variety of applications.

One of the widely used non linear load is the single phase bridge rectifier with a DC side capacitor. Figure 2.1 shows the circuit configuration of the conventional single phase rectifier identifying the regions of interest for research.

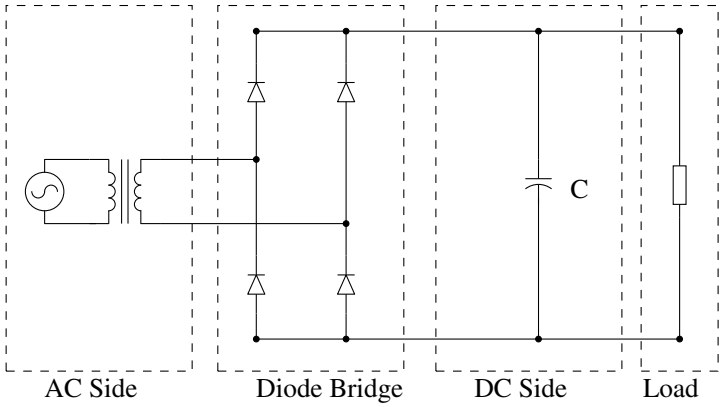


Figure 2.1: Single Phase Bridge Rectifier with Marked Regions of Research Groups

A literature in this field can be classified in general into two main groups:

1. Research focus on the AC side of the rectifier (including the diode bridge).

2. Research focus on the DC side of the rectifier (including the diode bridge).

Research has identified different ideas to improve the power factor; efficiency and reduce the harmonics content of the line current of conventional rectifier. A brief survey of research in this field is presented as follows:

2.1.1 Research in the AC Side of Rectifier

Khan et al. [16] Proposed a single MOSFET switch and series LC filter connected in series to the AC side of the bridge rectifier. The LC circuit used as an alternative path for the input current to keep it in a continuous flow. Although this scheme successfully increased the input power factor and reduced the harmonic distortion, the presence of the MOSFET switch and the large size series passive components in the AC side is considered as the main drawbacks. This is because they produce considerable losses and become very costly if high power, high specifications components have been used in order to reduce losses. All that makes this configuration only suitable for low power applications.

Prasad et al. [17] Proposed a passive circuit (input filter) in series with AC power supply. The inductor and the capacitor of the passive circuit are connected in parallel. The results showed an increase in the input power factor and power density of the rectifier.

The same architecture of [17] is presented in [18], but with additional capacitor placed in parallel between the passive circuit and the bridge rectifier. The results showed that the installation of this capacitor achieved a reduction in the THD of the line current with an improvement in the input power factor.

The size, cost, fixed compensation, resonance and losses considerations of the passive components remains the main drawbacks of both architectures [19].

Conventional single phase rectifier with a shunt active power filter are widely used in PFC and harmonic current compensation applications.

The researchers in [20–22] followed the theme of using shunt PFC boosting techniques to compensate the harmonic current drawn by the conventional rectifier. This is done by injecting equal but opposite currents to shape the pulsating line current to a sinusoidal form and synchronising the resulting current with the supply voltage. Several boost rectifier architectures and control schemes have been proposed and presented. The results showed that corrections in the input power factor (up to unity) have been achieved with a reduction in the harmonic distortion of the line current.

The research [23–32] shared the key point of using shunt active power filter techniques to compensate for harmonic current of the rectifier. The active power filter circuit is based on a single phase inverter circuit with a capacitor in the DC side and a passive circuit in the AC side of the inverter circuit. Various control schemes have been proposed and discussed in this research. The results of the proposed techniques demonstrated the capability to alleviate the harmonic distortion of the line current and correct the input power factor.

Qi et al. [33] proposed a single phase PWM rectifier with an AC side inductor is divided into two halves and placed on both sides of the AC supply. An auxiliary decoupling capacitor is also added to absorb the ripple power. A capacitor in the DC side of the rectifier is placed to support the output voltage and to filter out high frequency switching ripple voltage. The same concept of using two capacitors and two inductors to handle with ripple power and to reduce the ripple of the output voltage can be seen in [34]. Different circuit architectures and control schemes have been applied in both works.

Although the above techniques showed a reasonable performance to compensate for harmonic currents, the need for greater reliability and simpler construction with less complicated control systems is not met by these proposals.

2.1.2 Research in the DC Side of Rectifier

New single phase to three phase converters for motor drive system have been proposed in [35,36]. The presented circuits based on a single phase rectifier with parallel connected active ripple port and ends with three phase converter. The function of the ripple circuit is to decouple the ripple power that comes from the AC side. The ripple circuit is a kind of boost circuit and has a charging and discharging phase in its operation. Two different circuit configurations and control schemes have been used in these works.

Another single phase to three phase converter circuit is presented in [37]. It is utilized a small DC link capacitor. The proposed control method can drive a motor and shape the line current as a sinusoid simultaneously. However, the drive with this method has

high load current with low efficiency. The efficiency can be improved by keeping the DC link voltage constant at a certain level.

A single phase PWM rectifier with an active ripple port is proposed in [38, 39]. The ripple circuit has been added in parallel with the output of the PWM rectifier and works as an auxiliary circuit. Two different circuit configurations of the ripple circuit and control strategies have been used in these works. Both circuits achieved a reduction in the size of the required DC side capacitor with an increase in the power density of the system.

The common key point in the research [35, 36, 38, 39] is the use of an active ripple circuit to filter out the ripple power. The ripple circuit is utilized two or more switches and two or more passive components (inductor and capacitor) as energy storage devices.

Lima et al. [40] presented a new structure of single phase hybrid rectifier. This structure consists of a diode bridge rectifier in parallel with a non-isolated switched converter. The main aim of this configuration is to reduce a portion of the active power processed by the converter and delivered to the load. A PWM control technique is implemented to limit the contribution of the converter and to impose an input current from the bridge rectifier with low harmonic content.

Common PFC approaches are used widely in fluorescent lighting including an active and passive PFC techniques. Active PFC topology such as adding boosting stage after the diode bridge has the advantage of achieving close to unity power factor with smaller size; volume and weight of the circuit elements but with more complexity in circuit and control scheme [41]. Passive PFC circuits such as the Valley fill and the charge pump circuits have the advantages of less complexity in design and control scheme. The Valley fill circuit does not require any control circuit and it is capable to achieve a power factor of 95%. The circuit configuration and the key waveforms of the valley fill circuit is shown in figures 2.2, 2.3 respectively.

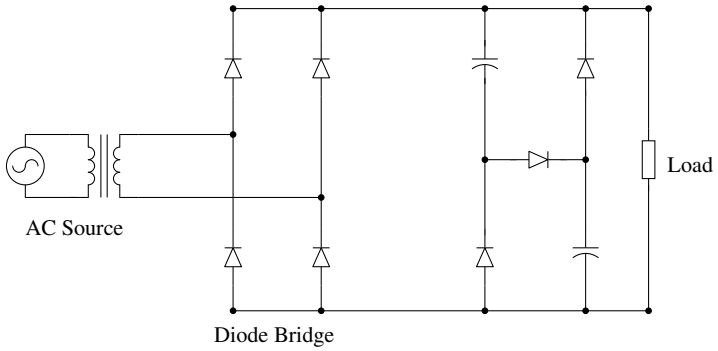


Figure 2.2: Valley Fill Circuit

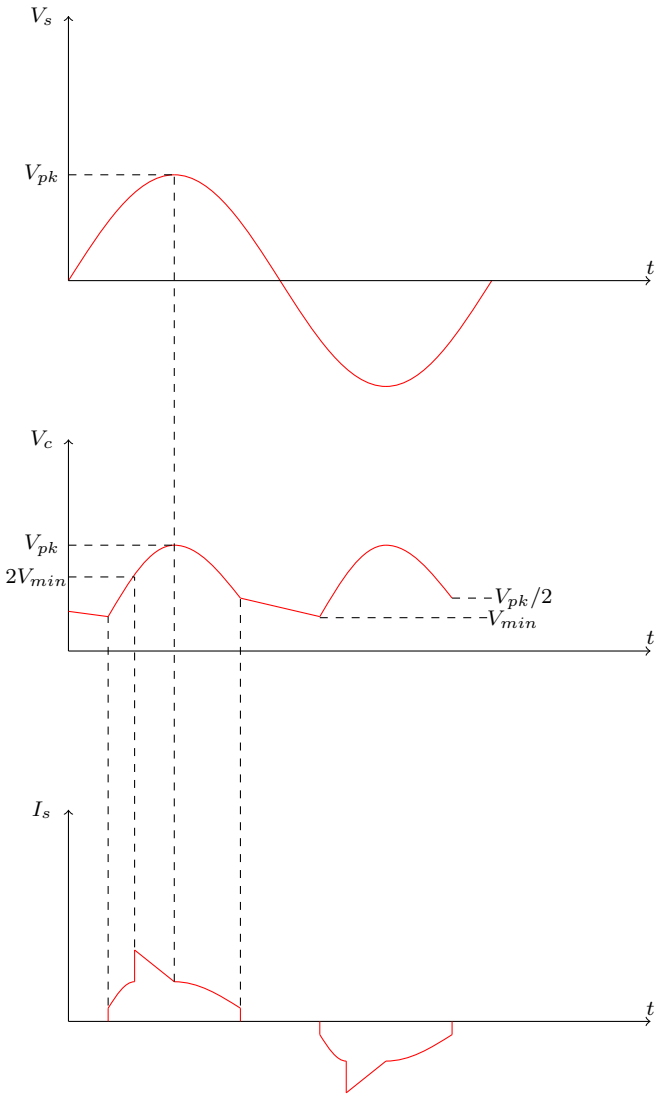


Figure 2.3: Theoretical Waveforms of the Valley Fill Circuit

The operating principles with full details of this kind of passive PFC circuit is presented in the works [42–44].

However, the relatively high THD (normally about 25%); high DC ripple voltage which leads to high crest factor in the lamp current and thus reduces the efficiency are the main drawbacks of this approach [45, 46].

The researchers in [42, 47] suggested a new method to achieve a lower value of the lamp current crest factor by employing pulse frequency modulation technique. This can be done based on the waveform of the DC link voltage which is predetermined by the Valley fill circuit. The waveform is then taken into the control scheme of the circuit. Different switching strategies have been used in both works to implement a changeable switching frequency in order to keep the crest factor in a lower value.

A simple single switch ballast circuit with Valley fill circuit is proposed in [48], this circuit is able to achieve ZCS to maximize the circuit efficiency.

A modified Valley fill circuit is presented in [49, 50]. The proposed circuit is capable to lower the discharge voltage of the circuit capacitor by inserting an additional branch within the original circuit. This results that the voltage across the capacitors is one-third of the peak voltage which allows a further extension to the conduction angle of the line current with lower THD and crest factor can be achieved.

2.2 DC-DC Converters

The use of conventional buck and boost converter circuits is usually accompanied by large switching noise through the switching transient in turn produces a voltage stress on the power switches of these circuits and a considerable switching losses which leads to poor power conversion efficiency. The noise is a result of the back e.m.f induced in the coils of the buck and boost circuits, which is a consequences of the discontinuous current of these coils during the switching transient. This e.m.f is a function of many factors like the coil size, load current and the switching frequency.

The use of coupled inductor is considered a key solution to many needs in the DC-DC converter circuits. The control of the diode current falling rate; the diode reverse-recovery alleviation; the employing of the coupled inductors to operate in the transformer mode to avoid the extreme duty cycle and to reduce the current ripple in high step-up or step-down conversion are some of these utilisations [51].

A coupled inductor topology can be defined as a sort of special purpose transformer. According to the way that coupled inductor is implemented, there are various models of them. The coils may be directly or inversely coupled; loosely or interleaved and may be implemented on two magnetic cores or combined on the same magnetic component. The characteristics and the performance for each of these models are different. To figure out the characteristics analysis and the performance evaluation for these various models of the coupled inductor, valuable studies have been made in [52–55]. This research provides a useful analysis about the subject.

Weinberg boost converter is presented in [13]. This converter can offers a continuous flow of the output current with a small current ripple. As a consequences of that, low switching noise and high conversion efficiency can be obtained. The circuit configuration of this converter was shown earlier in figure 1.22.

Close-coupled inductor topologies can achieve a higher power densities with reduced size, weight and losses in the magnetic components. These features are very desirable in electrical transport applications such as electric vehicles and railway traction [14, 56, 57].

The utilization of the integrating magnetic structure on a single core for the coupled inductors enables further reduction in the overall volume, weight and the copper usage of the magnetic components [58–60].

High voltage gain converters are widely employed in many applications such as photovoltaic systems; fuel cell systems and electric vehicles [61, 62]. High step-up converters can be implemented by combining a charge pump capacitor with the coupled inductors. Since the charge pump capacitor is connected in series with the coupled inductors, the charging current required by the capacitor can be reduced. The voltage gain can be significantly increased and the turn ratio of the coupled inductor can be reduced [62–67].

The voltage gain can be further extended with voltage doubler cells and diode-capacitor techniques combined with the coupled inductor. Different circuit configurations and designs are presented in [61, 68–71].

The voltage stress of power switches and diodes can be reduced by adding passive clamping circuits [72–74]. Passive clamp circuit is a combination of L, C, and diodes in certain arrangement. The passive clamp circuit is important to eliminate undesired resonance between the leakage inductor of coupled inductors and the stray capacitor of the diode, in addition to recover the trapped energy with the leakage inductance of the coupled inductor. The energy stored in the leakage inductance is recycled with the use of passive clamp circuit and transferred to the output side together with the input energy [75]. An active clamp circuit can be used for this purpose with a ZVS to avoid an extra switching loss as in [75–77]. ZVS techniques can be also implemented to drive the power switch of the boost converter which utilises the coupled inductor topology [78].

High step-up converter based on three-winding coupled inductors and voltage doubler circuit is presented in [79]. This converter utilizes a single active switch to reach the desired voltage gain with a continuous flow of the input current. Tseng et al. [80] presented a high step-up converter with three-winding coupled inductors and passive clamping technique to recycle the leakage energy and to alleviate the voltage stress on the power switches.

High step-up converter with active coupled inductor network is presented in [81]. The proposed converter contains two coupled inductors integrated on one magnetic core with two switches have been used in this converter circuit. The primary side of the coupled inductors are charged in parallel by the input voltage and discharged in series with the input voltage to achieve a high voltage gain. Passive lossless clamp circuit is also used to recycle the leakage energies and to reduce the voltage stress on the main switches.

Chapter 3

A Novel High Power Factor Single Phase Rectification Technique with Reduced Size DC Side Capacitor and Suppressed Line Current Harmonics

3.1 Introduction

A novel rectification technique for single phase system is presented in this chapter. The main aims of the proposed technique are to maintain high input power factor and provide a reduction in the size of the DC side capacitor with reduced line current harmonics compared to the conventional single phase rectifier.

In the conventional rectifier system, the main drawback is the pulsating line current which has a small duration with a surge value. This current is the required current to charge the large smoothing capacitor on the DC side of the rectifier and to supply the load during the conduction time of the bridge rectifier. The pulsating current results in large harmonics on the AC side of the rectifier and thus exposing the utility AC networks to low power factor (typically 0.3-0.6) and significant increase of losses due to the harmonic currents. The size of the smoothing capacitor restricts the increase in

power density of the conventional rectifier system. The new rectifier system allows the possibility to increase the power rating of such rectifiers to a higher values.

3.2 The Proposed Technique

3.2.1 Circuit Configuration

The circuit configuration of the proposed single-phase rectifier can be described by simplicity in design and the reliability in construction. The circuit configuration of the new rectifier is shown in figure 3.1. It consists of a branch of one bidirectional switch and capacitor connected in parallel to the diode bridge rectifier.

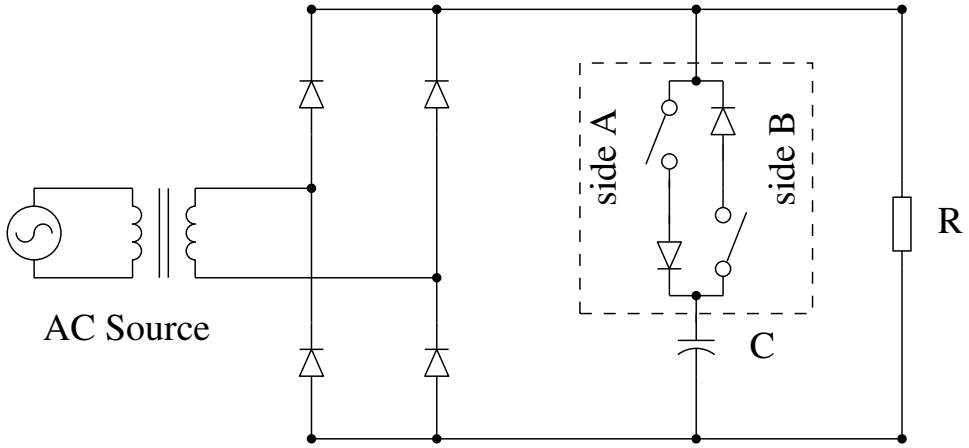


Figure 3.1: Circuit Configuration of the Proposed Single-Phase Rectifier

The circuit structure of the proposed bidirectional switch is shown in figure 3.2. This switch-cell uses two MOSFETs and a diode pair.

The design parameters used to determine and evaluate the system performance of the new rectifier system are illustrated in table 3.1.

Table 3.1: The Design Parameters

Parameter	Definition
V_{pk}	The peak value of A.C. supply voltage
V_{ref}	The selected reference D.C. voltage level
f	The supply voltage frequency
R	The connected load

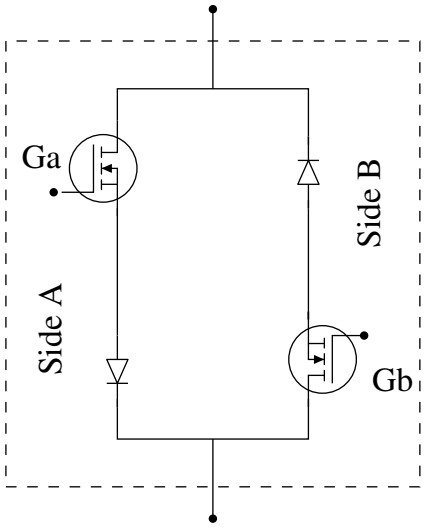


Figure 3.2: Structure of the Proposed Bidirectional Switch

3.2.2 Principles of Operation

The principles of operation of the proposed rectifier can be illustrated as shown in figure 3.3. The proposed control strategy of the new rectifier is based on a smart and uncomplicated idea. The control scheme that governs the action of the bidirectional switch has divided the operation of this rectifier into three operating conditions or three modes.

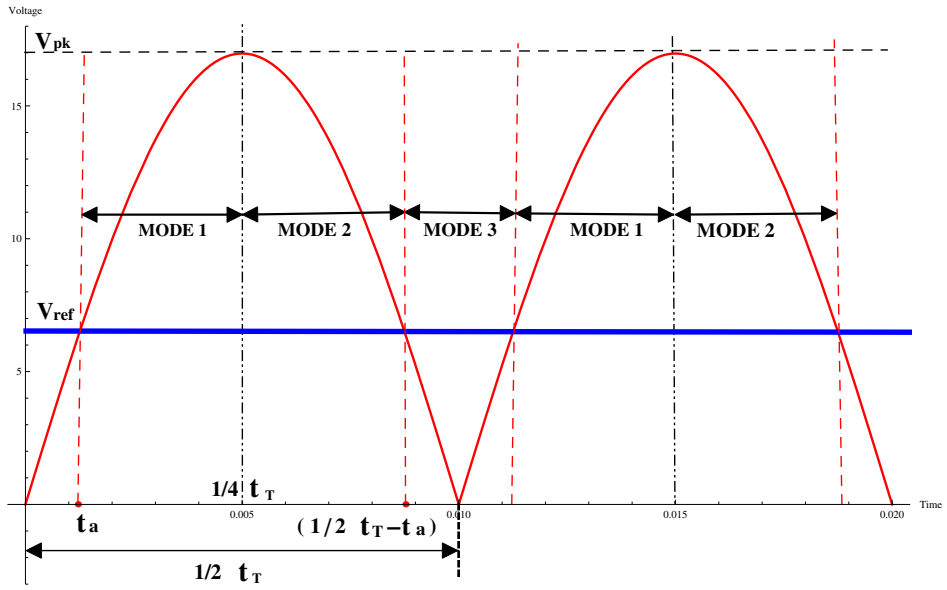


Figure 3.3: Operating Zones of The Proposed Technique

In figure 3.3, t_T is the full cycle time of the supply frequency, t_a is zero line current period in time.

Modes are defined by the supply voltage (the output voltage from the bridge rectifier)

in relation to the reference DC level (V_{ref}) or the threshold level.

MODE 1 : When the instantaneous value of the supply voltage is increasing and it is greater than or equal to the reference DC level (V_{ref}). In this mode,

- The bidirectional switch (side A) is now turned on, and (side B) is off.
- The load and the capacitor are now both connected to the supply voltage.

The equivalent circuit of the DC side of the rectifier in mode 1 is shown in figure 3.4.

Where i_s is the rectifier line current, i_c is the capacitor branch current, i_r is the load current, C is the capacitance of the storage capacitor, R_{oe} is the equivalent series resistance of the capacitor and MOSFETs.

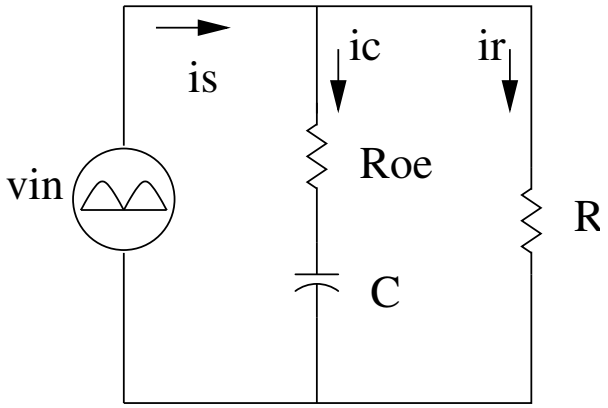


Figure 3.4: Equivalent Circuit of The Rectifier at Mode 1

Using the equivalent circuit of the capacitor in the frequency domain, the rectifier line current in the frequency domain I_s can be derived as follows.

Starting with,

$$I_s = I_c + I_r \tag{3.1}$$

Where, I_c, I_r are the capacitor branch current and load current respectively in the frequency domain.

$$I_c = \frac{V_{in} - \frac{V_o}{s}}{R_{oe} + \frac{1}{s\ C}} \tag{3.2}$$

Where, V_{in} is the input voltage in the frequency domain, V_o is initial value of the capacitor voltage.

$$R_{oe} = R_{DS(ON)} + ESR \tag{3.3}$$

Where,

$R_{DS(ON)}$ is the on state resistance of the used MOSFETs, ESR is the equivalent series resistance of the storage capacitor.

$$V_{in} = V_{pk}\frac{\omega}{s^2 + \omega^2} \tag{3.4}$$

$$V_o = V_{ref} \tag{3.5}$$

$$I_r = \frac{V_{in}}{R} = \frac{V_{pk}}{R} \cdot \frac{\omega}{s^2 + \omega^2} \tag{3.6}$$

By the substitution of (3.2), and (3.6) in (3.1), it can be expressed the rectifier line current I_s of mode 1 in the frequency domain as in (3.7).

$$I_s = \frac{\omega s V_{pk}}{R_{oe}\left(\omega^2 + s^2\right)(a + s)} - \frac{V_{ref}}{R_{oe}(a + s)} + \frac{\omega V_{pk}}{R\left(\omega^2 + s^2\right)} \tag{3.7}$$

Where,

$$a = \frac{1}{R_{oe}\ C} \tag{3.8}$$

This mode continues until the instantaneous value of the supply voltage reaches it's maximum value.

MODE 2 : When the instantaneous value of the supply voltage is decreasing and it is greater than or equal to the reference DC level (V_{ref}). In this mode,

- The bidirectional switch (side A and side B) are both off. The capacitor is disconnected from the supply and it is fully charged.
- The load is still connected to the supply voltage.

The equivalent circuit of this mode is just a resistive load connected to the bridge rectifier. Using similar way which is used to determine the rectifier line current in the frequency domain of mode 1. The line current of the rectifier in frequency domain of mode 2 can be expressed as in (3.9).

$$I_s = \frac{V_{pk}}{R} \cdot \frac{\omega}{(\omega^2 + s^2)} \tag{3.9}$$

This mode continues until the instantaneous value of the supply voltage falls below the reference DC level (V_{ref}).

MODE 3 : When the instantaneous value of the supply voltage is less than the reference DC level (V_{ref}). In this Mode,

- The bidirectional switch (side B) is turned on, and (side A) is Off.
- The capacitor is connected to the load, and the load current is completely supplied by the capacitor, while the supply is automatically disconnected by the diodes cathodes of the bridge rectifier.

The equivalent circuit for this mode is a simple RC circuit. Using similar way which is used to determine the rectifier line current of mode 1 and mode 2, the line current in the frequency domain I_s of mode 3 can be expressed as in (3.10). This mode continues until the instantaneous value of the supply voltage in the next incoming half cycle becomes greater than or equal to the reference DC level (V_{ref}). Then **MODE 1** follows as shown in figure 3.3.

$$I_s = \frac{V_{ref}}{(R_{oe} + R) \cdot (b + s)} \tag{3.10}$$

Where,

$$b = \frac{1}{(R_{oe} + R) \cdot C} \tag{3.11}$$

As a result of this circuit configuration and switching scheme, the output voltage and the capacitor voltage waveforms will be as shown in figures 3.5 and 3.6 respectively.

The value of the output voltage of the proposed rectifier can be expressed as in (3.12), and the average DC output voltage is given by (3.13)

$$V_{out} = \begin{cases} V_{pk}\ \sin(\omega t) & t_a \leq t < \frac{1}{2}t_T - t_a \\ V_{pk}\ e^{-\frac{t}{C(R+R_{oe})}} & \frac{1}{2}t_T - t_a \leq t < \frac{1}{2}t_T + t_a \end{cases} \tag{3.12}$$

$$V_{DC} = \frac{2}{t_T}\left[\int_{t_a}^{\frac{1}{2}t_T - t_a} V_{pk}\ \sin(\omega t)\ dt + \int_{\frac{1}{2}t_T - t_a}^{\frac{1}{2}t_T + t_a} V_{pk}\ e^{-\frac{t}{C(R+R_{oe})}}\ dt\right] \tag{3.13}$$

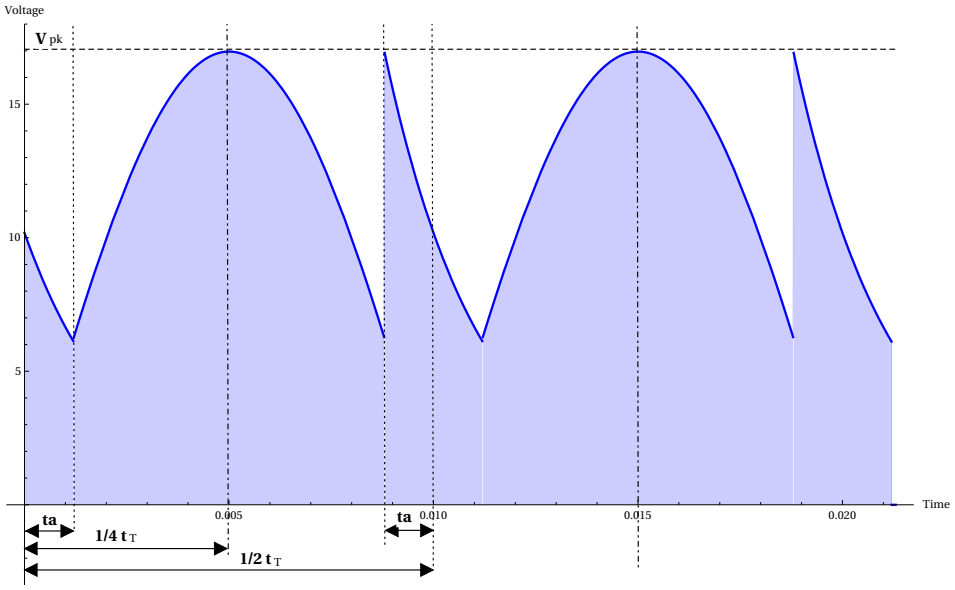


Figure 3.5: Analytical Rectifier Output Voltage Waveform with the Proposed Technique

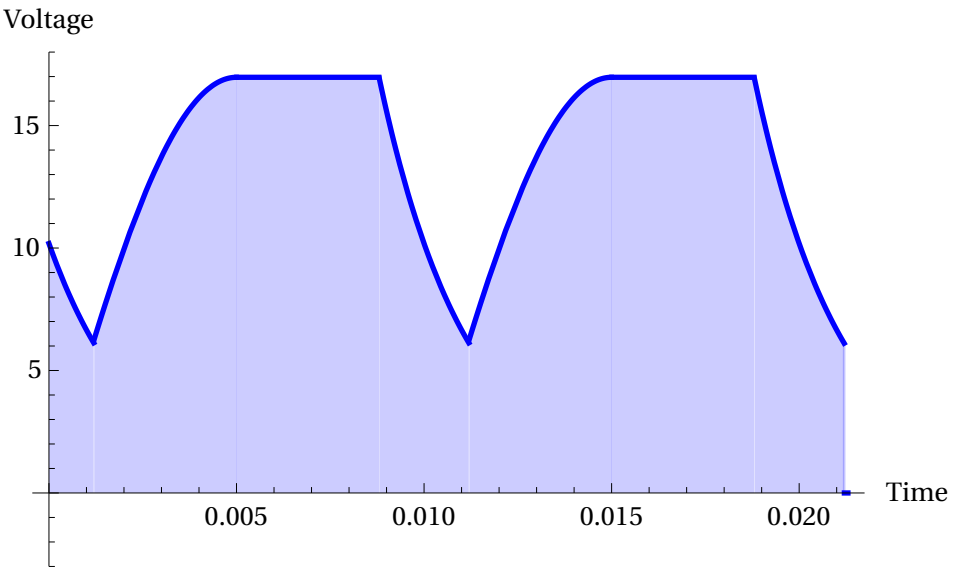


Figure 3.6: Analytical Capacitor Voltage Waveform with the Proposed Technique

It is assumed that a further DC-DC converter would be used in a practical application in order to reduce the DC voltage ripple of V_{out}. The reference DC level in this proposed architecture is to ensure any further DC-DC conversion has a defined minimum input voltage level. Typically a buck converter would be specified as having an input voltage range from the reference DC level to nearly the peak value of the supply voltage V_{pk}.

3.3 AC Side Analysis (Approximate Approach)

The analytical line current waveform of the proposed rectifier with the approximate approach is shown in figure 3.7.

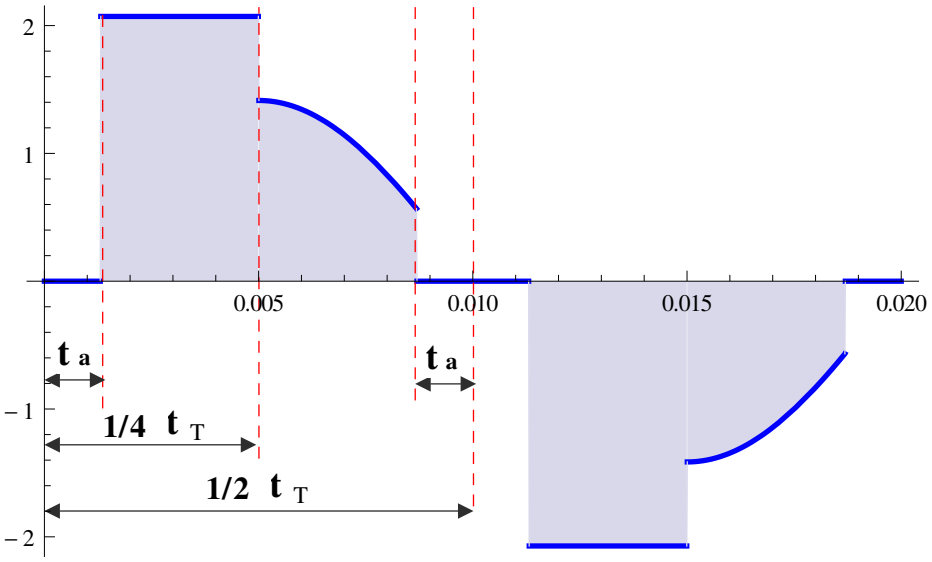


Figure 3.7: Analytical Rectifier Line Current Waveform with the Proposed Technique (Approx.)

Some approximations to the actual line current waveform have been made in order to simplify the waveform. These approximations result in an upper limit of the harmonic content of the line current.

It is clear that the line current is spread out over a wider area compared to a conventional single-phase rectifier. This current consists of three portions or segments which came from the three operating conditions described in 3.2.2.

The first period extends $[t_a \leq t < \frac{1}{4}t_T]$. This current segment represents the line current flowing in mode 1. In this period the supply voltage is connected to the load and as well as to the storage capacitor.

The second period extends $[\frac{1}{4}t_T \leq t < (\frac{1}{2}t_T - t_a)]$. This current segment represents the line current flowing in mode 2. The current waveform in this period is on the form of sinusoidal as the supply voltage is directly connected to the resistive load.

Zero line current period extends $[0 \leq t < t_a]$ & $[(\frac{1}{2}t_T - t_a) \leq t < \frac{1}{2}t_T]$. This segment represents mode 3, where the supply voltage is completely disconnected from the load

side (line current equal to zero) and the load current is fully supplied by the storage capacitor. It can be expressed the line current with it's three periods as follows:

$$\mathrm{i}(t) = \begin{cases} I_{pk} & t_a \leq t < \frac{1}{4}t_T \\ I_{sk}\sin(\omega t) & \frac{1}{4}t_T \leq t < \frac{1}{2}t_T - t_a \\ 0 & \text{otherwise} \end{cases} \tag{3.14}$$

Where, $\omega = 2\pi f$, I_{pk} is the peak value of the rectangular pulse of line current, I_{sk} is the peak value of the sinusoidal piecewise of line current.

To clarify the performance of the proposed technique, the AC side analysis of the new rectifier is done using Woodward's notation [82]. Woodward's notation is considered a powerful method in analysing piecewise waveforms in terms of Fourier series expansion, Fourier transform and frequency spectrum. It simplifies and makes it easier to deal with complicated waveforms like chopped waveforms or waveforms composed of different shapes.

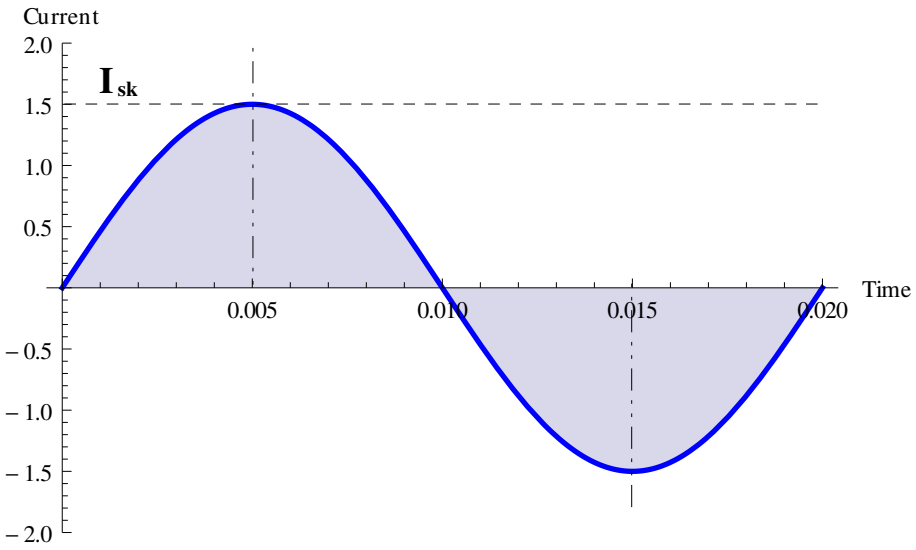
AC side analysis also included the derivations to determine the THD, the input power factor and the size of the DC bus capacitor.

- All necessary definitions and figures of the Woodward's notation is presented in A.1 of appendix A.

- The line current waveform which is shown in figure 3.7 can be built using two expressions. The first expression is for the portion of waveform that represent line current during mode 1, while the second is for the portion of waveform that is a chopped sinusoid and represents the current during mode 2. The process of obtaining the expression for the chopped sinusoid is first described here and then it will be applied to the full current waveform.

  The waveform of a pure sinusoid with a peak of I_{sk} is shown in figure 3.8.

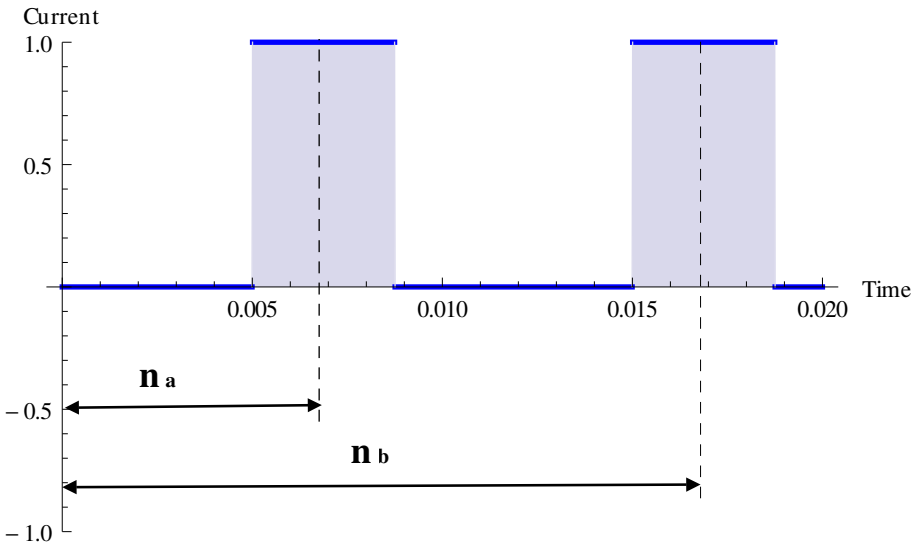
  This pure sinusoid waveform is multiplied with a train of unity amplitude Rect



$$I_{sk}\sin(2\pi ft),\ \ f = 50\ H_z$$

Figure 3.8: Pure Sinusoid Waveform

functions which is shown in figure 3.9 that can lead to a chopped sinusoid as shown in figure 3.10, which represent the line current in mode 2.



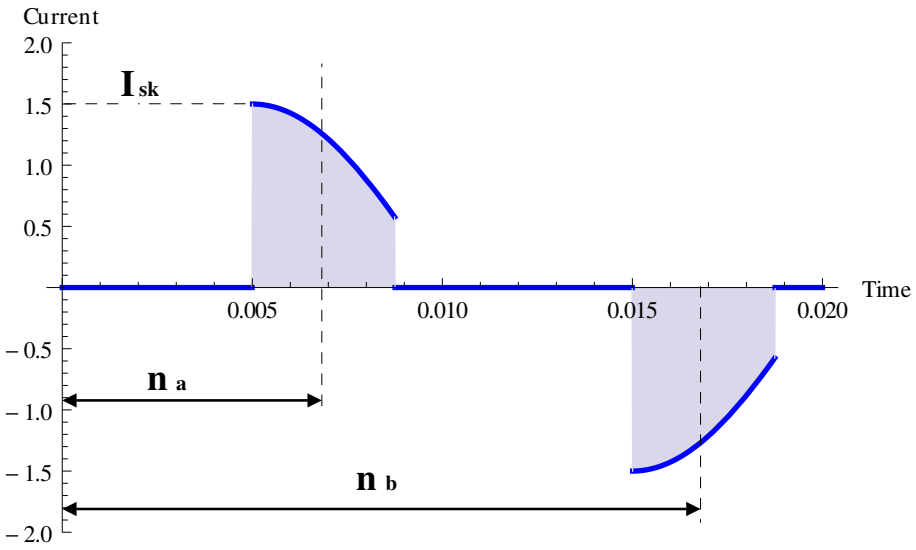
$$\mathcal{R}\left(t, n_a, \mathcal{W}\right) + \mathcal{R}\left(t, n_b, \mathcal{W}\right)$$

Figure 3.9: Unity Amplitude Rect Pulses

The Rect pulses of the rectangular segments of the line current with a peak of I_{pk} are shown in figure 3.11, which represent the line current in mode 1.

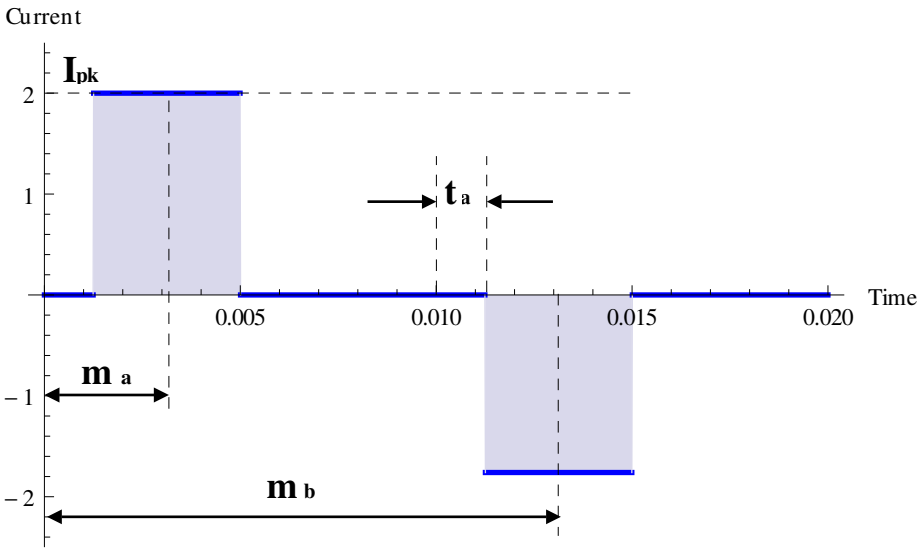
The final waveform is a sum of Rect pulses and the chopped sinusoid where,

$i(t) = i_1(t) + i_2(t)$, as shown in figure 3.7.



$$i_2\ (t) = I_{sk} \sin(\omega t)\left[\mathcal{R}\left(t, n_a, \mathcal{W}\right) + \mathcal{R}\left(t, n_b, \mathcal{W}\right)\right]$$

Figure 3.10: Sinusoid Multiplied By Unity Amplitude Rect Pulses



$$i_1\ (t) = I_{pk}\left[\mathcal{R}\left(t, m_a, \mathcal{W}\right) - \mathcal{R}\left(t, m_b, \mathcal{W}\right)\right]$$

Figure 3.11: Rect Pulses of the Rectangular Segments of the Line Current

- The mathematical process that describes this procedure is as follows

  Given design parameters, V_{pk}, V_{ref}, f, R.

  Defining

  α is zero line current period in degree, t_a is zero line current period in time.

$$\alpha = \sin^{-1}\left(\frac{V_{ref}}{V_{pk}}\right) \tag{3.15}$$

$$t_a = \left[\left(\frac{\alpha}{90}\right)\left(\frac{1}{4\,f}\right)\right] \tag{3.16}$$

  Using definitions

$$\mathcal{R}\left(t, a, W\right) = \text{Rect}\left[\frac{t-a}{W}\right] \tag{3.17}$$

$$\mathcal{S}\left(f, a, W\right) = |W|\ \text{Sinc}\left(W f\right) \cdot e^{-i2\pi a f} \tag{3.18}$$

  In figure 3.9, 3.13, and 3.11.

$$m_a = \left[t_a + \frac{1}{4f}\right] 0.5 \tag{3.19}$$

$$m_b = \left[t_a + \frac{5}{4f}\right] 0.5 \tag{3.20}$$

$$\mathcal{W} = \left(\frac{1}{4f} - t_a\right) \tag{3.21}$$

$$n_a = \frac{1}{4f} + \frac{\mathcal{W}}{2} \tag{3.22}$$

$$n_b = \frac{3}{4f} + \frac{\mathcal{W}}{2} \tag{3.23}$$

  The multiplication of the pure sinusoid with the unity amplitude Rect pulses leads to the convolution of the expressions in the frequency domain.

Starting with

$$|W| \text{ Sinc } [fW] \cdot e^{-i2\pi af}$$

And convolve it with the frequency domain expression of a pure sinusoid of frequency d given by

$$\frac{i}{2}\left[\delta(d) - \delta(-d)\right]$$

where $\delta(d)$ is a Dirac function, $d = 50$.

The convolution

$$\left(|W| \text{ Sinc } [fW] \cdot e^{-i2\pi af}\right) * \left(\frac{i}{2}\left[\delta(d) - \delta(-d)\right]\right)$$

where $*$ denotes the convolution operator, leads to

$$\begin{aligned} |W|\frac{i}{2}\big[&\text{Sinc}\left[(f+d)W\right]e^{-i2\pi a(f+d)} \\ &-\text{Sinc}\left[(f-d)W\right]e^{-i2\pi a(f-d)}\big] \end{aligned}$$

Thus defining a new function

$$\begin{aligned} \mathcal{S}_n(f,a,w,d) = \frac{|W|i}{2}\big[&\text{Sinc}\left[(f+d)W\right]e^{-i2\pi a(f+d)} \\ &-\text{Sinc}\left[(f-d)W\right]e^{-i2\pi a(f-d)}\big] \end{aligned} \tag{3.24}$$

This then leads to the following expression for the current waveform shown in figure 3.7.

$$\begin{aligned} i(t) =& I_{pk}\left[\mathcal{R}(t,m_a,\mathcal{W}) - \mathcal{R}(t,m_b,\mathcal{W})\right] + \\ & I_{sk}\sin(\omega t)\left[\mathcal{R}(t,n_a,\mathcal{W}) + \mathcal{R}(t,n_b,\mathcal{W})\right] \end{aligned} \tag{3.25}$$

This then enables to get an expression for the frequency domain spectra from inspection as

$$\begin{aligned} I(f) =& I_{pk}\left[\mathcal{S}\left(f, m_a, \mathcal{W}\right) - \mathcal{S}\left(f, m_b, \mathcal{W}\right)\right] + \\ & I_{sk}\left[\mathcal{S}_n\left(f, n_a, \mathcal{W}, d\right) + \mathcal{S}_n\left(f, n_b, \mathcal{W}, d\right)\right] \end{aligned} \tag{3.26}$$

Assuming the current is periodic, the spectral components at integer multiples of f are defined as

$$A(n) = \mathrm{Re}[I(fn)]2f \tag{3.27}$$

$$B(n) = -\,\mathrm{Im}[I(fn)]2f \tag{3.28}$$

Where, n is an integer, and this results in the following Fourier series expansion for $i(t, n)$.

$$i_h(t, n) = [A(n)\cos(\omega nt) + B(n)\sin(\omega nt)] \tag{3.29}$$

Where, i_h is the rms value of current of harmonic order n.

$$i(t, n) = \sum_{k=1}^{n} i_h(t, k) \tag{3.30}$$

And the magnitude of spectral component at n is given by

$$S(n) = \sqrt{A(n)^2 + B(n)^2} \tag{3.31}$$

- The capacitance of the storage capacitor can be expressed as in the following formula

$$C = \frac{2\ t_a}{\ln(\frac{V_{pk}}{V_{ref}}) \cdot (R + R_{oe})} \tag{3.32}$$

- The THD can be derived from the above expression of line current in frequency domain.

  Starting with (3.26),

  Let

  $\mathcal{S}\left(f, m_a, \mathcal{W}\right) = \mathcal{A},\ \ \mathcal{S}\left(f, m_b, \mathcal{W}\right) = \mathcal{B}.$

  $\mathcal{S}\left(f, n_a, \mathcal{W}, d\right) = \mathcal{C},\ \ \mathcal{S}\left(f, n_b, \mathcal{W}, d\right) = \mathcal{D}.$

$$I(f) = I_{pk}\left[\mathcal{A} - \mathcal{B}\right] + I_{sk}\left[\mathcal{C} + \mathcal{D}\right] \tag{3.33}$$

  At $t = \frac{1}{4}\ t_T$,

$$I_c = \frac{C(V_{pk} - V_{ref})}{(\frac{1}{4} \cdot t_T - t_a)} \tag{3.34}$$

  Where, I_c is the current of the storage capacitor.

$$I_{sk} = \frac{V_{pk}}{R} \tag{3.35}$$

  And

$$I_{pk} = I_{sk} + I_c \tag{3.36}$$

  Let

$$\gamma = \left(1 - \frac{V_{ref}}{V_{pk}}\right) \tag{3.37}$$

$$\beta = \frac{2\ t_a \cdot \gamma}{\ln(\frac{V_{pk}}{V_{ref}})(\frac{1}{4}\ t_T - t_a)(1 + \frac{R_{oe}}{R})} \tag{3.38}$$

  The substitution of (3.34), (3.35), (3.37), and (3.38) in (3.36) will result in

$$I_{pk} = I_{sk}\ [1 + \beta] \tag{3.39}$$

Then the substitution of (3.39) in (3.33), will result the following expression for the frequency domain spectra of the input current.

$$I(f) = I_{sk} \ ([1+\beta] \cdot [\mathcal{A} - \mathcal{B}] + [\mathcal{C} + \mathcal{D}]) \tag{3.40}$$

Using definition of THD,

$$THD = \sqrt{\sum_{h=2}^{40} \left(\frac{I_h}{I_1}\right)^2} \tag{3.41}$$

Where I_1 is the frequency spectra of the fundamental harmonic, I_h is the frequency spectra of the harmonic order h.

This then enables to get the final expression of THD for the line current of the proposed technique.

$$THD = \sqrt{\sum_{h=2}^{40} \left(\frac{[1+\beta] \cdot [\mathcal{A}_n - \mathcal{B}_n] + [\mathcal{C}_n + \mathcal{D}_n]}{[1+\beta] \cdot [\mathcal{A} - \mathcal{B}] + [\mathcal{C} + \mathcal{D}]}\right)^2} \tag{3.42}$$

Where, $\mathcal{A}_n$, $\mathcal{B}_n$, $\mathcal{C}_n$, and $\mathcal{D}_n$, are the frequency spectra of $(n \cdot f)$ harmonic order.

- The input power factor PF can be derived as follows

  Starting with

$$PF = \frac{P_{av}}{P_{va}} \tag{3.43}$$

Where P_{av} is the average input power, P_{va} is the Volt-Amperes.

$$P_{av} = \frac{1}{t_T} \int_0^{t_T} v(t) \cdot i(t) \ dt \tag{3.44}$$

Where $i(t)$ is as expressed in (3.25), or it can be expressed as in (3.14), $v(t)$ is the input voltage.

$$v(t) = V_{pk} \cdot \sin(\omega t) \tag{3.45}$$

That leads to the following expression of average input power

$$P_{av} = V_{pk} \left[I_{pk} \cdot J + I_{sk} \cdot K \right] \tag{3.46}$$

Where,

$$J = \left(\frac{\cos(\omega t_a)}{\pi} \right) \tag{3.47}$$

$$K = \left(\frac{1}{4} - \frac{t_a}{t_T} \right) + \left(\frac{\sin(2\omega t_a)}{4\pi} \right) \tag{3.48}$$

The Volt-Amperes

$$P_{va} = I_{rms} \cdot V_{rms} \tag{3.49}$$

Where,

$$V_{rms} = \frac{V_{pk}}{\sqrt{2}} \tag{3.50}$$

$$I_{rms} = \sqrt{\frac{1}{t_T} \int_0^{t_T} \left[i(t)^2 \right] \, dt} \tag{3.51}$$

Applying the current expression of (3.14) in (3.51), then multiplying the result by V_{rms} to get the final expression for (3.49).

$$P_{va} = \frac{V_{pk}^2}{\sqrt{2} \cdot R} \sqrt{\left[1 + \beta \right]^2 \cdot E + K} \tag{3.52}$$

Where,

$$E = \left(\frac{1}{2} - \frac{2\, t_a}{t_T} \right) \tag{3.53}$$

Applying the expressions of (3.46) and (3.52) in (3.43), to get the final expression of input power factor

$$PF = \frac{\sqrt{2} \cdot [(1+\beta) \cdot J + K]}{\sqrt{(1+\beta)^2 \cdot E + K}} \tag{3.54}$$

3.4 AC Side Analysis (Exact Approach)

The analytical line current waveform of the proposed rectifier with the exact approach will be as shown in figure 3.12.

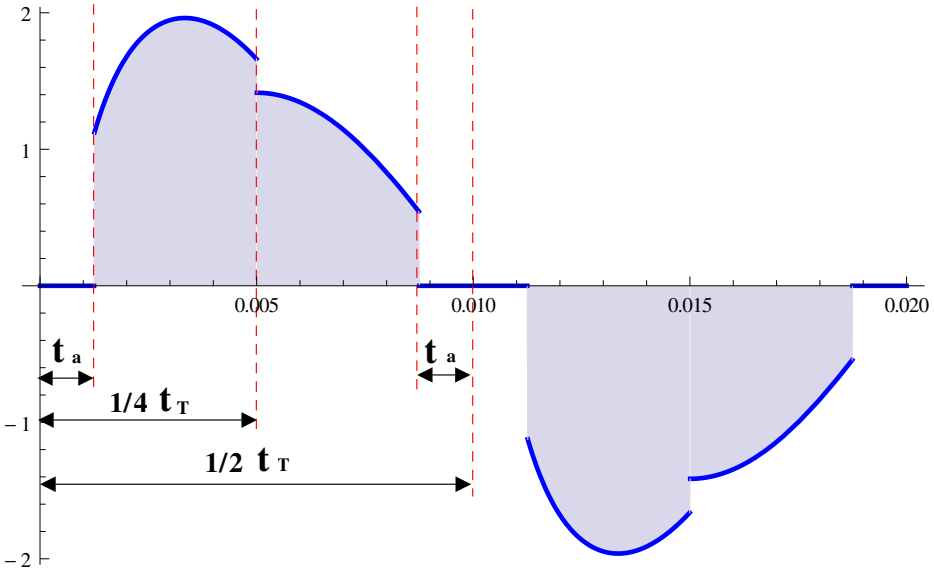


Figure 3.12: Analytical Rectifier Line Current Waveform with the Proposed Technique (Exact)

In comparison with the current waveform presented in figure 3.7, this current is more accurate and closer to reality as it came from the exact expression of the line current with no approximations or assumptions having been made.

It can be expressed the line current with it's three periods as follows:

$$\mathrm{i}(t) \quad = \quad \begin{cases} i_1(t) & t_a \leq t < \frac{1}{4}t_T \\ i_2(t) & \frac{1}{4}t_T \leq t < \frac{1}{2}t_T - t_a \\ 0 & \text{otherwise} \end{cases} \tag{3.55}$$

Where

$i_1(t)$ is the line current flowing during mode 1 and its expression is given by (3.58), $i_2(t)$ is the line current flowing during mode 2 and its expression is given by (3.56).

$$i_1(t) = \frac{a^2 R_{oe} V_{pk} \sin(\omega t) + \omega a R V_{pk} \cos(\omega t) + \omega^2 R V_{pk} \sin(\omega t) + \omega^2 R_{oe} V_{pk} \sin(\omega t)}{R R_{oe} \left(a^2 + \omega^2\right)} + \frac{e^{-at}\left(a^2(-V_{ref}) - \omega a V_{pk} - \omega^2 V_{ref}\right)}{R_{oe}\left(a^2 + \omega^2\right)} \quad (3.58)$$

$$i_2(t) = I_{sk} \sin(\omega t) \quad (3.56)$$

$$I_{sk} = \frac{V_{pk}}{R} \quad (3.57)$$

Where, I_{sk} is the peak value of line current in (mode 2), I_{pk} is the peak value of line current in (mode 1).

The full details of the inverse Laplace transformation code of $i_1(t)$ using Wolfram Mathematica 10.1, is presented in B.1 of appendix B.

To clarify the frequency content of the line current of the proposed rectifier with the exact approach, the AC side analysis of the rectifier has been done. In order to get the full and exact current formula for each of the current segments, the equivalent circuit of each mode in Laplace domain is determined and the rectifier current in frequency domain is obtained. The inverse Laplace transform is applied to get the full current formula in time domain. The representation of the rectifier current then is done using Woodward's notation [82].

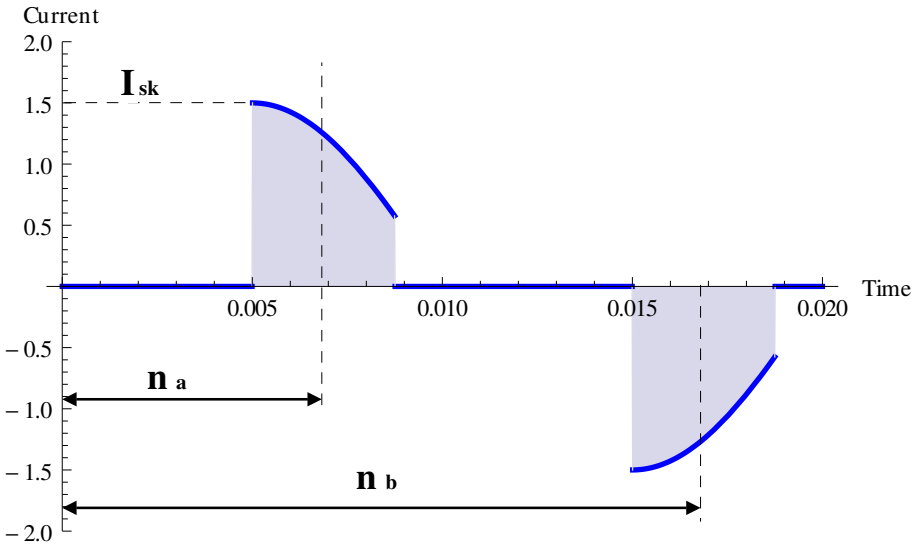
The AC side analysis also includes the calculations to determine the THD and the input power factor. This analysis is done using Wolfram Mathematica 10.1, and it's results are verified by the experimental results of a range of case studies.

- All necessary definitions and figures of the Woodward's notation can be found in A.1 of appendix A.

- The line current waveform shown in figure 3.12 can be built using two expressions. The first expression is for the portion of waveform that represent line current during mode 1, while the second is for the portion of waveform that is a chopped sinusoid and represents the current during mode 2. The process of obtaining the expression

for the chopped sinusoid is first described here and then it will be applied to the full current waveform.

The waveform of a pure sinusoid shown in figure 3.8, is multiplied with a train of unity amplitude Rect function which shown in figure 3.9, that can lead to a chopped sinusoid waveform as shown in figure 3.13, which represent the line current of the rectifier in mode 2.



$$i_b\ (t) = i_2(t)\left[\mathcal{R}\left(t, n_a, \mathcal{W}\right) + \mathcal{R}\left(t, n_b, \mathcal{W}\right)\right]$$

Figure 3.13: Sinusoid Multiplied by Unity Amplitude Rect Pulses

The same process can be applied to get an expression for the current in mode 1. The line current waveform of mode 1 which described in (3.58) is multiplied with a train of unity amplitude Rect function. This can lead to the current waveform shown in figure 3.14.

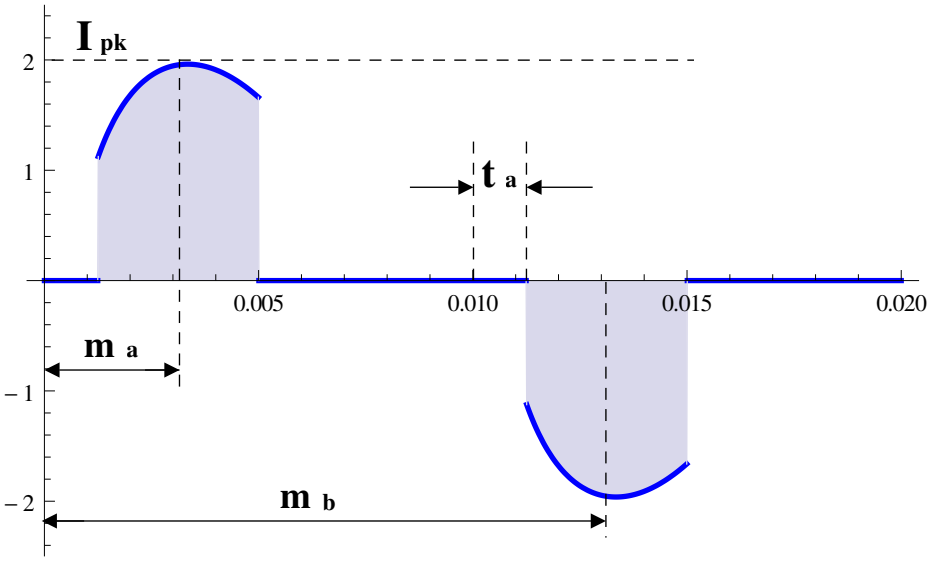
The final waveform is a sum of the two waveforms portions $i(t) = i_a(t) + i_b(t)$ as shown in figure 3.12.

- The mathematical process that describes this procedure is as follows

  Given a design parameters, V_{pk}, V_{ref}, f, R.

  Using the definitions were mentioned in (3.15) - (3.23).

  This then leads to the following expression for the current waveform shown in figure 3.12.



$$i_a\ (t) = i_1(t)\left[\mathcal{R}\left(t, m_a, \mathcal{W}\right)\right] - i_1\left(t - \tfrac{1}{2}t_T\right)\left[\mathcal{R}\left(t, m_b, \mathcal{W}\right)\right]$$

Figure 3.14: Rect Pulses of the Line Current in Mode 1

$$\begin{aligned} i(t) =& i_1(t)\left[\mathcal{R}\left(t, m_a, \mathcal{W}\right)\right] - i_1\left(t - \frac{1}{2}t_T\right)\left[\mathcal{R}\left(t, m_b, \mathcal{W}\right)\right] + \\ & i_2(t)\left[\mathcal{R}\left(t, n_a, \mathcal{W}\right) + \mathcal{R}\left(t, n_b, \mathcal{W}\right)\right] \end{aligned} \tag{3.59}$$

Assuming the current is periodic, the spectral components at integer multiples of f are defined as

$$A(n) = \frac{2}{t_T}\int_0^{t_T} i(t)\cos(\omega n t) \tag{3.60}$$

$$B(n) = \frac{2}{t_T}\int_0^{t_T} i(t)\sin(\omega n t) \tag{3.61}$$

Where n is an integer.

Using Fourier series expansion for $i(t, n)$ mentioned in (3.29) and (3.30), and the expression for the magnitude of spectral component given in (3.31).

- The THD can be derived from the expression of line current in the time domain given in (3.59), using the definition of the THD mentioned in (3.41).
- The capacitance of the storage capacitor is the same as in (3.32).

- The input power factor can be derived using the definition of the power factor mentioned in (3.43), while the expressions for the average input power and the Volt-Ampere are given in (3.44) and (3.49) respectively.

3.5 The Experimental Set-up

The prototype circuit of the proposed rectifier and the control circuit have been designed and fabricated. The layout of the prototype circuits of the proposed rectifier and the control scheme are shown in figures C.1, C.2 respectively in appendix C.

The control system has been designed to generate two different control signals which are used to fire two MOSFET driver circuits (both sides of the bidirectional switch circuit). Two N-channel MOSFETs have been used as switching devices with high-side MOSFET drivers to drive them.

The function of the control system is to generate the control signals according to the intersection points between the instantaneous values of the full wave rectifier output voltage and the reference DC level (V_{ref}). This ensures the implementation of the three operation modes mentioned in 3.2.2.

The heart of this design lies in the implementation of the control system commands onto both sides of the bidirectional switch circuit. Both sides of the bidirectional switch circuit are performed switching between two high potential sides. The first high potential side is the output voltage of the bridge rectifier whilst the second is the potential of the storage capacitor.

The continuous potential fluctuation across the switching device (MOSFETs), forced them to switch according to the required gate-source voltage (not according to the control commands) which is critical to ensure the correct operation.

The prototype circuit of the conventional single-phase rectifier has also been fabricated and tested in order to compare the performances of both rectifiers under an identical testing conditions.

3.6 Cases of Studies

In order to prove the validity of the proposed rectifier with further clarification for its characteristics and to demonstrate its advantages over the conventional system. A comparison between the performances of both rectifiers has been done.

Two case studies have been undertaken:

1. Conventional single phase rectifier.

2. Proposed single phase rectifier.

The performance analysis of both case studies are presented and discussed. The scales of the graphs in both cases have been kept identical in order to clarify the differences between them.

Some approximations to the practical waveforms of the line current in both case studies have been made in order to simplify the waveforms. These approximations result in an upper limit to the harmonic content of the line current. The input voltage waveform in this section is assumed to be a pure sinusoid, however the experimental input voltage waveform is best described as an asymmetric-flat-top sinusoid.

In order to ensure robust comparison between the two cases, the experimental set-up in both cases have been done under identical testing conditions. An identical input power supply and loading conditions have been applied. A power supply of 12V rms, 50 Hz, and a resistive load of 12 Ω, have been used.

3.6.1 Conventional Single Phase Rectifier

The full details of the harmonic analysis of the line current of the conventional rectifier is presented in A.2 of appendix A. This analysis is done using Woodward's notation [82].

The performance analysis of this case study is illustrated below. The full details of the performance analysis code using Wolfram Mathematica 10.1, for this case study is presented in B.2 of appendix B.

- The analytical line current waveform is shown in figure 3.15. Although the load is pure resistive, the line current flows for a short period of time and it seems as a short surge of current. This is the required current to charge the smoothing capacitor in the DC side of the rectifier.

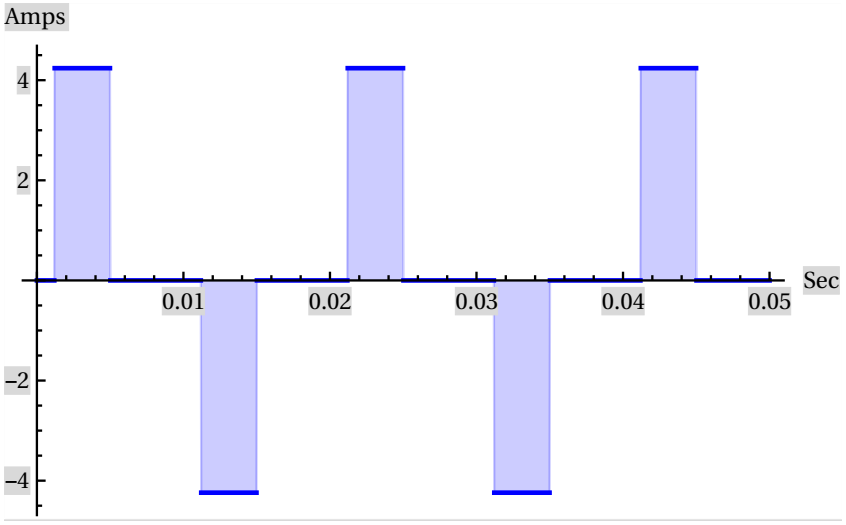


Figure 3.15: Analytical Line Current Waveform of the Conventional Rectifier

- The rms value of the line current is computed after identifying the period of the squared current waveform. The squared current waveform is shown in figure 3.16. The rms value of the line current for this case is computed as 2.6 Amps.

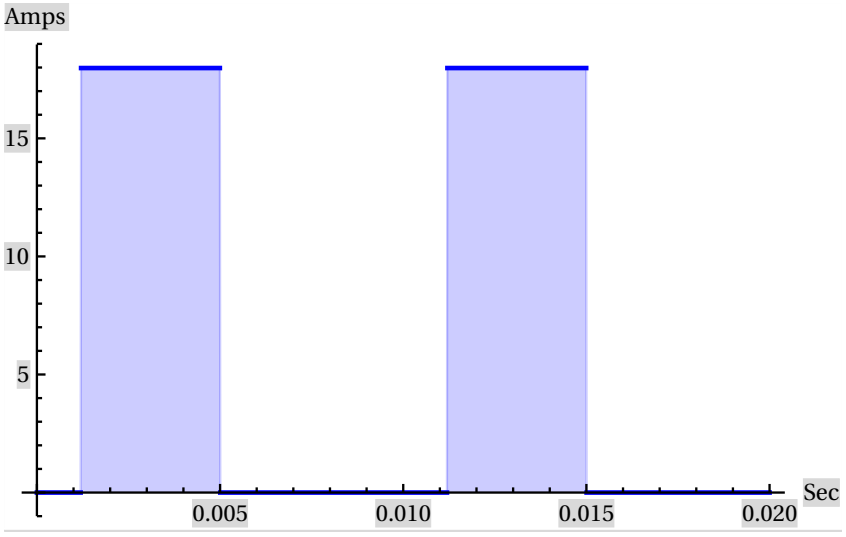


Figure 3.16: Analytical Squared Line Current Waveform of the Conventional Rectifier

- The volt-amperes can be obtained from the rms values of the input current and voltage. The average value of the instantaneous input power can be determined

from the input current and voltage waveforms. Figure 3.17 shows the instantaneous input power waveform. The Volt-Amperes and the average value of the instantaneous input power are computed as 31.35 VA and 21.29 W respectively.

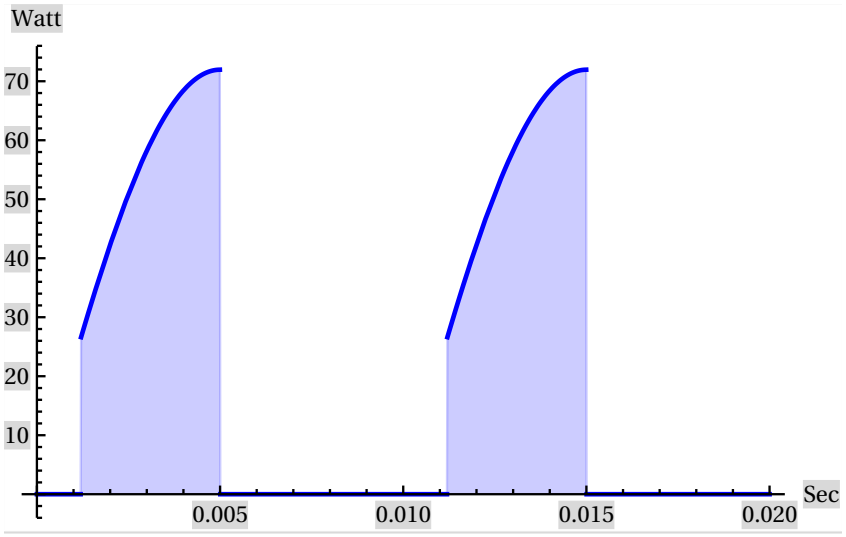


Figure 3.17: Analytical Instantaneous Input Power Waveform of the Conventional Rectifier

- The input power factor can be easily evaluated from the Volt-Amperes and the average value of the instantaneous input power calculations.

$$PF = \frac{21.29}{31.35} = 0.67$$

It is noted that, although the load is pure resistive, the value of power factor is around 67% from the default value for pure resistive load (unity power factor).

- The displacement factor can be evaluated from the displacement angle θ.

It is the angle between the fundamental component of the input current and voltage waveforms. This angle can be evaluated through the harmonic analysis of the line current of the conventional rectifier presented in A.2 of appendix A. The displacement factor for this case is computed as 0.82.

Figure 3.18 shows the displacement angle for this case study. Both the fundamental component of the input current and the input voltage waveforms have been plotted

together with an amplitude of unity, in order to clarify the displacement angle between them.

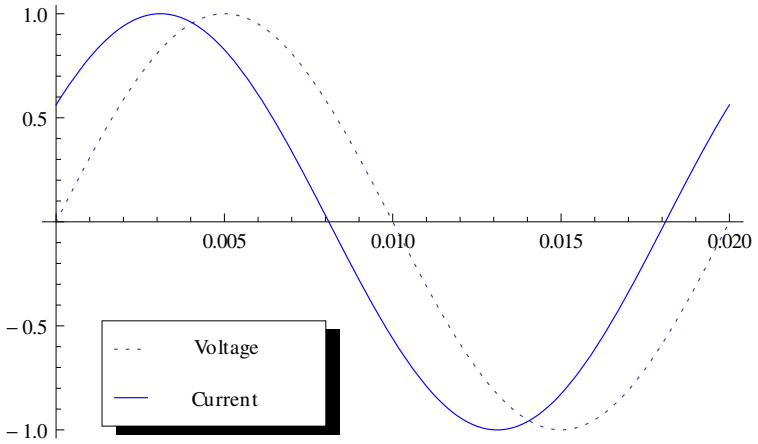


Figure 3.18: Analytical Displacement Angle of the Conventional Rectifier

- The distortion factor can be determined from the values of displacement factor and power factor.

  The distortion factor for this case is found as 0.81. The distortion factor is considered a good indicator for the system losses caused by harmonics. It reflects how big the harmonic distortion occurs in the line current of the rectifier.

- The Fourier analysis of a wide band of harmonic orders of the line current have been done. This band is from the fundamental component up to harmonic order of 1000.

  The fundamental component of the line current with the harmonic orders of 3rd, 11th and 1000, are illustrated in figure 3.19.

  It is noted from the way that harmonics are distributed, the peak of most harmonic components occurs in a short period of time. This way of harmonic distribution will produce a short surge of line current.

  The full details of the Fourier analysis for the conventional rectifier is presented in A.2 of appendix A. The final formula that used to determine the Fourier analysis

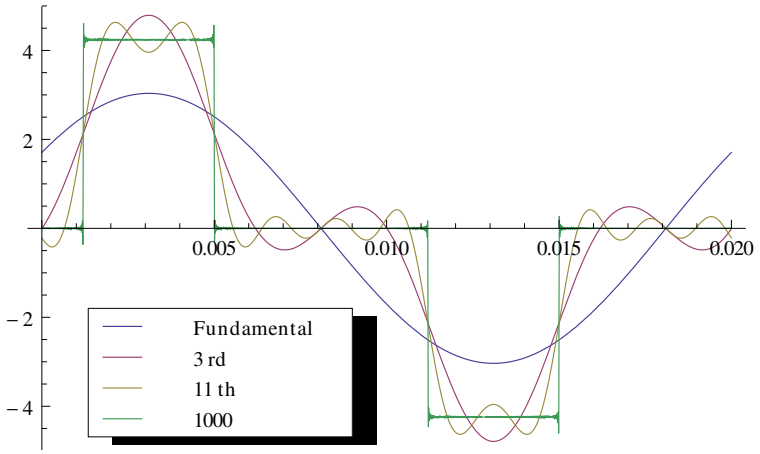


Figure 3.19: Fourier Analysis of the Line Current of the Conventional Rectifier

for this case is given by (3.30).

- The frequency spectrum of the line current is shown in figure 3.20. This frequency spectrum is up to harmonic order of 40. It is valuable to note that according to the way that Wolfram Mathematica 10.1, is used to display the frequency spectrum components, I found that each component of the frequency spectrum is shifted forward by one step (ex: the spectrum component located in division 10, is actually the ninth component).

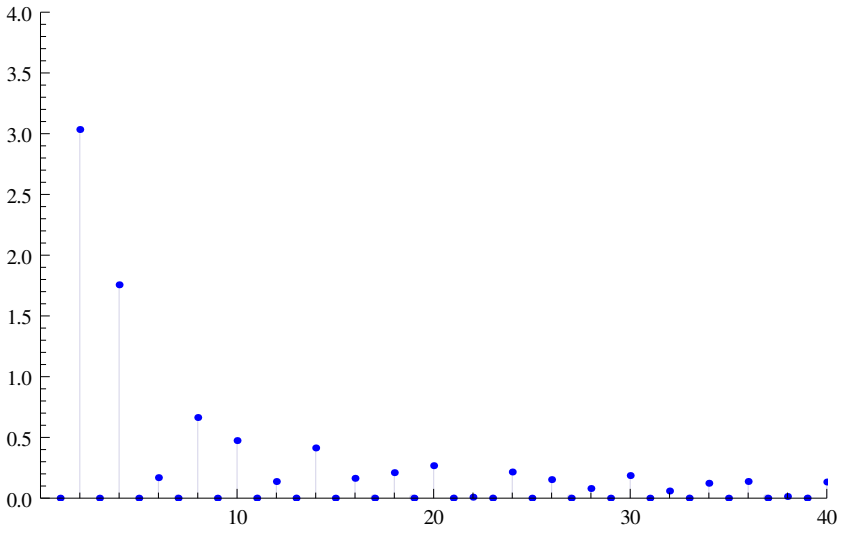


Figure 3.20: Analytical Frequency Spectrum of the Line Current of the Conventional Rectifier

In figure 3.20, the first few harmonic components have a considerable amplitude compared with the fundamental. This is undesirable in any electrical conversion application. The formula that used to represent the frequency spectrum for this case study is expressed in (3.31).

- The THD of the line current for this case is computed after calculating the harmonic components values up to harmonic order of 40.

  The expression to identify the THD is given in (3.41). This expression is used to determine the ratio of the THD related to the fundamental component value. The THD in this case is computed to be 68%. This value clearly showed how much the total distortion is happened due to the harmonics in the line current of the conventional system.

- The measured line current waveform of this case study is shown in figure 3.21.

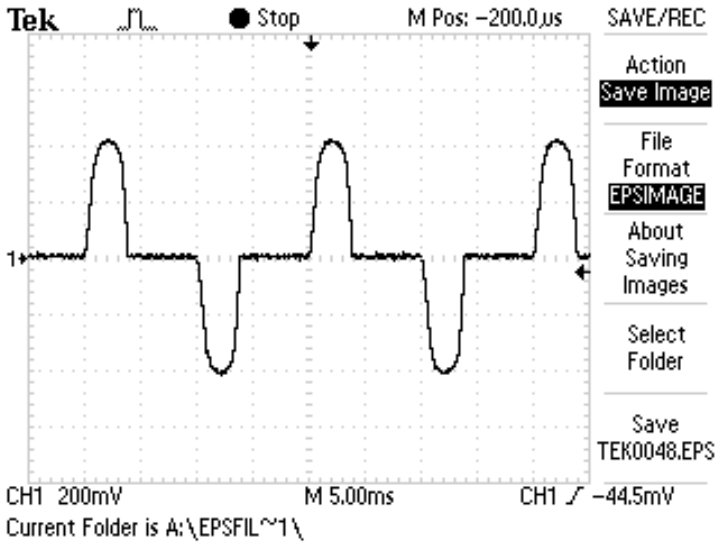


Figure 3.21: Experimental Line Current Waveform of the Conventional Rectifier

From figure 3.21, the line current waveform is too close to the rectangular pulse waveform which is fully compatible with the assumption of adopting this shape in the representation of the line current in the mathematical analysis presented in A.2 of appendix A.

- The measured output voltage waveform is shown in figure 3.22.

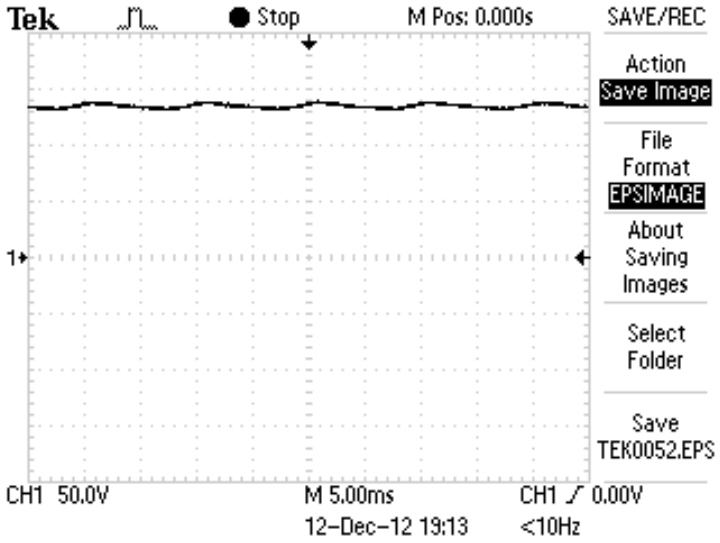


Figure 3.22: Experimental Output Voltage Waveform of the Conventional Rectifier

- The size of the smoothing capacitor that is used in this test is predetermined using the analytical solution of the formula expressed in (1.14). A graph shown in figure 1.9 represent the nomogram for this formula.

  The capacitor size is computed for this case as 12000 μF. This is the required value to keep the conduction angle at 70° , with a percentage ripple not exceed 6% from the peak value of the output voltage. This conduction angle is typical for many applications.

3.6.2 Proposed Single Phase Rectifier

The performance analysis of the new rectifier is illustrated below. The full details of the performance analysis code using Wolfram Mathematica 10.1, for this case study is presented in B.3 of appendix B.

- The analytical line current waveform (with approximate approach) is shown in figure 3.23.

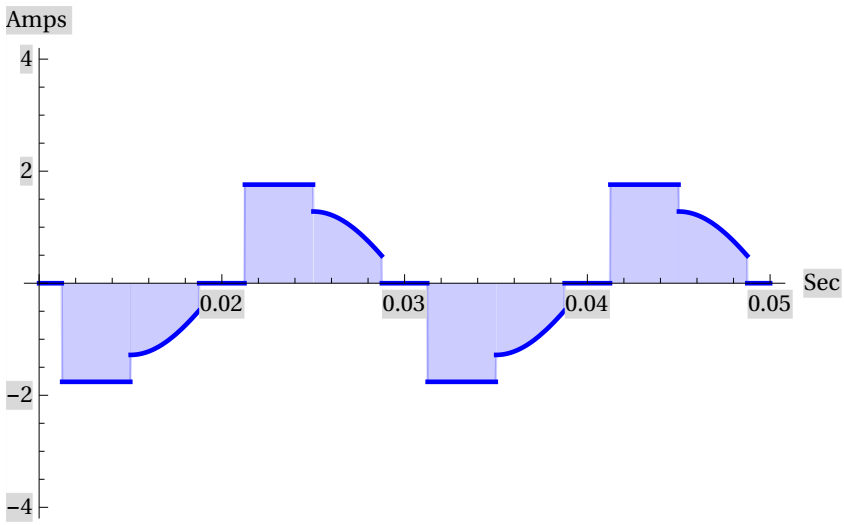


Figure 3.23: Analytical Line Current Waveform of the Proposed Rectifier

Comparing figures 3.23 and 3.15. The line current of this rectifier is spread out over a wider area. This current has an additional feature which is lower peak value than the conventional system for the same connected load (more than two times lower). The peak values of the line current in the conventional and the proposed rectifiers were 4.24 Amps, 1.76 Amps respectively.

This current consists of three segments, these three segments came from the three operating conditions or modes described in 3.2.2. The first current segment is the rectangular pulse, this piecewise current represent the line current in mode 1.

The assumption made here is that the current in this period is a rectangular pulse. This is a worst case scenario in terms of harmonic content compared to the actual observed current in the practical results.

- The rms value of the line current is computed after identifying the periods of the squared current waveform. The squared current waveform is illustrated in figure 3.24. The rms value of the line current is computed to be 1.24 Amps. This value is less than half the rms value of the line current in the conventional system.

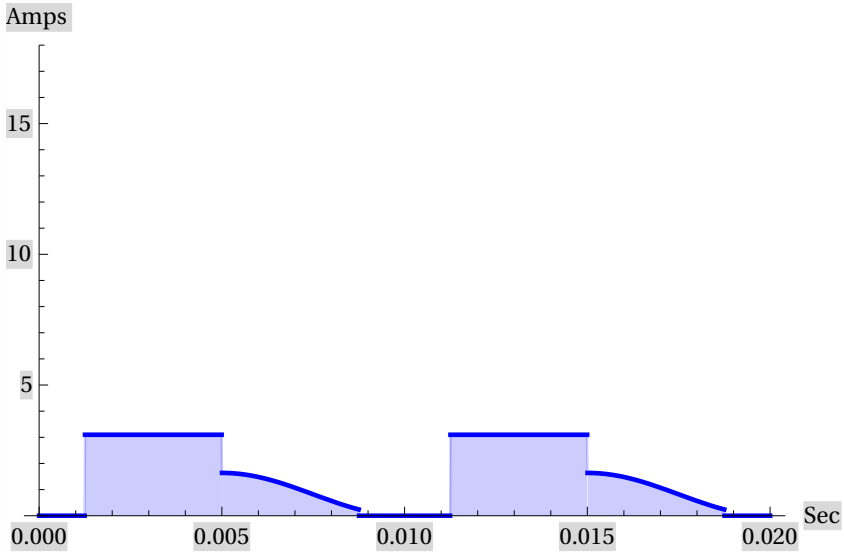


Figure 3.24: Analytical Squared Line Current Waveform of the Proposed Rectifier

- The volt-amperes is obtained from the rms values of the input current and voltage. The average value of the instantaneous input power is determined from the input current and voltage waveforms. Figure 3.25 shows the instantaneous input power waveform. The volt amperes and the average value of the instantaneous input power are computed as 14.88 VA and 14 W respectively.

  It is noted that, although the identical power supply and loading conditions have been applied in both cases studies (conventional and the proposed systems), a significant difference between the instantaneous input power waveforms in both cases can be observed. These differences are in the peak values of the input power pulses and in the period of time that each pulse is extended.

- The conduction time of the line current is crucial to determine the input power factor of the rectifier. By comparing figures 3.17 and 3.25, this time period is nearly two times bigger than the time period in the conventional system. Using the approximate approach of the AC side analysis, the input power factor is obtained

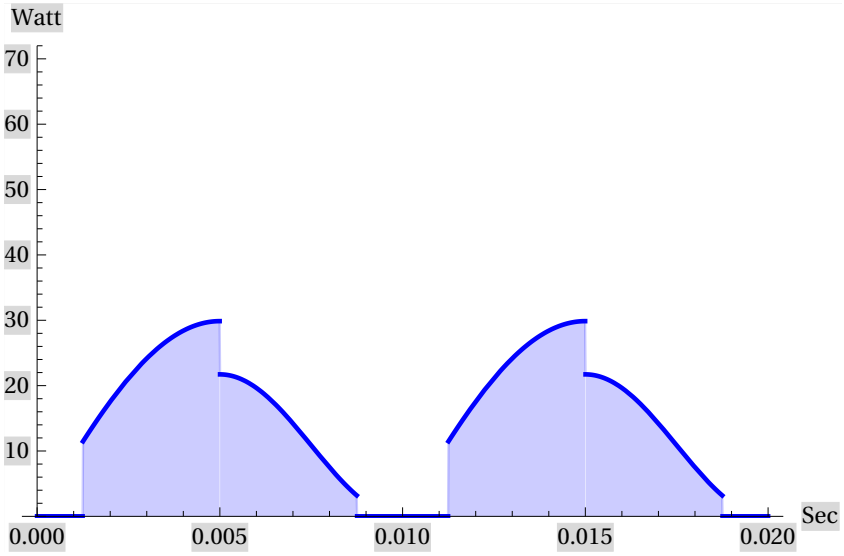


Figure 3.25: Analytical Instantaneous Input Power Waveform of the Proposed Rectifier

by applying the derived expressions of the power factor. it computed as 0.94 for this case with the approximate approach, while with the exact approach it found as 0.95.

- The displacement factor is evaluated from the displacement angle. The displacement angle is evaluated through the harmonic analysis of the line current. The full details of the harmonic analysis of the proposed rectifier is presented in 3.3. The displacement factor is computed for this case to be 0.98.

  Figure 3.26, shows the displacement angle. In order to clarify the displacement angle between the fundamental component of the line current and the input voltage waveforms, both waveforms have been plotted together with an amplitude of unity.

- The distortion factor is computed as 0.96 for this case. This value is clearly reflects how much the reduction in the total system losses that caused by harmonics compared with the conventional system.

- Fourier analysis of a wide band of harmonic orders of the line current has been done. This band is from the fundamental component up to harmonic order of 1000. The full details of the Fourier analysis for the proposed rectifier is presented in 3.3. The final formula that used to determine the Fourier analysis for this case

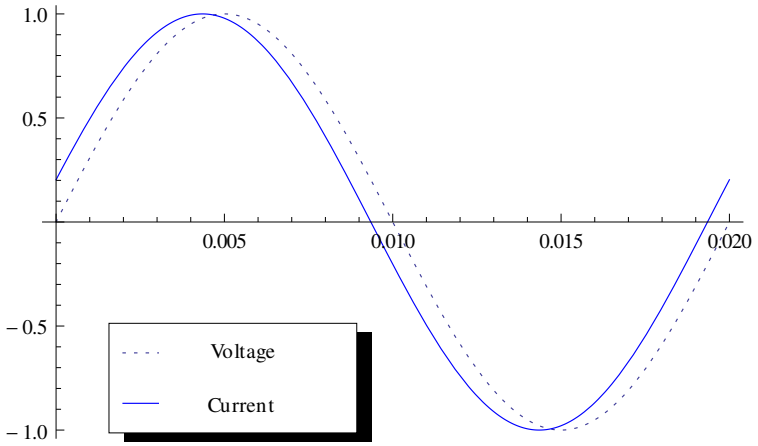


Figure 3.26: Analytical Displacement Angle of the Proposed Rectifier

is given by (3.30).

The fundamental component of the line current with the harmonic orders of 3rd, 11th and 1000, are illustrated in figure 3.27.

This figure shows the fundamental component with some of the low order harmonics which are considered the most important and influential in the performance analysis of any power conversion application. Also, it shows the harmonic order of 1000, in order to prove there is no remarkable impact of harmonics beyond or even below this point. From the shown harmonic components and the way that they are distributed, it can say there is no considerable distortion to the mains AC supply comes from the existing harmonics.

- The assumption of there is no big impact of the existing harmonic components on the mains is supported by the frequency spectrum graph of the line current.

  The frequency spectrum of the analytical line current waveform for this case in both approaches (approximate and exact) are shown in figures 3.28, 3.29 respectively. They illustrate the harmonics content up to harmonic order of 40. It can be observed that there is a slim difference in the frequency content of the frequency spectrum in both approaches.

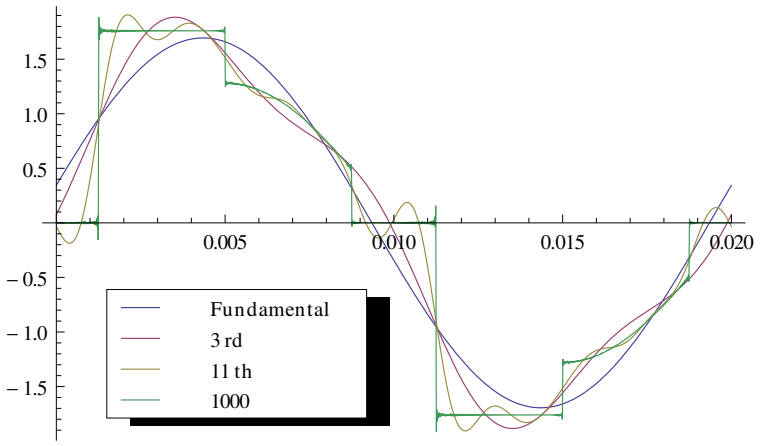


Figure 3.27: Fourier Analysis of the line Current of Proposed Rectifier

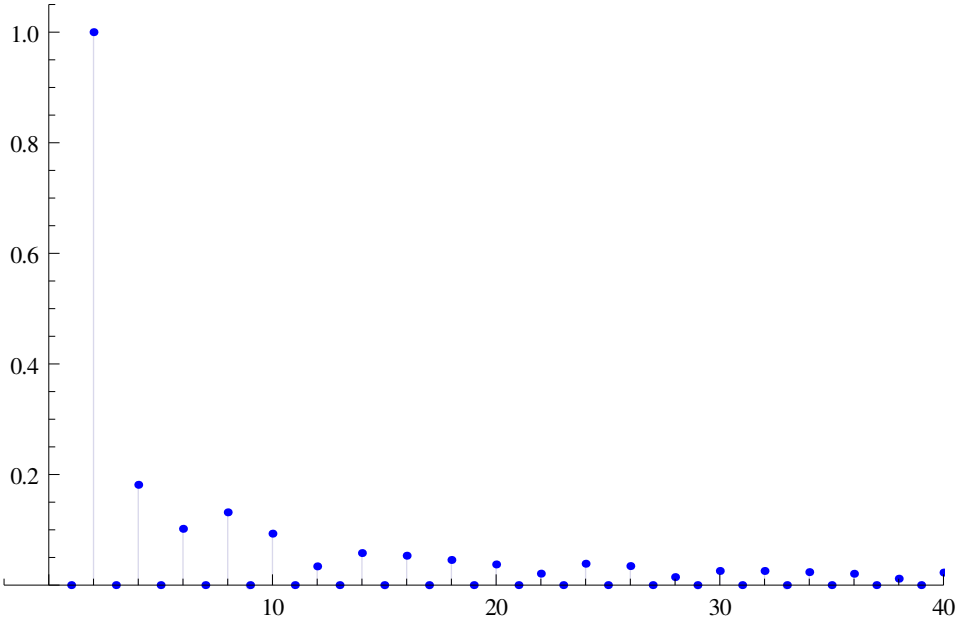


Figure 3.28: Frequency Spectrum of the Line Current with Approximate Approach

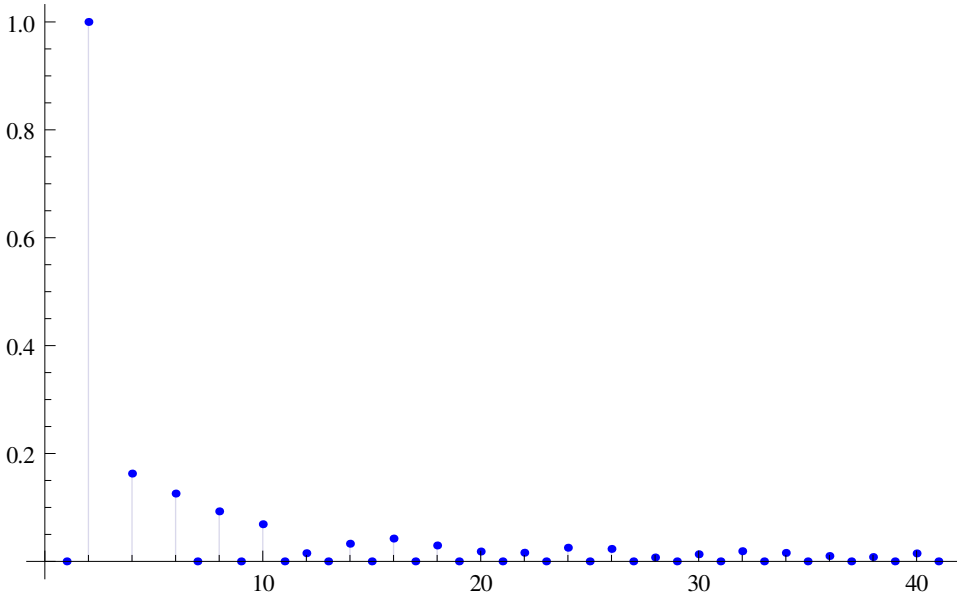


Figure 3.29: Frequency Spectrum of the Line Current with Exact Approach

These two graphs have two main features, primarily, there is no remarkable harmonic amplitude beyond the harmonic order of 9. Secondly, the amplitude of the 3rd, 5th, 7th and the 9th harmonic are small compared to the fundamental. Also the amplitude of the fundamental component in the new rectifier is approximately half the amplitude of the fundamental component in the conventional rectifier for the same case study.

- The THD of the line current for this case is computed after calculating the harmonics values up to harmonic order of 40.

  The ratio of the THD is given in (3.41), and the value of the THD according to this expression is computed to be 28%.

- The size of the storage capacitor used in the experimental set-up for this case study is predetermined using the formula expressed in (3.32) which is presented in both approaches of analysis. The size of this capacitor is computed to be 217 μF.

- The design parameters illustrated in table 3.2, have been applied in the experimental set-up of the prototype circuit for this case study.

Table 3.2: Applied Design Parameters of the Case Study

Parameter	Value
V_{pk}	$12\sqrt{2}\ V$
V_{ref}	$6.5\ V$
f	$50\ H_z$
R	$12\ \Omega$

- The measured line current waveform is shown in figure 3.30. The three portions of the line current which mentioned in 3.2.2 are very obvious in this figure.

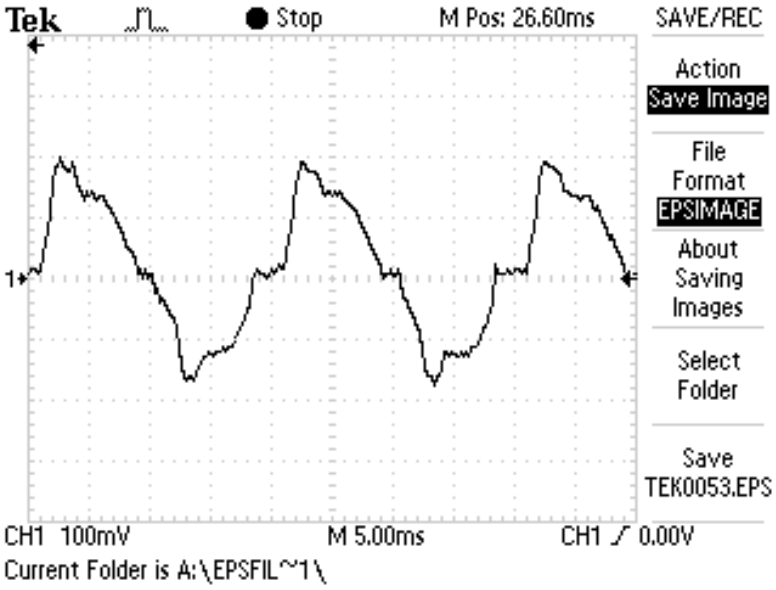


Figure 3.30: Experimental Line Current Waveform of the Proposed Rectifier

In figure 3.30, there is some asymmetry in the zero current periods. The reason for that is the leakage current which comes from the action of the bidirectional switch circuit. This is due to the delay between switching on the incoming device (side 1) and switching off the outgoing device (side 2). This leakage current would not makes any noticeable difference on the rest of the current portions.

- The practical output voltage and the supply voltage waveforms of this case are shown in figure 3.31, while the capacitor voltage and the supply voltage waveforms are shown in figure 3.32,

  From figures 3.31 and 3.32, it is clear that the capacitor voltage is synchronised with the output voltage. This is because the capacitor voltage is resulting from the same procedure of operating conditions and control scheme.

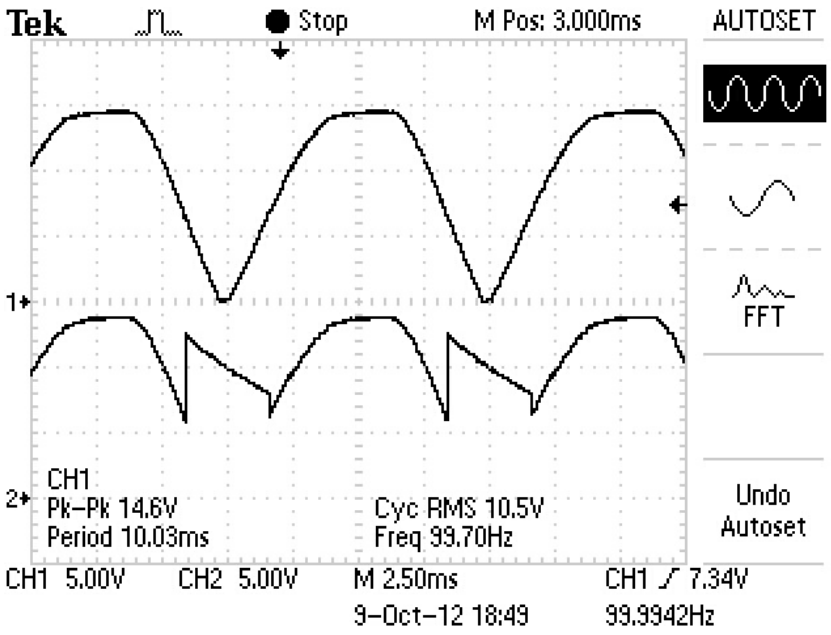


Figure 3.31: Experimental Supply Voltage and the Output Voltage Waveforms

From figure 3.32, it is noted that the capacitor voltage waveform consists of three periods. These three periods also came from the three operating conditions mentioned in 3.2.2 and they are fully compatible with them.

The first period is the charging mode or mode 1, where the capacitor is connected to the mains to charge and storing energy.

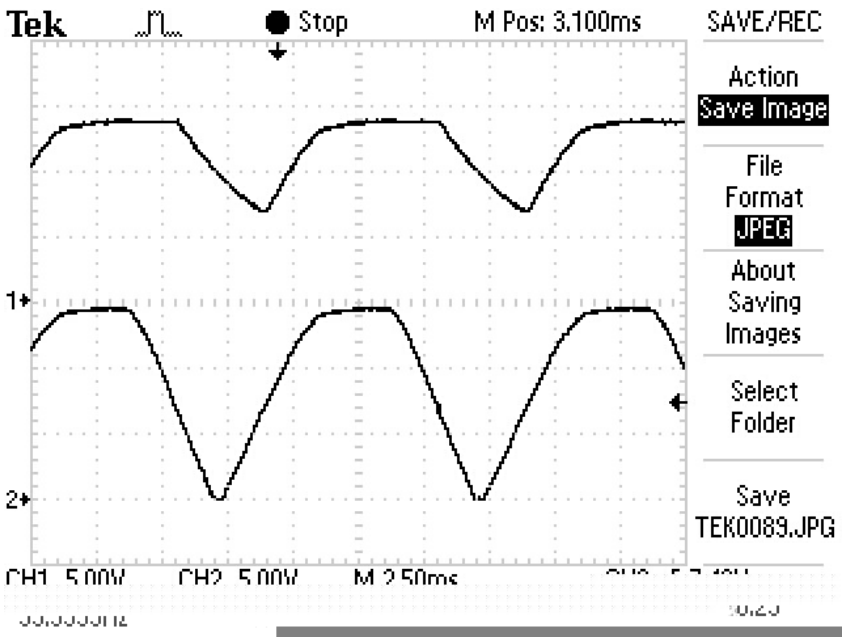


Figure 3.32: Experimental Capacitor Voltage and the Supply Voltage Waveforms

Keep charging mode or mode 2, that is the second period. Where the capacitor is disconnected from the mains and the load and it is fully charged.

The third period is the discharging mode or mode 3, where the capacitor is discharged into the load. The capacitor is the only energy source for the circuit in this mode as the supply voltage is completely disconnected by the diodes of the bridge rectifier and the load is fully served by the storage capacitor during the entire period of mode 3.

3.7 Results and Discussion

In order to clarify the performance of the proposed rectification technique, the system performance has been examined. A wide range of case studies with different sets of design parameters have been undertaken. They include the test of the prototype circuit and the AC side analysis of the test results obtained.

- The input power factor variation against the voltage ratio (V_{ref}/V_{pk}) with different loading conditions is shown in figure 3.33. It is clear that the proposed rectifier maintains nearly unity input power factor with up to 20% of this ratio.

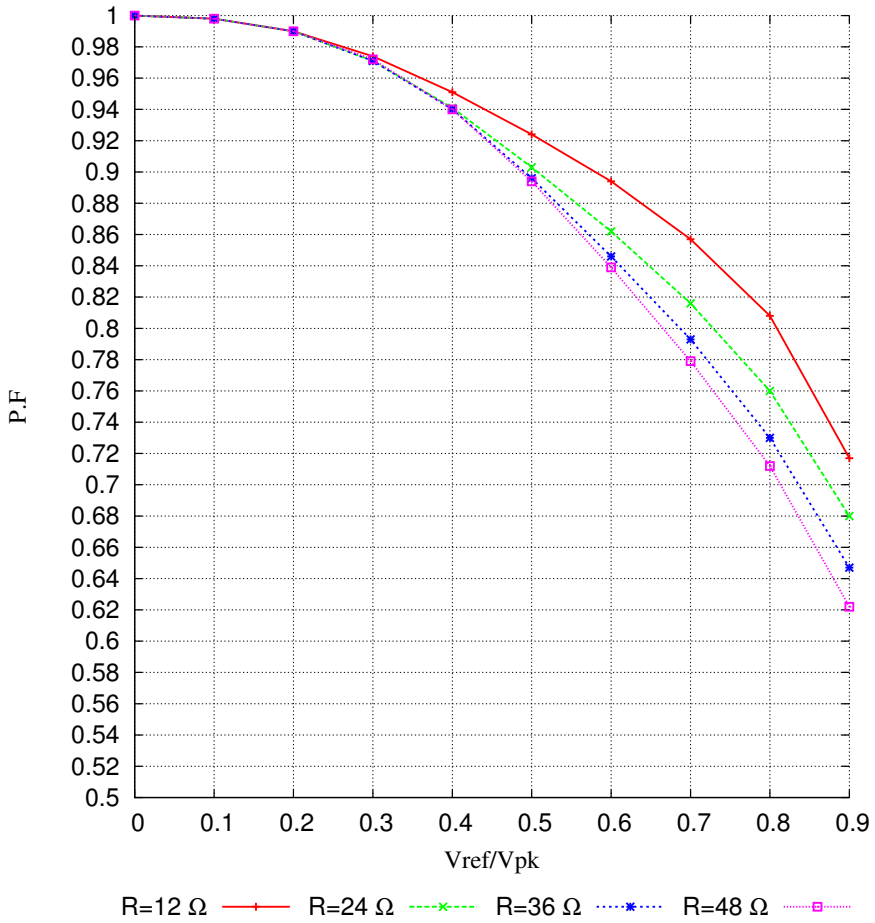


Figure 3.33: Power Factor vs the Voltage Ratio (V_{ref}/V_{pk})

- The required size of the DC side capacitor in relation to the voltage ratio (V_{ref}/V_{pk}) under different applied loads is shown in figure 3.34. The capacitor size is strongly depending on the voltage ratio and it can be as small as 10% of the size of the smoothing capacitor in the conventional system.

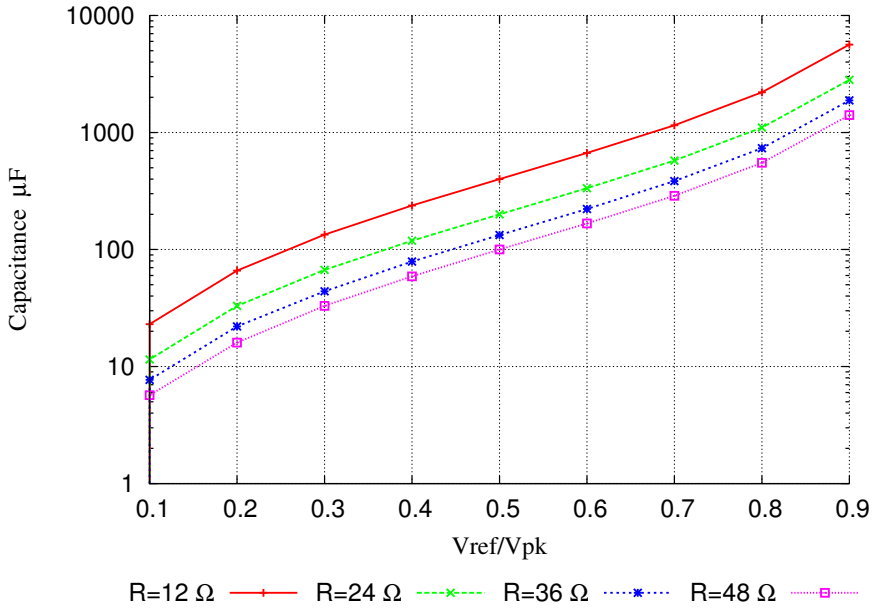


Figure 3.34: The DC Side Capacitor Size vs the Voltage Ratio (V_{ref}/V_{pk})

- The THD of the line current in relation to the voltage ratio (V_{ref}/V_{pk}) with variety of loads is shown in figure 3.35. The THD is nearly 3% at 10% and 10% at 20% of this ratio.

- For a certain loading condition (24Ω) the relationship between the required DC side capacitor and the voltage ratio with different supply frequencies is shown in figure 3.36. By increasing the supply frequency the required capacitor size becomes even more smaller. This feature can be very useful in higher frequencies applications such as the aircraft's power supplies when the weight and the size of the power supply is more important. The THD is not much affected by the frequency changing that is obvious in figure 3.37.

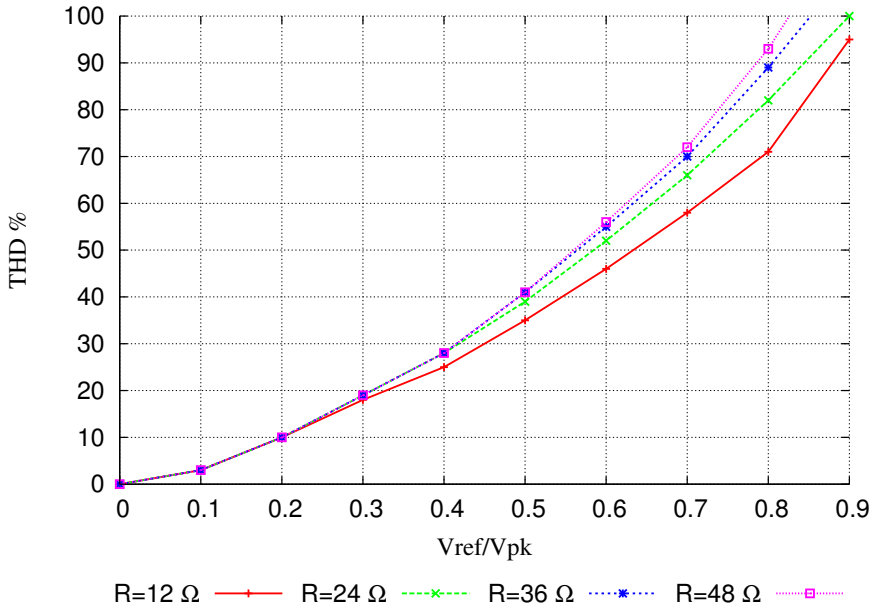


Figure 3.35: The THD vs the Voltage Ratio (V_{ref}/V_{pk})

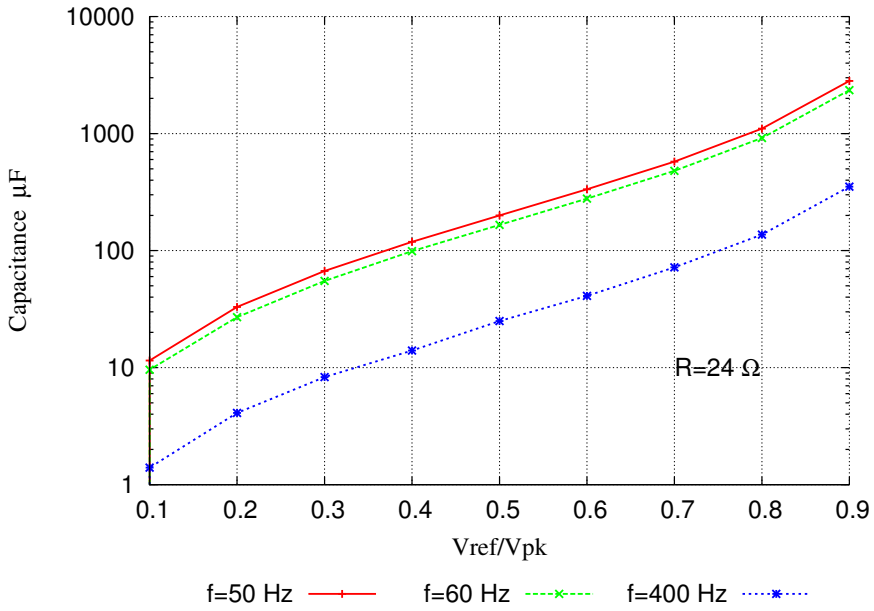


Figure 3.36: The DC Side Capacitor Size vs the Line Frequency

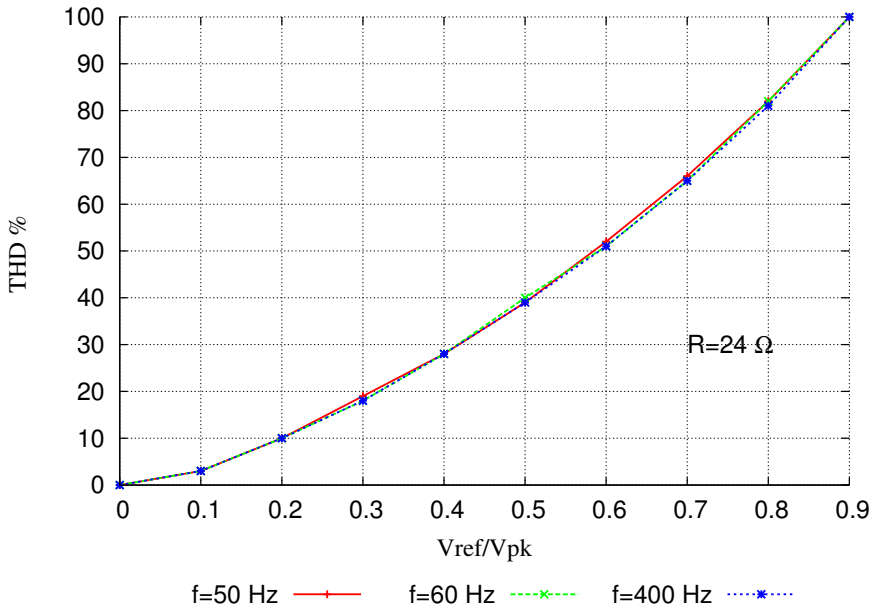


Figure 3.37: The THD vs the Line Frequency

3.8 Summary

This chapter can be summarized as follows:

- A novel single phase rectification technique with a new architecture and control strategy is proposed.
- The circuit configuration and the principles of operation of the proposed rectifier architecture is presented.
- The AC side analysis of the new rectifier is done using Woodward's notation with two approaches of analysis are included for this purpose (exact and approximate).
- The AC side analysis of the conventional single phase rectifier is also done using Woodward's notation.
- Woodwards notation applied to chopped waveforms is used to represent the line current for both rectifiers (proposed and the conventional) .
- The prototype circuits of the proposed and the conventional rectifiers have been designed, fabricated and tested.

- The prototype circuit of the control circuit of the new rectifier has been designed and fabricated.
- A wide range of case studies have been undertaken to prove the validity of the proposed technique and to clarify the performance of the new rectifier.
- A comparison between the performances of the conventional and the proposed rectifiers have been done by conducting two case studies under the same testing conditions.
- The results proved the ability of the new technique to maintain high input power factor. This is obtained with a reduced size capacitor in the DC side of the rectifier.
- The proposed technique provided a reduction in the size of the DC side capacitor. This reduction can be as low as less than 10% of the size of the typical smoothing capacitor in the conventional system.
- The harmonics analysis showed low harmonic content of the line current of the proposed technique with low THD.
- This work has been published in [83] and [84].

Chapter 4

A Novel Buck-Boost DC-DC Converter Using Close-Coupled Inductors and Passive Clamped Circuit

4.1 Introduction

A new step-up-down DC-DC converter architecture is proposed in this chapter. The new converter utilises the close inversely-coupled inductors topology in both its conversion stages (buck and boost). This converter aims to reduce the switching noise that usually accompanies the conventional buck and boost converter circuits and causes a considerable switching losses that leads to poor power conversion efficiency. Switching noise can be reduced by reducing the back e.m.f induced in the main inductor. The new converter architecture can achieve a high power conversion efficiency for this kind of power converters which dealing with a wide range of supply voltages and serves a wide variety of applications.

4.2 The Proposed Buck-Boost Converter

4.2.1 Circuit Configuration

The circuit configuration of the proposed buck-boost converter is depicted in figure 4.1.

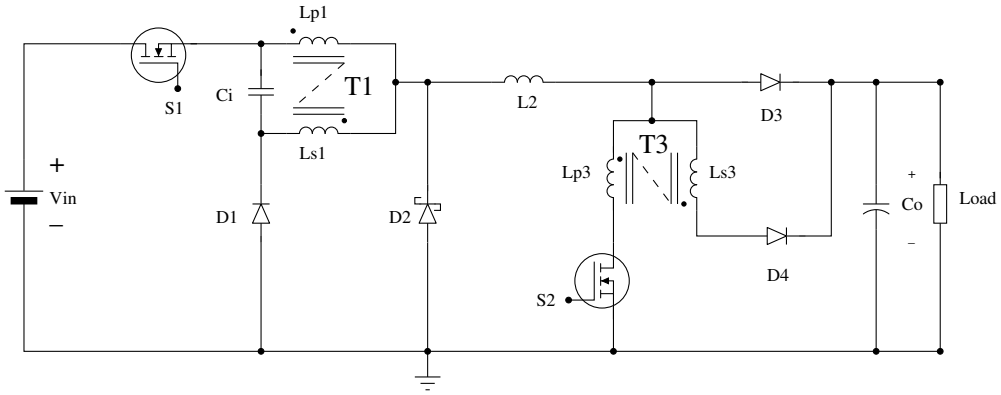


Figure 4.1: Circuit Configuration of the Proposed Buck-Boost DC-DC Converter

The entire circuit can be represented as two phases or stages. The first phase is the buck stage which consists of the power switch S_1, the inductors L_{p1}, L_{s1} which they are inversely coupled inductors on the same ferrite core (primary and secondary windings of transformer T_1), input capacitor C_i, diodes D_1, D_2 and the main inductor L_2. The boost phase follows the buck stage and therefore the two stages share the main inductors L_2 and the diode D_2. The rest of the boost stage are the inductors L_{p3}, L_{s3} which they are also inversely coupled on the same core (primary and secondary windings of transformer T_3), power switch S_2, diodes D_3, D_4 and the output filter capacitor C_o.

4.2.2 Principles of Operation

According to the applied sets of the duty cycles for the power switches S_1, S_2, the proposed converter can work as just a buck, boost or buck-boost converter.

The operating principles for buck-boost operation in CCM and steady state conditions are only discussed in this section. In order to clearly illustrate the principles of operation for the proposed converter, the following assumption have been made:

- The parasitic resistance and capacitance of all diodes and power switches are neglected.

- The parasitic resistance and capacitance of all passive components are neglected.
- The forward voltage drop of all diodes are assumed to be zero.
- The turn ratio n of the coupled inductors windings (transformers T_1, T_3) is unity.
- The magnetic field in the main inductor does not saturate.
- The magnetising inductance of the coupled inductors for both transformers have been integrated to the primary winding.

The circuit analysis can be simplified by representing the entire converter circuit as two sub-circuits or two stages. The first stage is the buck stage, the second is the boost stage. The circuits for buck and boost stages are shown in figures 4.2, 4.3 respectively.

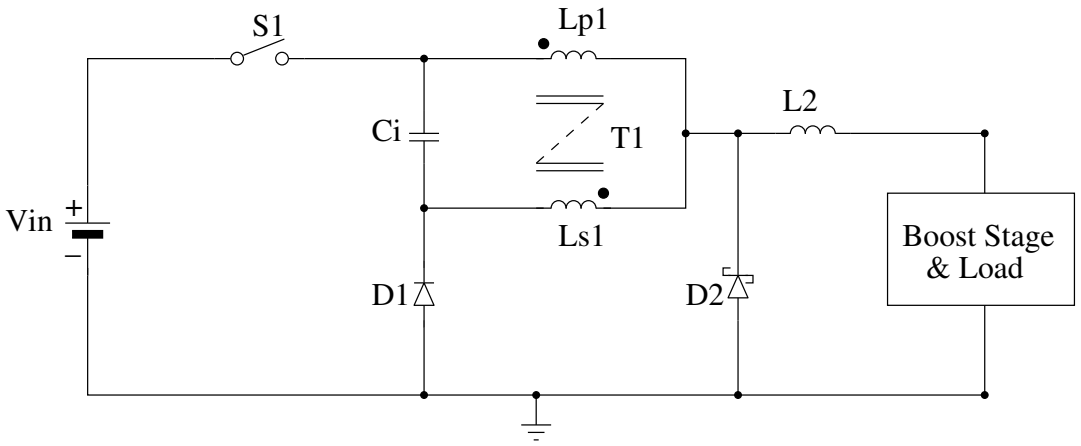


Figure 4.2: Buck Stage of the Proposed Buck-Boost DC-DC Converter

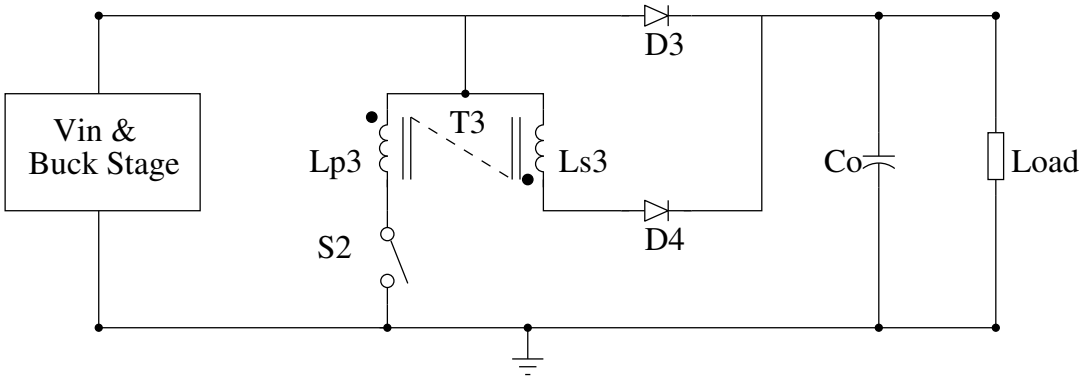


Figure 4.3: Boost Stage of the Proposed Buck-Boost DC-DC Converter

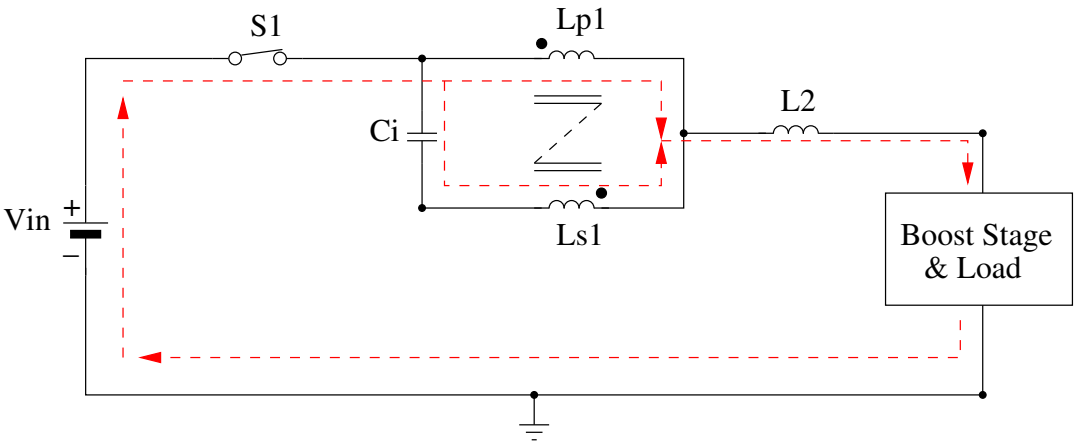


Figure 4.4: On State of Buck Stage

Buck stage : The buck stage is shown in figure 4.2, in this stage there are two states:

- On state, [S_1 on, D_1, D_2 off]: When the switch S_1 is turned on, the energy starts flowing through the primary winding L_{p1}, in the meanwhile the capacitor Ci provides a parallel path for energy to flow into the secondary winding L_{s1}. Both energy paths are merged together in the common point of the coupled inductors just at the main inductor L_2. As a consequences both diodes D_1 and D_2 are now off. Some energy is stored in both sides of the coupled inductors (the primary and the secondary windings of the transformer T_1) and the capacitor Ci. The equivalent circuit of this case with all currents paths is shown in figure 4.4. The current of the main inductor L_2 is the sum of the both sides of the coupled inductors currents.
- Off state, [S_1 off, D_1, D_2 on]: Once the switch S_1 is going to switch off, the energy releasing process is started. The capacitor Ci starts discharging its energy instantaneously to the primary winding L_{p1}. The secondary winding L_{s1} releases its energy to the capacitor Ci, whilst the primary winding releases some of the stored energy to the main inductor L_2. The time constant of discharging the capacitor is crucial to avoid any discontinuity of the current flowing to the primary winding L_{p1}. The capacitor in this case is much faster than any particular diode available to overcome the problem of delay in

conduction due to the required conduction time by any used diode. Once the diode D_1 starts to conduct it will provide with the capacitor Ci an additional path for current to flow alongside with the current path of schottky diode D_2. The equivalent circuit of this case with all currents paths is shown in figure 4.5.

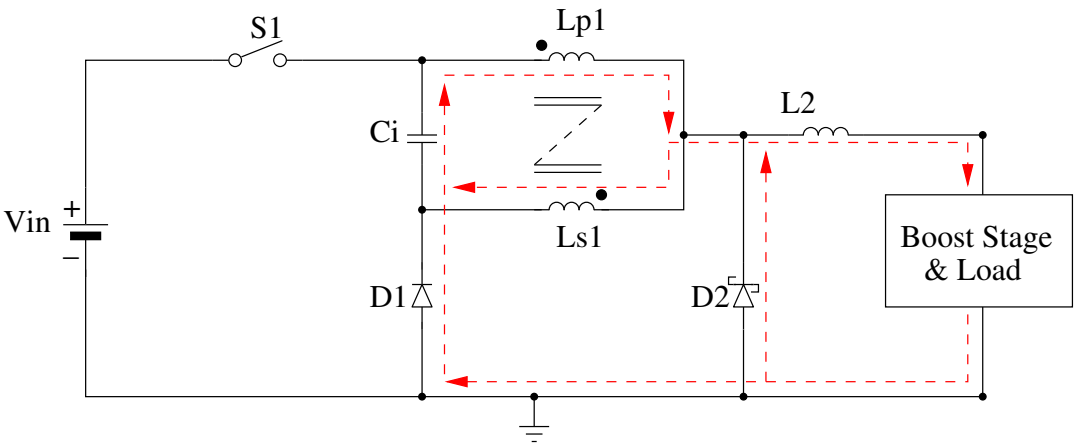


Figure 4.5: Off State of Buck Stage

The current of the main inductor L_2 is the sum of both diodes currents D_1 and D_2. This arrangement ensures a continuous flow of current in the coupled inductors and the main inductor even with off time of the switch S_1. As a results of this configuration, there is a small effect of the back e.m.f induced in the couple inductors and the main inductor L_2 of the buck stage. All actual currents waveforms are presented in 4.5.

Boost stage : The boost stage is shown in figure 4.3. The output voltage and current of the buck stage now becomes the source of this stage. This stage also has two states:

– On state, [S_2, D_4 on, D_3 off]: When the switch S_2 is turned on, the main current which is the output current of the buck stage will split into two. This is due to the effect of the unity turn ratio transformer T_3 (the coupled inductors L_{p3} and L_{s3}). The currents in both the primary winding L_{p3} and the secondary winding L_{s3} have the same magnitude. Once the voltage on

the anode of the diode D_4 is equal to the output voltage, this diode becomes forwards biased. The secondary winding of the transformer T_3 now provides a path for energy to flow into the load side through diode D_4. This results in diode D_3 being turned off as the output voltage is now applied on its cathode. The equivalent circuit of this case with all currents paths is clearly illustrated in figure 4.6.

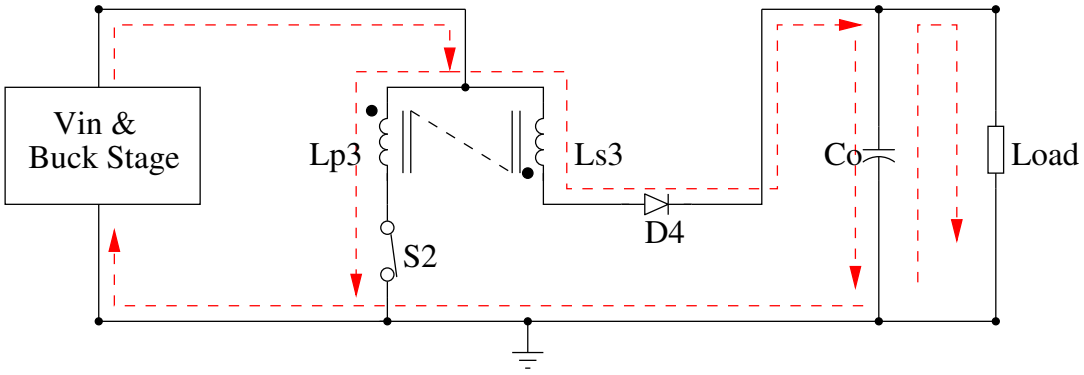


Figure 4.6: On State of Boost Stage

– Off state, [S_2, D_4 off, D_3 on]:

When the switch S_2 is turned off, the diode D_3 becomes forwards biased once the voltage on its anode is equal to the output voltage. The main current then goes directly to the load side through diode D_3. The output voltage is now applied on the cathode of diode D_4 which results in diode D_4 being turned off. The equivalent circuit of this case with all currents paths is shown in figure 4.7.

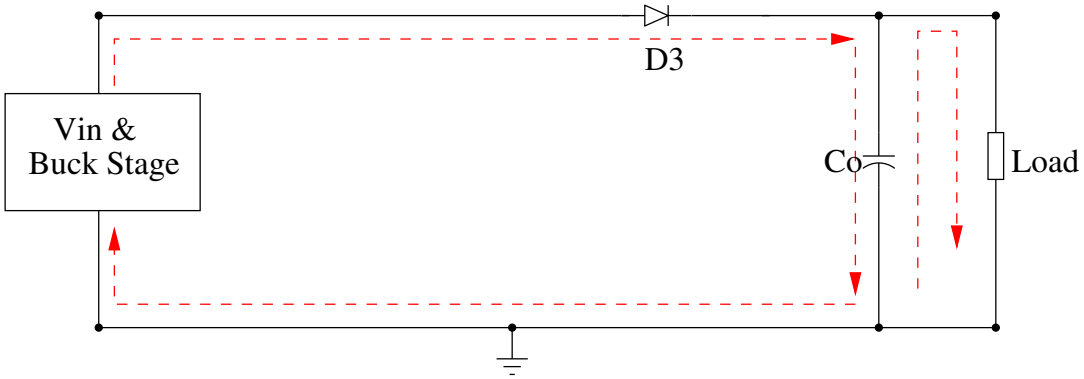


Figure 4.7: Off State of Boost Stage

4.3 Transfer Function

The proposed converter can work as just a buck, boost, or buck-boost converter according to the applied set of duty cycles for the switches S_1 and S_2. The transfer function of the buck-boost converter at steady state condition and CCM of operation is presented here. It can be derived by getting the rate of change of the converter current in four different cases. The converter current means the current flowing in the main inductor i_{L_2}.

These cases represent the logical permutations of both power switches S_1 and S_2. By returning to the full circuit diagram of the proposed converter in figure 4.1, these four states can be described as follows:

Starting with the definitions of the key variables in this derivation:

i_{max} is the maximum value of i_{L_2},

i_{min} is the minimum value of i_{L_2},

α, β are intermediate values of i_{L_2},

$\alpha > i_{min}$, $\beta < i_{max}$,

t_1 is the time duration of case 1,

t_2 is the time duration of case 2,

t_3 is the time duration of case 3,

t_4 is the time duration of case 4,

$t_1 + t_2 + t_3 + t_4 = T$,

T is the full time period of one frequency cycle.

A schematic diagram of the inductor current during one complete cycle of switching frequency and indicating all time durations of the four cases with their current gradients (slopes) and amplitudes are shown in figure 4.8.

- Case 1: [S_1: On, S_2: Off, $0 < t \leq t_1$], When the switch S_1 is turned on during this period, the supply voltage is connected to the buck stage. Diodes D_1, D_2 and D_4 are all being turned off, while diode D_3 is being forwards biased. The input current here is equal to the output current.

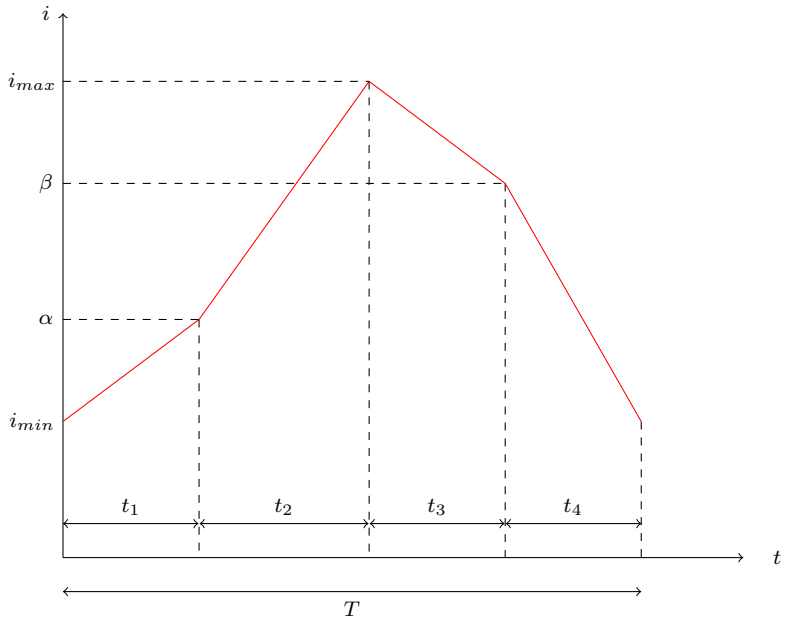


Figure 4.8: Inductor Current Waveform

$$i_{in} = i_{L_2} \tag{4.1}$$

$$V_{L2} = V_{in} - V_{out} = L_2 \frac{di_{in}}{dt} \tag{4.2}$$

$$L_2 \frac{di_{in}}{dt} = L_2 \frac{(\alpha - i_{min})}{t_1} \tag{4.3}$$

$$V_{in} - V_{out} = L_2 \frac{(\alpha - i_{min})}{t_1} \tag{4.4}$$

Where, i_{in} is the input current, V_{in} is the supply voltage, V_{out} is the output voltage, V_{L2} is the voltage across the main inductor L_2.

- Case 2: [S_1: On, S_2: On, $t_1 < t \leq t_2$], When switches S_1 and S_2 are both turned on during this period, both the supply voltage and the boost stage are being connected. Due to the effect of the transformer T_3, the input current to the boost stage is divided into two currents with the same magnitude.

The diode D_4 is being forwards biased, while diodes D_1, D_2 and D_3 is are all being turned off during the period of case 2.

$$i_{in} = i_{L_2} \tag{4.5}$$

$$V_{L2} = V_{in} - \frac{V_{out}}{2} = L_2 \frac{di_{in}}{dt} \tag{4.6}$$

$$L_2 \frac{di_{in}}{dt} = L_2 \frac{(i_{max} - \alpha)}{t_2} \tag{4.7}$$

$$V_{in} - \frac{V_{out}}{2} = L_2 \frac{(i_{max} - \alpha)}{t_2} \tag{4.8}$$

- Case 3: [S_1: Off, S_2: On, $t_2 < t \leq t_3$], When the switch S_1 is turned off during this period, the supply voltage is being disconnected from the the buck stage, while diodes D_1, D_2 are being forwards biased. The boost stage here is still connected as the status of switch S_2 would not change during this period. Diodes D_3 and D_4 are also still unchanged during case 3.

$$i_{in} = i_{L_2} \tag{4.9}$$

$$V_{L2} = \frac{V_{out}}{2} = L_2 \frac{di_{in}}{dt} \tag{4.10}$$

$$L_2 \frac{di_{in}}{dt} = L_2 \frac{(i_{max} - \beta)}{t_3} \tag{4.11}$$

$$\frac{V_{out}}{2} = L_2 \frac{(i_{max} - \beta)}{t_3} \tag{4.12}$$

- Case 4: [S_1: Off, S_2 : Off, $t_3 < t \leq t_4$], During this case, both the supply voltage and the boost stage are being disconnected. Diodes D_1, D_2 and D_3 are all being forwards biased, while diode D_4 is being reverse biased. The input current here is equal to the output current.

$$i_{in} = i_{L_2} \tag{4.13}$$

$$V_{L2} = V_{out} = L_2 \ \frac{di_{in}}{dt} \tag{4.14}$$

$$L_2 \ \frac{di_{in}}{dt} = L_2 \ \frac{(\beta - i_{min})}{t_4} \tag{4.15}$$

$$V_{out} = L_2 \ \frac{(\beta - i_{min})}{t_4} \tag{4.16}$$

At steady state condition with CCM of operation, the rise in current during case 1 and case 2 should equal the fall in current during case 3 and case 4.

$$[(\alpha - i_{min}) + (i_{max} - \alpha)] \ L_2 = [(i_{max} - \beta) + (\beta - i_{min})] \ L_2 \tag{4.17}$$

Dividing both sides of (4.17) by L_2 and by substitution in (4.4), (4.8), (4.12) and (4.16), the equation of (4.17) can be formulated as follow

$$\left[(V_{in} - V_{out}) \ t_1 + (V_{in} - \frac{V_{out}}{2}) \ t_2\right] = \left[(\frac{V_{out}}{2}) \ t_3 + (V_{out}) \ t_4\right] \tag{4.18}$$

Then,

$$(t_1 + t_2) \ V_{in} = \left[(t_1 + t_4) + \frac{1}{2}(t_2 + t_3)\right] \ V_{out} \tag{4.19}$$

Defining:

D_1, D_2 are the duty cycles of switches S_1, S_2 respectively, D_1, D_2 can be expressed as below

$$D_1 = \frac{(t_1 + t_2)}{(t_1 + t_2 + t_3 + t_4)} \tag{4.20}$$

$$D_2 = \frac{(t_2 + t_3)}{(t_1 + t_2 + t_3 + t_4)} \tag{4.21}$$

And,

$$(1 - D_2) = \frac{(t_1 + t_4)}{(t_1 + t_2 + t_3 + t_4)} \tag{4.22}$$

By Substitution of (4.20), (4.21) and (4.22) in (4.19)

$$D_1 \; V_{in} = (1 - D_2 + \frac{1}{2} D_2) \; V_{out} \tag{4.23}$$

The overall duty cycle of the proposed buck-boost converter can be expressed as in (4.24).

$$\frac{V_{out}}{V_{in}} = \frac{D_1}{(1 - \frac{D_2}{2})} \tag{4.24}$$

4.4 Experimental Set-up

The prototype circuit of the new converter has been fabricated and tested. The layout of the prototype circuit of the proposed buck-boost DC-DC converter is shown in figure D.1 in appendix D. A single control circuit has been used to generate two different control signals which are used to fire two MOSFET driver circuits. The Micro-controller (STM32F4 High-Performance Discovery Board) is used for this purpose. Two N-channel MOSFETs have been used as switching devices S_1 and S_2 with two high-side MOSFET drivers to drive them. The function of the control circuit is to generate different sets of the duty cycles D_1 and D_2 for the switches S_1 and S_2 respectively. The sets started from 5% for both duty cycles and end up with 90% for the buck and 80% for the boost, step-up by 5% or 10%. A full range of the boost duty cycle (from 5% up to 80%) for each step of top-up for the buck duty cycle have been undertaken. This is to ensure a comprehensive understanding the performance of the proposed converter.

The parameters values of the converter circuit which are used in this experimental set-up are presented in table 4.1.

Table 4.1: Experimental Set-up Parameters

Parameter	Value
L_{p1}, L_{s1}	$98\mu H$
L_{p3}, L_{s3}	$234\mu H$
L_2	$3.54mH$
C_i	$4.8\mu F$
C_o	$112\mu F$

4.5 Experimental Results of Case Studies

To prove the validity of the proposed converter architecture a range of case studies have been undertaken. The practical results of the buck-boost operation only is presented in this section. In order to clarify the actual current waveforms of the new converter and to verify the principles of operation mentioned in 4.2.2, four case studies are presented in this section.

The applied supply voltage, duty cycles of switches S_1, S_2 and the connected loads for all four cases are presented in table 4.2.

The same parameters values of the the converter circuit presented in table 4.1 have been used in all case studies.

Table 4.2: Cases Studies Testing Conditions

Case Study	V_{in}	R_{load}	D_1	D_2
1	$14V$	11Ω	50%	50%
2	$14V$	11Ω	70%	70%
3	$14V$	22Ω	50%	50%
4	$14V$	22Ω	70%	70%

In order to facilitate the follow up of energy flow process and currents distribution in the circuit, full converter circuit diagram with all currents paths (with red arrows) are shown in figure 4.9.

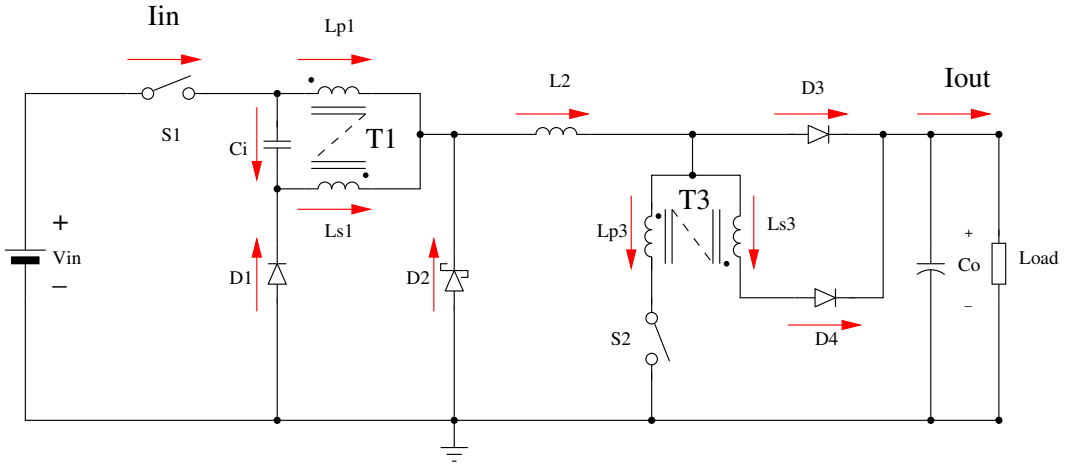


Figure 4.9: Circuit Configuration of the Proposed Converter with All Currents Paths

4.5.1 Case Study 1

The experimental current waveforms of the buck stage are shown in figures 4.10, 4.11 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure 4.12, while the current waveforms of the boost stage and the output current are all shown in figure 4.13. The measured efficiency for this particular case is 95.6%.

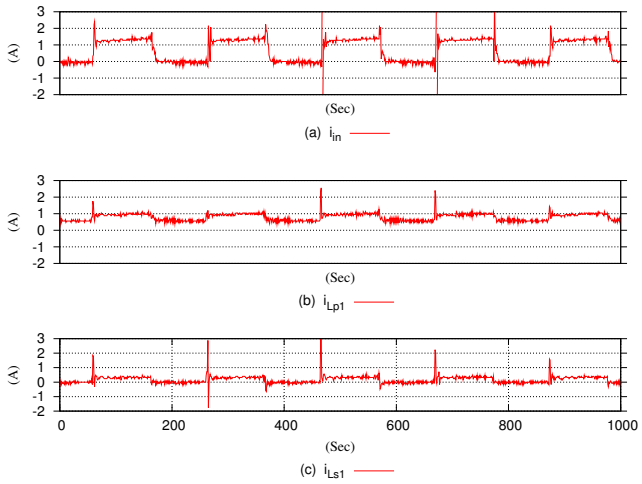


Figure 4.10: Experimental Current Waveforms of Case Study 1: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

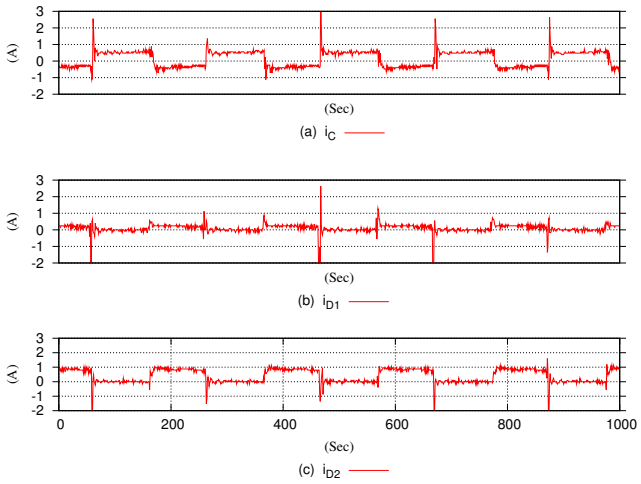


Figure 4.11: Experimental Current Waveforms of Case Study 1: (a) current of capacitor C_i, (b) current of diode D_1, (c) current of diode D_2,

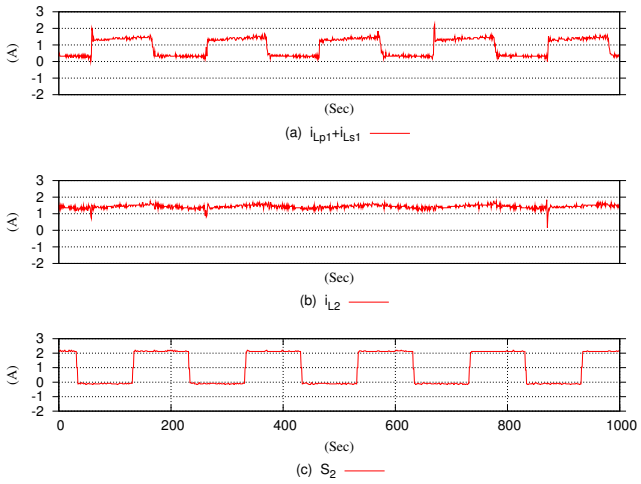


Figure 4.12: Experimental Current Waveforms of Case Study 1: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

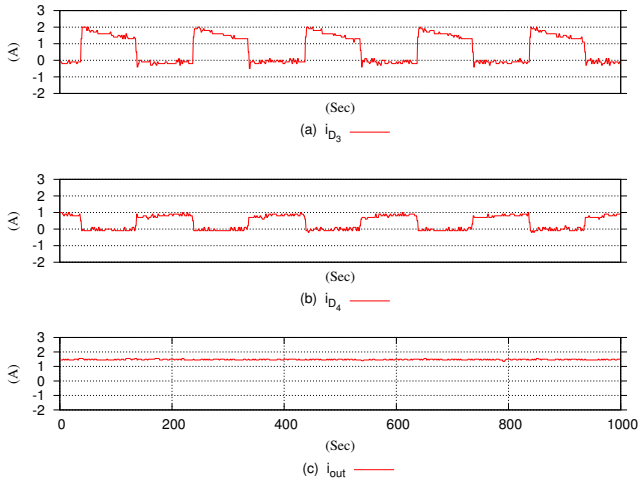


Figure 4.13: Experimental Current Waveforms of Case Study 1: (a) current of diode D_3, (b) current of diode D_4, (c) output current i_{out}

4.5.2 Case Study 2

The experimental current waveforms of the buck stage are shown in figures 4.14, 4.15 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure 4.16, while the current waveforms of the boost stage and the output current are all shown in figure 4.17. The measured efficiency for this particular case is 95.3%.

The other two case studies are presented in appendix E.

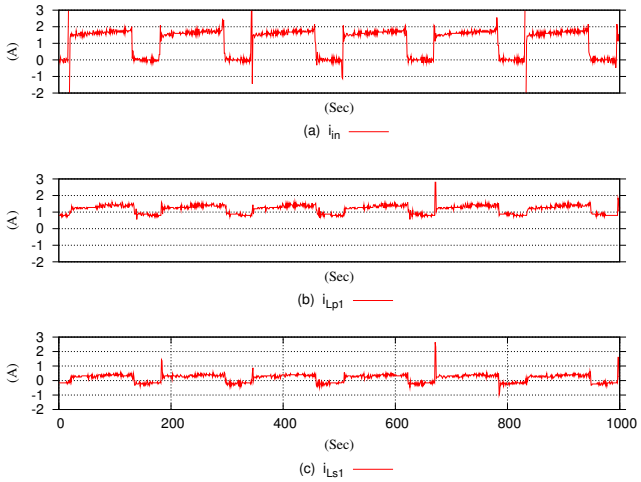


Figure 4.14: Experimental Current Waveforms of Case Study 2: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

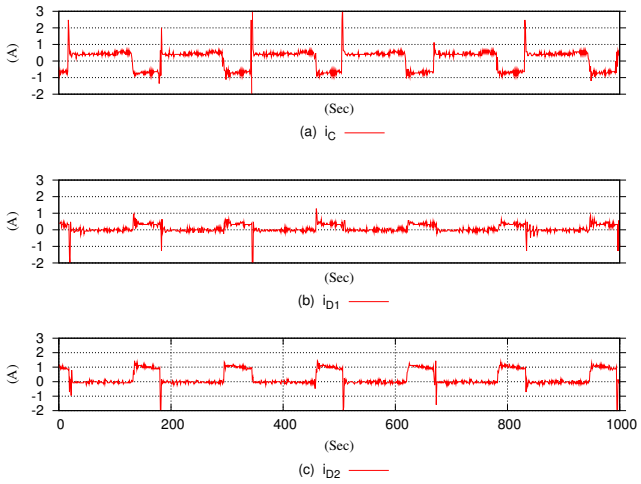


Figure 4.15: Experimental Current Waveforms of Case Study 2: (a) current of capacitor C_i, (b) current of diode D_1, (c) current of diode D_2,

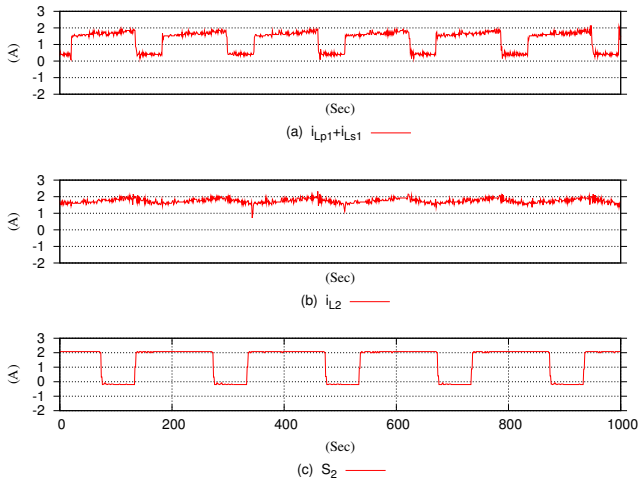


Figure 4.16: Experimental Current Waveforms of Case Study 2: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

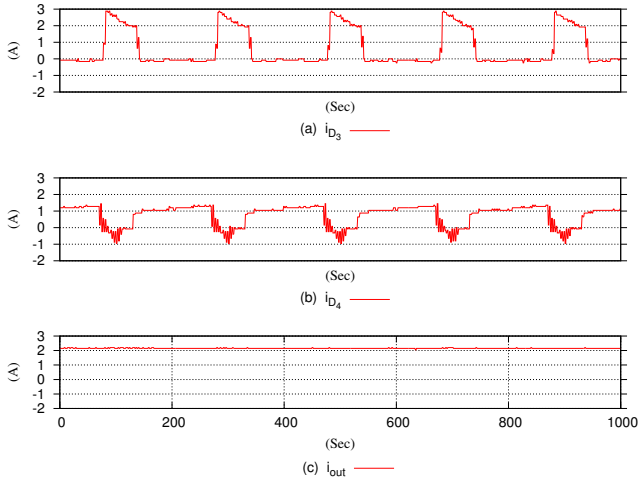


Figure 4.17: Experimental Current Waveforms of Case Study 2: (a) current of diode D_3, (b) current of diode D_4, (c) output current i_{out}

4.6 Simulated Results of Case Studies

A simulation model for the circuit configuration of the proposed buck-boost DC-DC converter has been implemented. The layout of the simulation model of this converter using LT spice IV 4.22 is shown in figure D.2 in appendix D. The same design parameters of the prototype circuit mentioned in table 4.1 have been used in this model. In order to confirm the practical results of the case studies presented in 4.5, the simulation model of the converter has been examined with the same case studies presented in table 4.2. Testing conditions mentioned in table 4.2 have been also applied during the simulation of this model. The only difference between the practical and the simulated measures is the absence of current sensors in this model. Current sensors are necessary in the prototype circuit in order to capture the current waveforms. This results in a slim margin between the practical and the simulated results. From the results of the simulated case studies shown below, it is clear that the simulated results are in accordance with practical results and highly compatible.

4.6.1 Case Study 1

The simulated current waveforms of the buck stage are shown in figures 4.18, 4.19 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure 4.20, while the current waveforms of the boost stage and the output current are all shown in figure 4.21.

4.6.2 Case Study 2

The simulated current waveforms of the buck stage are shown in figures 4.22, 4.23 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure 4.24, while the current waveforms of the boost stage and the output current are all shown in figure 4.25.

The other two case studies are presented in appendix F.

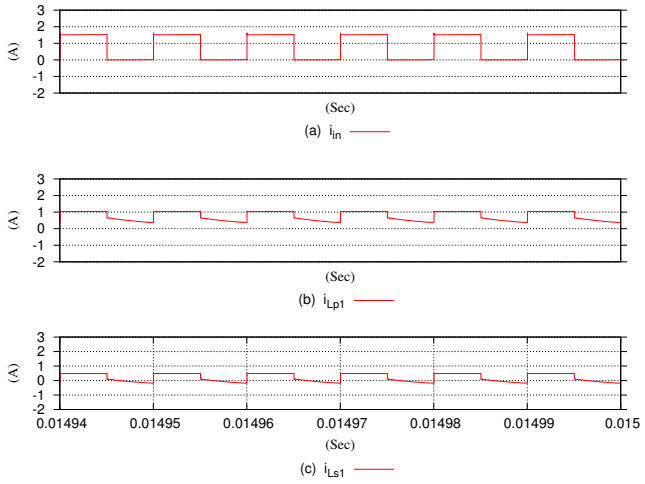


Figure 4.18: Simulated Current Waveforms of Case Study 1: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

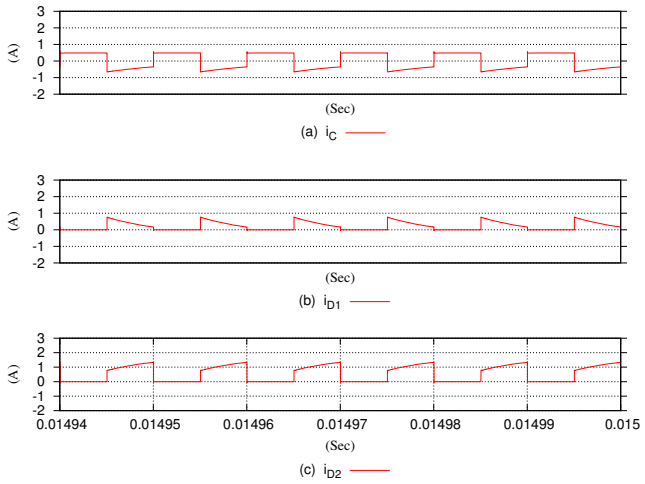


Figure 4.19: Simulated Current Waveforms of Case Study 1: (a) current of capacitor C_i, (b) current of diode D_1, (c) current of diode D_2,

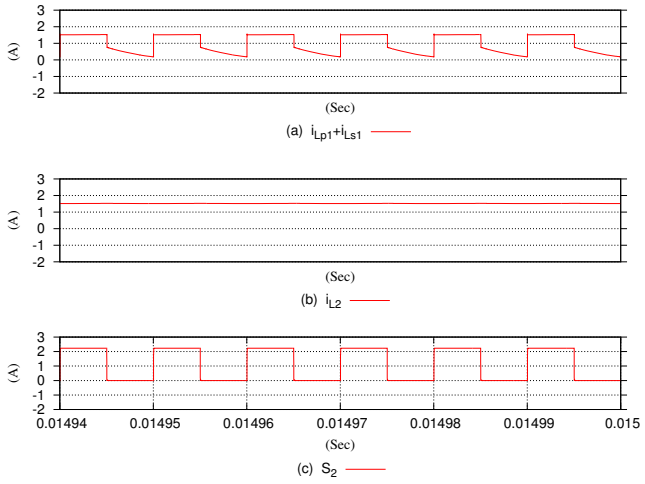


Figure 4.20: Simulated Current Waveforms of Case Study 1: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

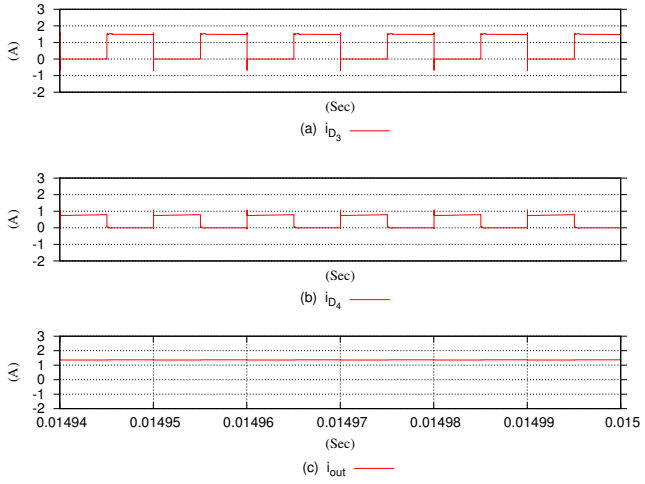


Figure 4.21: Simulated Current Waveforms of Case Study 1: (a) current of diode D_3, (b) current of diode D_4, (c) output current i_{out}

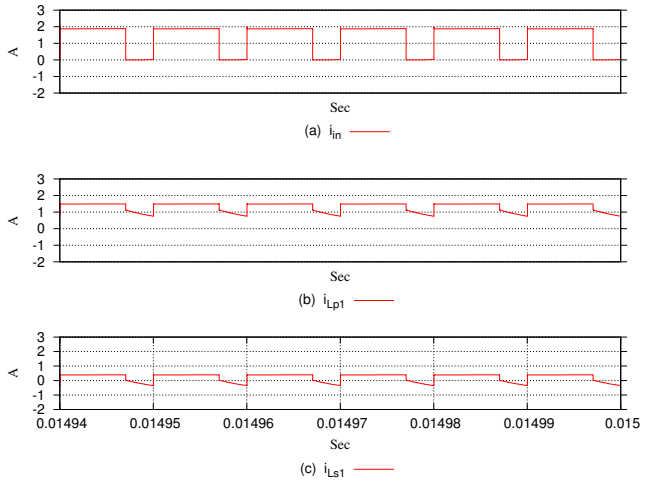


Figure 4.22: Simulated Current Waveforms of Case Study 2: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

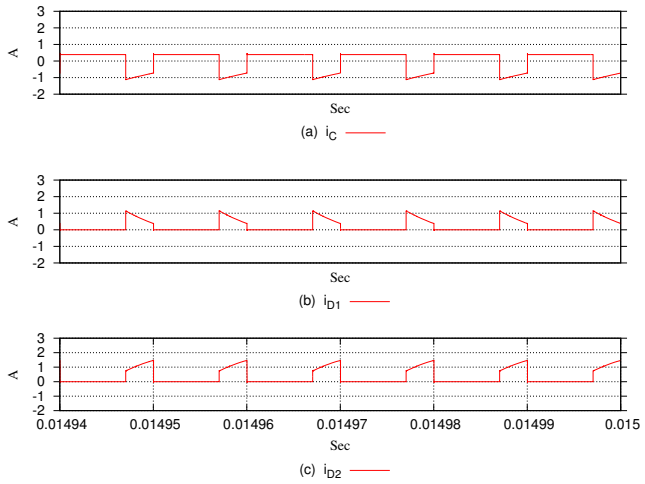


Figure 4.23: Simulated Current Waveforms of Case Study 2: (a) current of capacitor C_i, (b) current of diode D_1, (c) current of diode D_2,

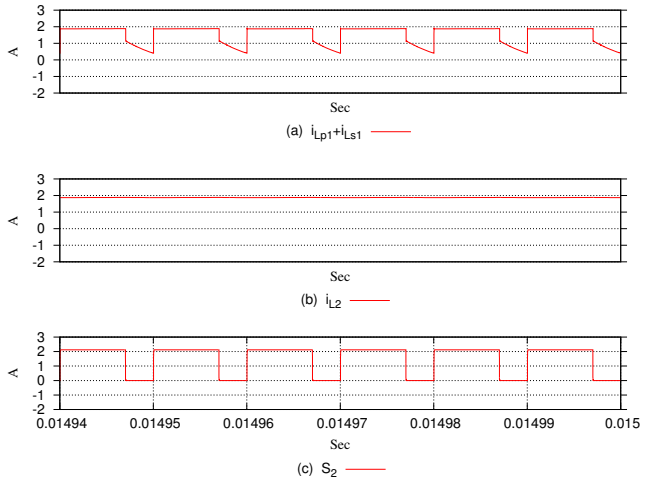


Figure 4.24: Simulated Current Waveforms of Case Study 2: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

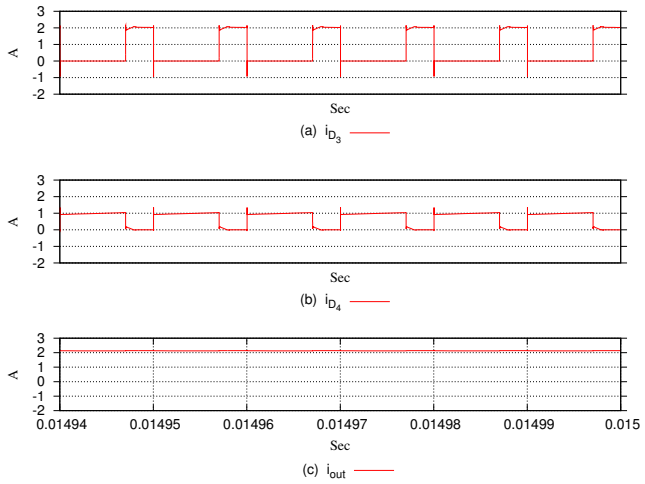


Figure 4.25: Simulated Current Waveforms of Case Study 2: (a) current of diode D_3, (b) current of diode D_4, (c) output current i_{out}

4.7 Experimental Results and Discussion

In order to clarify the performance of the proposed converter, the system performance has been examined. The practical results of a range of cases (using 7 V input and a 22Ω load, 14 V input and a 44Ω load, and 20 V input with 66Ω load) at 100 kHz switching frequency is presented in figure 4.26.

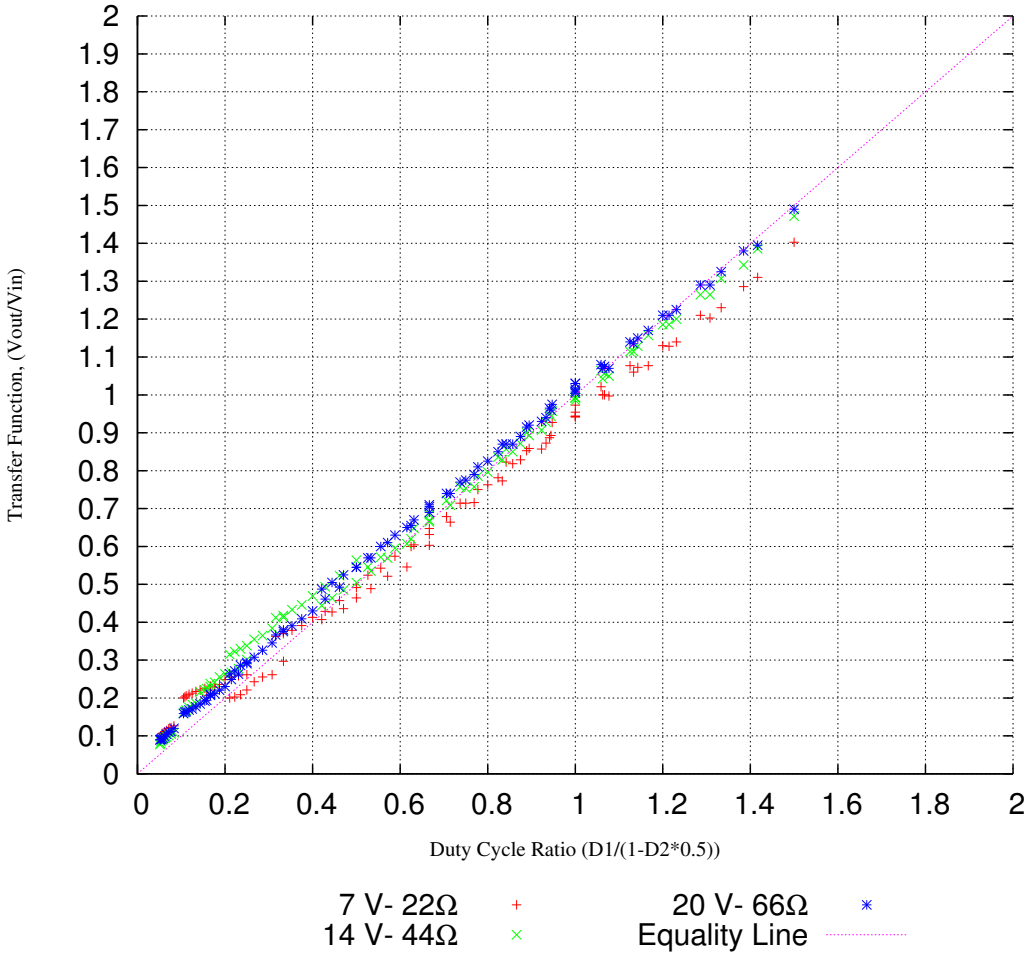


Figure 4.26: Experimental Results of a Range of Case Studies

A full range of duty cycle sets for switches S_1 and S_2 as mentioned in 4.4 has been used for each of these cases. The results confirm the validity of (4.24). The y axis represents the ratio $y = \frac{V_{out}}{V_{in}}$, whereas the x axis is the duty cycle. For clarity the line $y = x$, which represent (4.24) is also provided.

Figure 4.26 showed clearly the linearity performance of the proposed system and how does it work with a variety of duty cycles and loading conditions. Also it showed there is

very small deviation in some test points from the equality line of the analytical derived duty cycle. This deviation being more noticeable when the duty cycle of the boost switch S_2 skips the value of 50%. The results verified the compatibility between the analytical and practical results of the proposed converter. It also can be considered as a good indicator for the slim rate of noise and losses in this circuit.

The efficiency measurements for a selected case study from the above three cases (using 20 V input and a 66Ω load) have been done. The measured efficiency curve for this case under various output power is shown in figure 4.27. Figure 4.27 showed the measured efficiency points and the best fit curve that connecting all measured points for this case study.

Although, the efficiency curve showed high efficiency performance is achieved with the new converter architecture, further investigations and analysis to determine the design parameters of this circuit with a better components choice can result in making this circuit to work more efficiently.

4.8 The Transient Response

Figures 4.28, 4.29, are the turn On and turn Off transient response of the proposed converter respectively. The same parameters values of table 4.1 have been used in this test points. The input voltage of $20V$ and a load of 66Ω at 100 kHz switching frequency with 30% duty cycle for both switches have been applied. It is clear that this topology has little or no transient overshoot even while switching at constant duty cycles and at a fixed switching frequency.

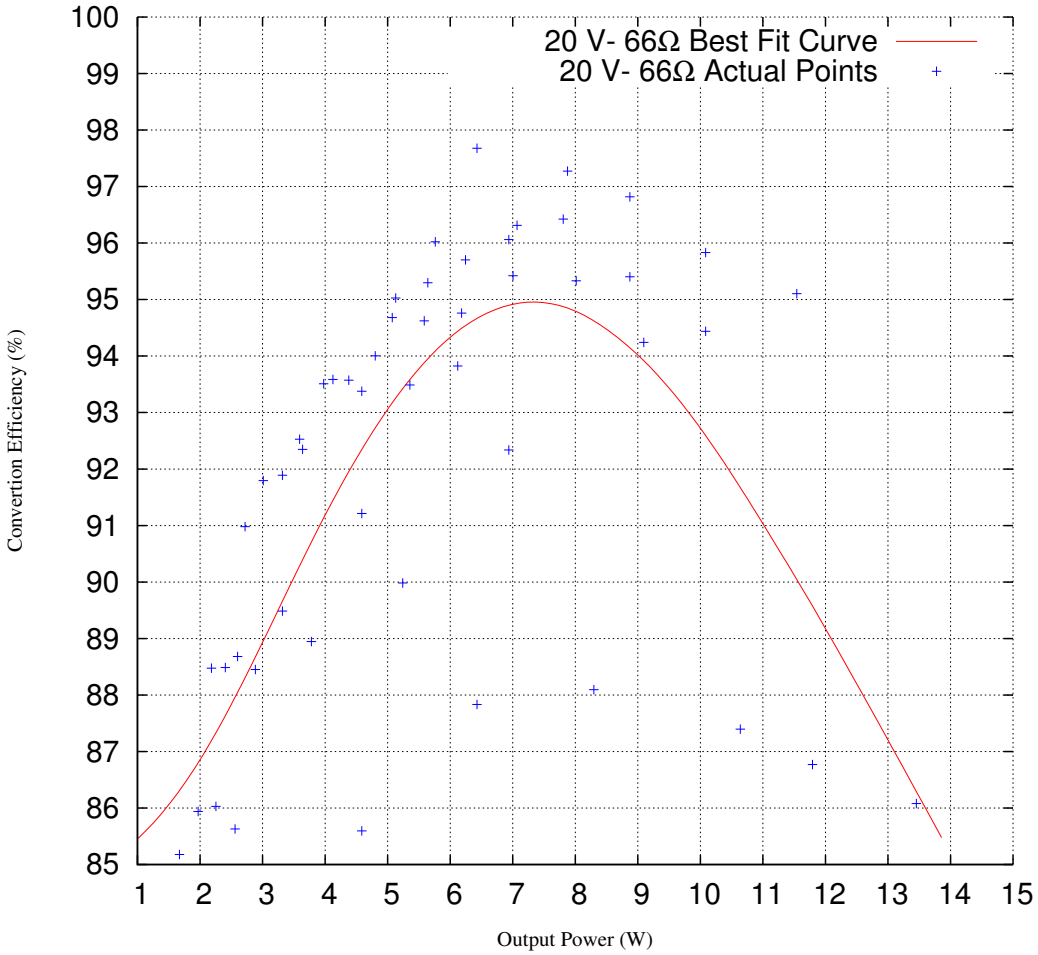


Figure 4.27: Measured Efficiency Versus Output Power

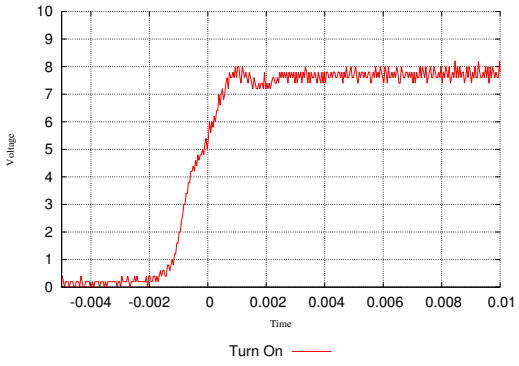


Figure 4.28: Turn On Transient

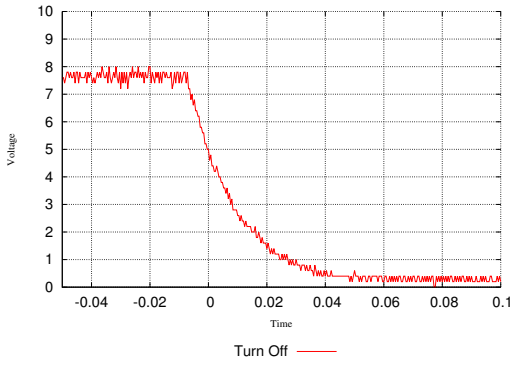


Figure 4.29: Turn Off Transient

4.9 Summary

This chapter can be summarized as follows:

- A novel buck-boost DC-DC converter architecture with its transfer function is presented in this chapter.
- This converter utilises the close inversely-coupled inductors topology in both its conversion stages (buck and boost).
- In buck stage, this topology with additional passive component (capacitor) connected across the free terminals of coupled inductors and in series with a normal diode can work as a passive clamped circuit.
- The function of the passive clamped circuit is to recycle the leakage energies of the coupled inductors which results in an efficiency improvement of the power converter. Also, this circuit is used to clamp the large voltage spikes (due to the impedance buffer provided by the coupled inductors) in order to limit the voltage stress on the main switch S_1.
- This configuration ensures a continuous flow of current through the buck stage even with the off time of the buck switch S_1. This results in a reduction in the back e.m.f induced in the main inductor and thus reducing the switching noise.
- The close coupled inductors arrangement also been utilised in the boost stage to ensure a continuous output current by providing an alternative (parallel) path for energy to flow during the on time of boost switch S_2.
- The prototype circuit of the proposed converter has been fabricated and tested.
- A simulation model for the circuit configuration of the new converter also has been done using LT spice IV 4.22.
- The proposed architecture has been verified the simulated and the experimental results.

- The practical results confirmed the validity of the transfer function with a range of case studies have been included in this work.
- The highest achieved efficiency observed in the experiments is 97.7% while the average efficiency for selected test points is 95.85%.
- This work has been published in [85].

Chapter 5

Conclusions and Future Work

5.1 Conclusions

The aim of this dissertation is to investigate the AC to DC power conversion in single phase systems. Improving AC to DC power conversion is of increasing concern due to the rapidly growth in a wide variety of applications that use direct current and in different power levels starting from a few watts as in chargers of personal IT devices and upto a few mega watts as in converters for distributed generation systems.

- The first phase of this research is focused on the investigations to find a new approach of AC to DC rectification in single phase systems.

  A novel single phase rectification technique with a new architecture and control strategy is proposed. This technique is characterised by simplicity in design and reduced complexity in control scheme.

  The circuit configuration of the proposed rectifier is simple in construction and reliable. This rectifier consists of switched capacitor branch in parallel with the output of the diode bridge rectifier. The switched capacitor branch includes a capacitor and a bidirectional switch arranged in series so that the switch can control the charging and discharging of the capacitor. The circuit structure of the proposed switch-cell (bidirectional switch) uses two MOSFETs and a diode pair.

The control scheme that controls the action of the switch-cell is based on a simple and uncomplicated idea. This idea is based on choosing a threshold level for the output voltage of the rectifier. When the output voltage of the bridge rectifier is rising and it is above that threshold level, the switch is closed so that the capacitor charges and the load is supplied from the output of the bridge rectifier. When the output of the bridge rectifier is falling and it is above the threshold level, the switch is opened so that the capacitor is isolated from the load and it is fully charged, while the load still being supplied by the output of the bridge rectifier. When the output of the bridge rectifier is falling and it is below the threshold level, the switch is closed so that the load is served by discharging the capacitor, while the supply is automatically disconnected through the diodes of the bridge rectifier.

The new rectifier architecture provided no switching action (switching free) in the path of the rectifier current. Switching is only required in the parallel branch. This makes the rectifier very useful when is used in medium and high power applications as there is no more switching losses caused by extra switches in the path of the line current.

This rectifier allows to obtain high input power factor and thus higher efficiency to be achieved. The current harmonics generation is suppressed resulting in a lower level of harmonic content of the line current of the rectifier. The new architecture provides a reduction in the size of the DC side capacitor. This reduction can be as low as less than 10% of the size of the typical smoothing capacitor in the conventional single phase rectifier. The size of the smoothing capacitor restrict the increase in power density of the conventional rectifier system. The new rectifier now allows the possibility to increase the power rating of such loads to a higher values.

The prototype circuits of the proposed and the conventional rectifiers have been designed, fabricated and tested. A wide range of case studies have been undertaken to prove the validity of the new rectifier.

A comparison between the performances of the conventional and the proposed

rectifiers have been done by conducting two case studies under an identical testing conditions. The main disadvantage with the use of the conventional system is the low input power factor, typically between $0.3 - 0.6$. Also, the presence of the large smoothing capacitor results in the generation of a large line current harmonics injected to the utility AC supply networks which has a serious impact on the safe operation of other equipment or devices.

The proposed rectification technique has many features over the classic and the modified Valley fill circuit. These features are the ability of changing the conduction time of the line current freely. This can be done by adjusting the right threshold level that ensures the desired conduction time and thus the required power factor. The other feature is the ability of charging the DC side capacitor with nearly the peak value of the supply voltage. This results in a bigger amount of charge and thus an energy which can be stored into the capacitor and then supplied to the load.

The results proved the ability of the new technique to obtain a high input power factor. This is achieved with a reduced size capacitor in the DC side of the rectifier.

The proposed technique provided a reduction in the size of the DC side capacitor. This reduction is depending on the selected design parameters of the rectifier circuit and strongly depended on the value of the DC reference level (threshold level).

The threshold level also determines the ripple in the output voltage of the rectifier, so lower values of the threshold level will end-up with a large ripple in the output voltage. A trade off between the threshold level and an acceptable value of the ripple in the output voltage should rely in order to get a compromise solution to the ripple at the output of this rectifier. This is to ensure any further DC-DC conversion has a defined minimum and maximum input voltage range.

Woodward's notation is used to represent the line current in the AC side analysis of both rectifiers (proposed and conventional). Woodward's notation applied to chopped waveforms is considered a powerful method in analysing piecewise wave-

forms in terms of Fourier series expansion, Fourier Transform, and the frequency spectrum.

The harmonic analysis showed a lower harmonic content of the line current of the proposed technique with lower THD. The reduction in the harmonic content of the line current depends on the selected values of the voltage ratio (threshold level to the peak value of the supply voltage).

The performance analysis of the new technique showed that the best results can be obtained from this rectifier with a lower values of the voltage ratio. This is very desirable for a wide variety of applications. This work has been published in [83] and [84].

- The second phase of this research is focused on the DC-DC conversion architectures.

  A novel buck-boost converter architecture using close-coupled inductors with its transfer function is proposed.

  Coupled inductor is one of the essential component in power electronics circuits and plays a key role in the DC-DC converters. Converters utilises the coupled inductors topology can achieve a higher power density with a better performance. According to the way that the coupled inductors are coupled, whether they are directly or inversely coupled, the way they are made, whether they are loosely or interleaved wound and whether they are placed on two magnetic cores or combined on the same magnetic core, the characteristics and the performance of each single case will be different.

  The entire circuit of the new converter can be represented as two phases or stages (buck and boost). This circuit comprises a single power switch for each stage and single main inductor which is shared between the two stages. The proposed converter utilises close inversely-coupled inductors topology in both its conversion stages. It benefited from this topology in two different ways.

  In buck stage, this topology with additional passive component (capacitor) connected across the free terminals of coupled inductors and in series with a normal

diode can work as a passive clamped circuit. The function of the passive clamped circuit is to recycle the leakage energies of the coupled inductors which results in an efficiency improvement of the power converter. Also, this circuit is used to clamp the large voltage spikes (due to the impedance buffer provided by the coupled inductors) in order to limit the voltage stress on the main switch.

This configuration ensures a continuous current flow through the buck stage even with the off time of the buck switch. This results in a reduction in the back e.m.f induced in the main inductor and thus reducing the switching noise.

The switching noise resulting from the back e.m.f induced in the main inductor is considered as a major drawback in the conventional step-down converter circuits which causes large switching losses and results in high voltage stress on the power switch. These loses are often dissipated as heat, which requires an additional facilities to be added to the converter circuit and thus an increase in the size and cost of such converters. Furthermore, the outputs of the converter(current and voltage) are affected by the switching noise. This can be described as in the modulation in the communication systems where the noise signal is modulated over the converter outputs (the carrier signal).

The close coupled inductors arrangement also been utilised in the boost stage to ensure a continuous output current by providing an alternative (parallel) path for energy to flow during the on time of boost switch.

The first energy path can be formed by connecting the the output of the buck stage to the load side through a diode. The other path of energy can be formed by connecting the common point of the coupled inductors to the output of the buck stage, then the free end of one inductor is connected to the power switch of the boost stage, while the free end of the other inductor is connected to the load side through a diode. By this way, the two parallel paths are exchanged the delivery of energy to the load side during the on and off states of the boost switch.

The proposed DC-DC converter can work as just a buck, boost, or buck-boost

converter according to the applied set of duty cycles for the power switches S_1 and S_2. The transfer function of the buck-boost converter in CCM of operation and steady state conditions is presented. This transfer function is derived by getting the rate of change of the converter current in four different cases. These cases represent the logical permutations of both power switches of the converter.

The prototype circuit of the proposed converter has been fabricated and tested. The practical results confirmed the validity of the transfer function with a range of case studies have been included in this work. However, the results showed there is a small deviation in some test points from the equality line of the duty cycle. This deviation being more noticeable when the duty cycle of the boost switch skips the value of 50%. A simulation model for the circuit configuration of the new converter has been done using LT spice IV 4.22. In order to confirm the practical results, the simulation model has been examined with a range of case studies. The same design parameters of the prototype circuit and an identical testing conditions of the practical case studies have been applied during the simulation of this model. The proposed architecture has been verified the simulated and the experimental results.

The new topology strongly reduce the noise and thus the losses that usually accompanies the conventional buck and boost converter circuits. This results in high power conversion efficiency for this kind of converters dealing with a wide range of supply voltages and serves a wide variety of applications. The highest achieved efficiency observed in the experiments is 97.7% while the average efficiency for selected test points is 95.85%. Although, the measured efficiency showed a high efficiency power conversion has been achieved with the new converter architecture, further investigations can be done to determine the sources of loss in this circuit which can result in making this circuit to work more efficiently.

The new topology provides a reduction in the voltage stress of the power switches due to the impedance buffer provided by the coupled inductors. Moreover, the new architecture has little or no transient overshoot even while switching at constant

duty cycles and at a fixed switching frequency.

Finally, the proposed architecture provides a reduction in the total volume, weight and losses of the magnetic components used as both inductors (the coupled inductors) have been placed on the same magnetic core.

5.2 Future Work

The suggestions for the future work can be identified as in two groups:

5.2.1 The Rectification Technique Presented in Chapter 3

- The circuit configuration of the bidirectional switch can be modified in order to reduce the charging current during the charging mode (mode 1).
- This modification can be done by using a fixed (constant) charging current circuit placed in the charging side of the bidirectional switch and works during the entire period of mode 1.
- Another modification can be also useful for this purpose by connecting a small inductor in the path of the charging current (the charging side of the bidirectional switch) just before the capacitor with a free-wheeling diode connected across the capacitor and in series with this inductor. This arrangement would particularly suitable for use in conjunction with a higher frequency supplies, as the higher frequencies would allow the use of smaller inductor.
- The use of silicon carbide diode instead of the normal diode in building the circuit of the bidirectional switch. This diode has no reverse current, this current is the reason for some difficulties in the control of bidirectional switch circuit.
- A DC-DC converter connected in parallel with the output of the new rectifier in order to reduce the ripple of the output voltage and to deliver a level DC voltage to the connected load.

- Depending on the applied topology of the DC-DC converter, the output DC voltage that delivered to the load could be larger or smaller than the threshold level.

- A new prototype circuit of this rectifier in higher power scale can be designed and tested, in order to investigate the effects of the parasitic capacitance and inductance of the power switched and diodes on the performance of the proposed rectifier.

- An investigation can be done to find out how much this technique is feasible and applicable in three-phase four wires systems. This can be done through the implementation of three-single modules of the new rectifier and tested with a three-phase four wires power supply.

5.2.2 Buck-Boost DC-DC Converter Presented in Chapter 4

- The investigations to utilise the DC output of the proposed single phase rectifier in chapter 3, as the DC input to the proposed buck-boost converter presented in chapter 4.

- The use of Micro-controller (STM32F4 High-Performance Discovery Board) to control the work of the entire circuit (the rectifier and the DC-DC converter). This 168 MHz Micro-controller is $32-bit$ product range that combines very high performance and provides a large number of features, like the capability of precise monitoring and control with storage and debugging facilities built on the same motherboard. This can offer the capability to perform the required control action in order to maintain a stable and accurate output to the connected load.

- Further investigations in the boost stage of the proposed buck-boost converter in order to figure out the reasons of the non-linear performance of this stage when the applied duty cycle of the boost switch skips the value of 50%.

- An investigation can be done to determine the sources of loss in the converter circuit which can result in make this circuit work more efficiently. These investigations will include the analysis to determine the design parameters of the converter circuit

with a better component choice. This has to be done in conjunction with the work to specify the limits of the appropriate bandwidth of switching frequencies which ensures a better performance with the specified design parameters.

- A new prototype circuit of this converter in higher power scale can be designed and tested, in order to investigate the effects of the parasitic capacitance and inductance of the power switched and diodes on the performance of the proposed converter.

- An investigation can be done to find out the feasibility and the applicability of this topology in three-phase four wires systems. this can be done through the implementation of three-single modules of the DC-DC converter and tested with a three-phase four wires power supply.

Published Papers

IEEE IFEEC 2013, The 1st International Future Energy Electronics Conference Paper

Design of Single Bidirectional Switch Single Phase Rectifier with Reduced Size DC Side Capacitor

This paper was presented by the author at IEEE IFEEC 2013.

Design of Single Bidirectional Switch Single Phase Rectifier with Reduced Size DC Side Capacitor

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***Abstract*—A single phase rectification technique with a new architecture and control scheme is proposed. The new circuit is constructed by connecting a single bidirectional switch and capacitor in parallel to the diode bridge rectifier. The control strategy is carefully designed to maintain a high input power factor, provide a reduction in the size of the DC side capacitor and reduce the line current harmonics compared with the conventional rectifier. Circuit configuration, design parameters, principles of operation and the mathematical analysis are presented. The AC side harmonics analysis is done using Woodward's notation which applies to chopped waveforms. The proposed concept is verified by the experimental results of a case study.**

***Index Terms*—power density; rectification power rating**

I. INTRODUCTION

The enormous increase in non-linear loads connected to the utility power systems represent a serious challenge because of the pulsating withdrawn current. This result in huge harmonics on the AC side and thus reducing the power networks capacity and ability to absorb loads.

Harmonics are responsible for exposing the utility to a poor power factor and significant increase in losses and thus reduces power networks efficiency.

The reason behind this current harmonics phenomenon is the large smoothing capacitor required to reduce the power ripple in the DC side of the rectifier. The size of this capacitor restricts the capability of increasing the power density of such loads.

One of the widely used non liner loads is the conventional single phase rectifier. [1]–[3] Presents an input filter in series to the AC power supply of the bridge rectifier. The size, fixed compensation, resonance and losses considerations of the passive components remains the main drawbacks of these architectures [4].

Research [5]–[8] participated the same main idea of using shunt (PFC) boosting techniques to compensate the harmonic current drawn by the conventional single phase rectifier. [9]–[13] shared the key point of using shunt active power filter techniques to compensate for harmonic current of the conventional rectifier.

II. THE PROPOSED TECHNIQUE

A. Circuit Configuration

The circuit configuration of the proposed single phase rectifier is shown in figure 1. It consists of a branch of one bidirectional switch and capacitor connected in parallel to the diode bridge rectifier.

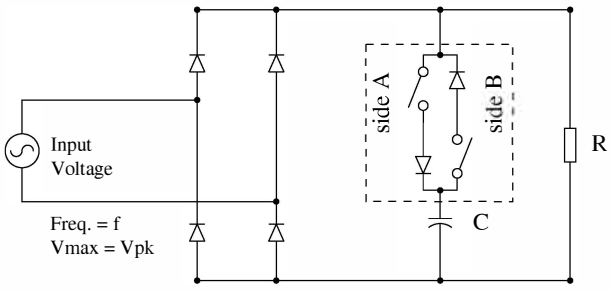


Fig. 1. The Circuit Configuration of The Proposed Rectifier

The circuit structure of the proposed bidirectional switch is shown in figure 2. This switch-cell uses two MOSFETs and diode pair.

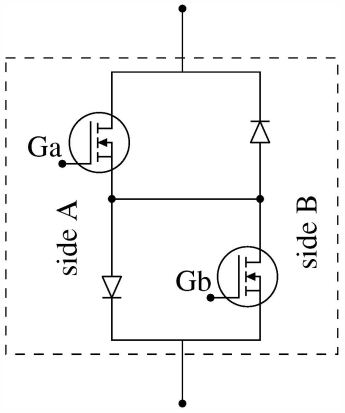


Fig. 2. The Structure of The Proposed Bidirectional Switch

The design parameters which they used to determine and evaluate the system performance in this technique are illustrated in table I

TABLE I
THE DESIGN PARAMETERS

Parameter	Definition
V_{pk}	The peak value of A.C. supply voltage (V_{max})
V_{ref}	The selected reference D.C. voltage level
f	The supply voltage frequency
R	The applied resistive load

B. Principles of Operation

The principles of operation of the proposed rectifier can be illustrated as shown in figure 3. The control scheme that governs the action of the bidirectional switch has divided the operation of this rectifier into three operating conditions or three modes.

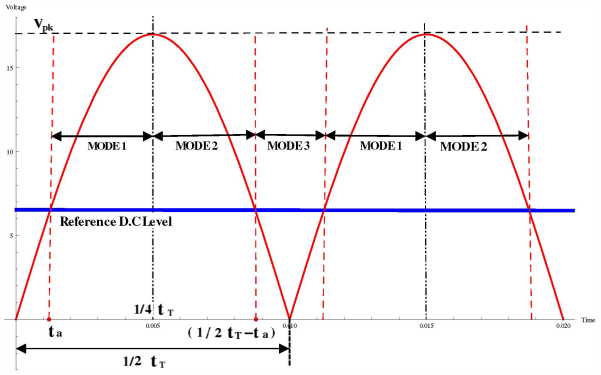


Fig. 3. The Operating Zones of The Proposed Technique

Modes are defined by the supply voltage (the output voltage from the bridge rectifier) in relation to the Reference DC level.

MODE 1 : When the instantaneous value of the supply voltage is increasing and it is greater than or equal to the Reference DC level. In this Mode,

- The bidirectional switch (side A) is now turned On, and (side B) is Off.
- The load and the capacitor are now both connected to the supply voltage.

This mode continues until the instantaneous value of the supply voltage reaches it's maximum value.

MODE 2 : When the instantaneous value of the supply voltage is decreasing and it is greater than or equal to the Reference DC level. In this Mode,

- The bidirectional switch (side A and side B) are both off. The capacitor is disconnected from the supply and it is fully charged.
- The load is still connected to the supply voltage.

This mode continues until the instantaneous value of the supply voltage falls below the Reference DC level.

MODE 3 : When the instantaneous value of the supply voltage is less than the Reference DC level. In this Mode,

- The bidirectional switch (side B) is turned On, and (side A) is Off.
- The capacitor is connected to the load, and the load current is completely served by the capacitor, while the supply is automatically disconnected through the diodes of the bridge rectifier.

This mode continues until the instantaneous value of the supply voltage in the next incoming half cycle becomes greater than or equal to the Reference DC level. Then leads to **MODE 1**.

As a result of this circuit configuration and switching scheme, the analytical line current waveform will be as shown in figure 4.

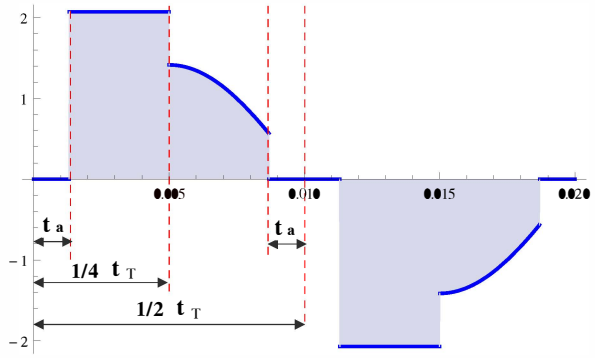


Fig. 4. The Analytical Line Current Waveform of The Proposed Rectifier

Where, t_T is the full cycle time of the supply voltage, t_a is zero line current period in time and it's definition will be in the section III.

This current consists of three periods which come from the three modes described above. It can be expressed the line current with it's three periods as in the following formula:

$$\mathrm{i}(t) \quad = \quad \begin{cases} I_{pk} & t_a \leq t < \frac{1}{4}t_T \\ I_{sk}\sin(\omega t) & \frac{1}{4}t_T \leq t < \frac{1}{2}t_T - t_a \\ 0 & \text{otherwise} \end{cases} \tag{1}$$

Where, $\omega = 2\pi f$, I_{pk} is the peak value of the rectangular pulse of line current (mode 1), I_{sk} is the peak value of the sinusoidal piecewise of line current (mode 2).

The value of the output voltage of the proposed rectifier can be expressed as in (2) and the average DC output voltage is given by (3).

$$V_{out} = \begin{cases} V_{pk}\ \sin(\omega t) & t_a \leq t < \frac{1}{2}t_T - t_a \\ V_{pk}\ e^{-\frac{2t}{CR}} & \frac{1}{2}t_T - t_a \leq t < \frac{1}{2}t_T + t_a \end{cases} \tag{2}$$

$$V_{DC} = \frac{2}{t_T}\left[\int_{t_a}^{\frac{1}{2}t_T - t_a} V_{pk}\ \sin(\omega t)\ dt + \int_{\frac{1}{2}t_T - t_a}^{\frac{1}{2}t_T + t_a} V_{pk}\ e^{-\frac{2t_a}{CR}}\ dt\right] \tag{3}$$

Where, C is the capacitance of the storage capacitor.

III. AC Side Analysis

To clarify the performance of the proposed technique, the harmonics analysis of the rectifier line current is done using Woodward's notation [14]. Woodward's notation is considered a powerful method in analysing piecewise waveforms in terms of Fourier series expansion, Fourier transform, and frequency spectrum. It is simplifies and makes it easier to deal with complicated waveforms like chopped waveforms or waveforms composed of different shapes.

AC side analysis also included the derivations to determine the size of the DC bus capacitor and the input power factor.

- The definitions of Woodward's notation can be expressed in the following formula:

$$\text{Rect}(t) = \mathcal{R}(t) = \begin{cases} 1 & -\frac{1}{2} < t < +\frac{1}{2} \\ \frac{1}{2} & t = \pm\frac{1}{2} \\ 0 & x < -\frac{1}{2} \text{ and } x > \frac{1}{2} \end{cases} \quad (4)$$

$$\text{Sinc}(f) = \mathcal{S}(f) = \begin{cases} \frac{\sin(\pi f)}{\pi f} & f \neq 0 \\ 1 & f = 0 \end{cases} \quad (5)$$

The Fourier Transform of the Rect and Sinc pulse can then be expressed as follows

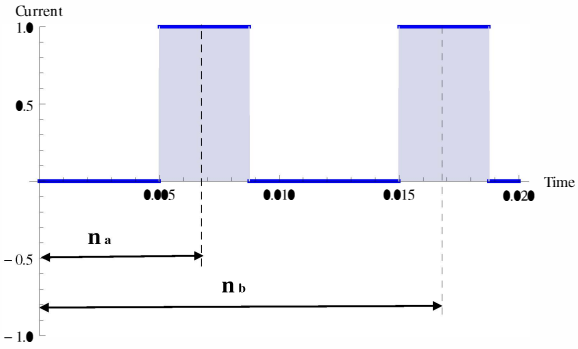
$$\text{Rect}(t) \Leftrightarrow \text{Sinc}(f) \quad (6)$$

$$\text{Rect}\left(\frac{t}{W}\right) \Leftrightarrow |W|\text{Sinc}(Wf) \quad (7)$$

$$\text{Rect}\left(\frac{t-a}{W}\right) \Leftrightarrow |W|\text{Sinc}(Wf)e^{-i2\pi af} \quad (8)$$

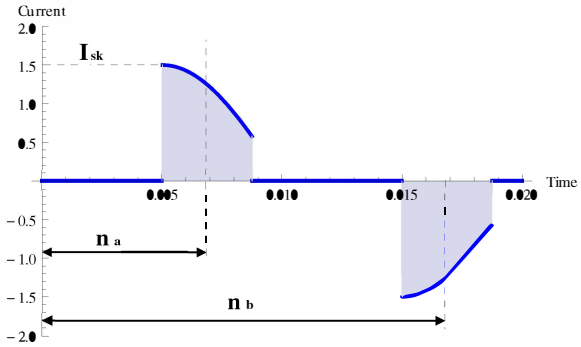
Where W is the pulse width in time, a is the pulse width centre in time, f is the frequency, i is the complex operator $i = \sqrt{-1}$.

- The line current waveform which is shown in figure 4, can be built using the Rect function and an expression for the portion of the waveform that is a chopped sinusoid. The process of obtaining the expression for the chopped sinusoid is first described here and then it will be applied to the full current waveform.
  The waveform of a pure sinusoid is multiplied with a train of unity amplitude Rect functions which shown in figure 5 can lead to a chopped sinusoid as shown in 6.



$$\mathcal{R}(t, n_a, \mathcal{W}) + \mathcal{R}(t, n_b, \mathcal{W})$$

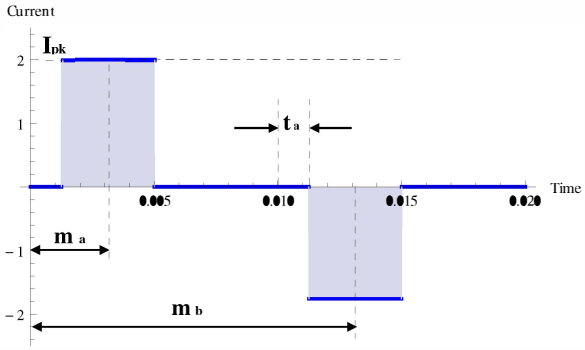
Fig. 5. Unity Amplitude Rect Pulses



$$i_1(t) = I_{sk}\sin(\omega t)\left[\mathcal{R}(t, n_a, \mathcal{W}) + \mathcal{R}(t, n_b, \mathcal{W})\right]$$

Fig. 6. Sinusoid Multiplied By Unity Amplitude Rect Pulses

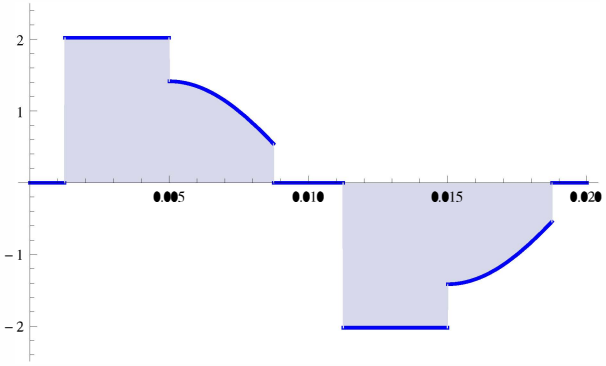
The Rect pulses for the rectangular pulses of the line current are shown in figure 7.



$$i_2(t) = I_{pk}\left[\mathcal{R}(t, m_a, \mathcal{W}) - \mathcal{R}(t, m_b, \mathcal{W})\right]$$

Fig. 7. Rect Pulses

The final waveform is a sum of Rect pulses and the chopped sinusoid as shown in figure 8.



$$i(t) = i_1(t) + i_2(t)$$

Fig. 8. The Line Current Waveform of The Proposed Rectifier

- The mathematical process that describes this procedure is as follows
  Given a design parameters, V_{pk}, V_{ref}, f, R.
  Defining

α is zero line current period in degree, t_a is zero line current period in time.

$$\alpha = \sin^{-1}\left(\frac{V_{ref}}{V_{pk}}\right) \tag{9}$$

$$t_a = \left[\left(\frac{\alpha}{90}\right)\left(\frac{1}{4\ f}\right)\right] \tag{10}$$

Using definitions

$$\mathcal{R}(t,a,W) = \text{Rect}\left[\frac{t-a}{W}\right] \tag{11}$$

$$\mathcal{S}(f,a,W) = |W|\ \text{Sinc}\ (Wf)\cdot e^{-i2\pi af} \tag{12}$$

In figure 5, 6, and 7.

$$n_a = \frac{1}{4f} + \frac{\mathcal{W}}{2} \tag{13}$$

$$n_b = \frac{3}{4f} + \frac{\mathcal{W}}{2} \tag{14}$$

$$\mathcal{W} = \left(\frac{1}{4f} - t_a\right) \tag{15}$$

$$m_a = \left[t_a + \frac{1}{4f}\right]0.5 \tag{16}$$

$$m_b = \left[t_a + \frac{5}{4f}\right]0.5 \tag{17}$$

The multiplication of the pure sinusoid with the unity amplitude Rect pulses leads to the convolution of the expressions in the frequency domain.
Starting with

$$|W|\ \text{Sinc}\ \ [fW]\cdot e^{-i2\pi af}$$

and convolve it with the frequency domain expression of a pure sinusoid of frequency d given by

$$\frac{i}{2}\left[\delta(d) - \delta(-d)\right]$$

where $\delta(d)$ is a Dirac function, $d = 50$.
The convolution

$$\left(|W|\ \text{Sinc}\ \ [fW]\cdot e^{-i2\pi af}\right) * \left(\frac{i}{2}\left[\delta(d) - \delta(-d)\right]\right)$$

where $*$ denotes the convolution operator, leads to

$$|W|\frac{i}{2}\Big[\text{Sinc}\left[(f+d)W\right]e^{-i2\pi a(f+d)} - \text{Sinc}\left[(f-d)W\right]e^{-i2\pi a(f-d)}\Big]$$

Thus defining a new function

$$\mathcal{S}_n(f,a,w,d) = \frac{|W|i}{2}\Big[\text{Sinc}\left[(f+d)W\right]e^{-i2\pi a(f+d)} - \text{Sinc}\left[(f-d)W\right]e^{-i2\pi a(f-d)}\Big] \tag{18}$$

This then leads to the following expression for the current waveform shown in figure 8.

$$i(t) = I_{pk}\left[\mathcal{R}(t,m_a,\mathcal{W}) - \mathcal{R}(t,m_b,\mathcal{W})\right] + I_{sk}\sin(\omega t)\left[\mathcal{R}(t,n_a,\mathcal{W}) + \mathcal{R}(t,n_b,\mathcal{W})\right] \tag{19}$$

This then enables to get an expression for the frequency domain spectra from inspection as

$$I(f) = I_{pk}\left[\mathcal{S}(f,m_a,\mathcal{W}) - \mathcal{S}(f,m_b,\mathcal{W})\right] + I_{sk}\left[\mathcal{S}_n(f,n_a,\mathcal{W},d) + \mathcal{S}_n(f,n_b,\mathcal{W},d)\right] \tag{20}$$

Assuming the current is periodic, the spectral components at integer multiples of f are defined as

$$A(n) = \text{Re}[I(fn)]2f \tag{21}$$

$$B(n) = -\,\text{Im}[I(fn)]2f \tag{22}$$

Where, n is an integer, and this results in the following Fourier series expansion for $i(t,n)$.

$$i_h(t,n) = \left[A(n)\cos(\omega nt) + B(n)\sin(\omega nt)\right] \tag{23}$$

Where, i_h is the rms value of the current of harmonic order n.

$$i(t,n) = \sum_{k=1}^{n} i_h(t,k) \tag{24}$$

And the magnitude of spectral component at n is given by

$$S(n) = \sqrt{A(n)^2 + B(n)^2} \tag{25}$$

- The capacitance of the storage capacitor can be expressed as in the following formula

$$C = \frac{2\ t_a}{\ln(\frac{V_{pk}}{V_{ref}})\cdot R} \tag{26}$$

At t = $\frac{1}{4}\ t_T$,

$$I_c = \frac{C(V_{pk} - V_{ref})}{(\frac{1}{4}\cdot t_T - t_a)} \tag{27}$$

Where, I_c is the current of the storage capacitor.

$$I_{sk} = \frac{V_{pk}}{R} \tag{28}$$

And

$$I_{pk} = I_{sk} + I_c \tag{29}$$

Let

$$\gamma = \left(1 - \frac{V_{ref}}{V_{pk}}\right) \tag{30}$$

$$\beta = \frac{2\ t_a\cdot\gamma}{ln(\frac{V_{pk}}{V_{ref}})(\frac{1}{4}\ t_T - t_a)} \tag{31}$$

The substitution of (26), (27), (28), (30), and (31) in (29) will result

$$I_{pk} = I_{sk}\ [1+\beta] \tag{32}$$

- The input power factor PF can be derived as follows Starting with

$$PF = \frac{P_{av}}{P_{va}} \tag{33}$$

Where P_{av} is the average input power, P_{va} is the Volt-Amperes.

$$P_{av} = \frac{1}{T}\int_0^T v(t)\cdot i(t)\ dt \tag{34}$$

Where $i(t)$ is as expressed in (19) or it can be expressed as in (1), whilst the input voltage is given by

$$v(t) = V_{pk}\cdot \sin(\omega t) \tag{35}$$

That leads to the following expression of average input power

$$P_{av} = V_{pk}\left[I_{pk}\cdot J + I_{sk}\cdot K\right] \tag{36}$$

Where,

$$J = \left(\frac{\cos(\omega t_a)}{\pi}\right) \tag{37}$$

$$K = \left(\frac{1}{4} - \frac{t_a}{t_T}\right) + \left(\frac{\sin(2\omega t_a)}{4\pi}\right) \tag{38}$$

The Volt-Amperes

$$P_{va} = I_{rms}\cdot V_{rms} \tag{39}$$

Where,

$$V_{rms} = \frac{V_{pk}}{\sqrt{2}} \tag{40}$$

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T \left[i(t)^2\right]\ dt} \tag{41}$$

Applying the current expression of (1) in (41), then multiplying the result with (40) to get the final expression for (39)

$$P_{va} = \frac{V_{pk}^2}{\sqrt{2}\cdot R}\sqrt{\left[1+\beta\right]^2\cdot E + K} \tag{42}$$

Where,

$$E = \left(\frac{1}{2} - \frac{2\ t_a}{t_T}\right) \tag{43}$$

Applying the expressions of (36) and (42) in (33) to get the final expression of input power factor

$$PF = \frac{\sqrt{2}\cdot\left[(1+\beta)\cdot J + K\right]}{\sqrt{(1+\beta)^2\cdot E + K}} \tag{44}$$

IV. THE EXPERIMENTAL SETUP

The prototype circuit of the proposed rectifier has been designed and fabricated. A Single control circuit has been used to generate two different control signals which are used to fire two MOSFET driver circuits (both sides of the bidirectional switch circuit), two N-channel MOSFETs have been used as switching devices.

To prove the validity of the proposed rectifier a case study has been undertaken which includes the test of the prototype circuit and the AC side analysis of the test results obtained. The following design parameters have been applied in the experimental setup of the prototype rectifier circuit.

TABLE II
APPLIED DESIGN PARAMETERS IN CASE STUDY

Parameter	Value
V_{pk}	$17\ V$
V_{ref}	$6.5\ V$
f	$50\ H_z$
R	$12\ \Omega$

The analysis in the case presented are verified by the experimental results.

Some approximations to the experimental waveforms of current have been made in order to simplify the waveforms. These approximations result in an upper limit to the harmonic content of the current waveform. The input voltage waveform in this section is assumed to be a pure sinusoid, however the experimental input voltage waveform is best described as an asymmetric-flat-top sinusoid.

The actual line current waveform is shown in figure 9. The three portions of line current which mentioned earlier in section II-B are very obvious in this figure but there is some unequally in the zero current periods. The reason for that is the leakage current which comes from the action of the bidirectional switch circuit. This is due to the delay between switching on the incoming device (side 1) and switching off the outgoing device (side 2). This leakage current would not makes any noticeable difference on the rest of the current periods.

The frequency spectrum of the analytical line current is shown in figure 10 which illustrates the frequency content up to harmonic order of 40.

The input power factor is obtained by applying the derived expression for the power factor and for this case it computed as 0.94.

V. CONCLUSION AND DISCUSSION

A single phase rectification technique with a new architecture and control strategy is proposed in this paper. The prototype circuit has been designed, fabricated and tested. A case study has been undertaken to prove the validity of the proposed rectifier.

The results proved the ability of the new technique to obtain a high input power factor 0.94 for the above case study. This power factor is obtained with a small capacitor 217 μF in the

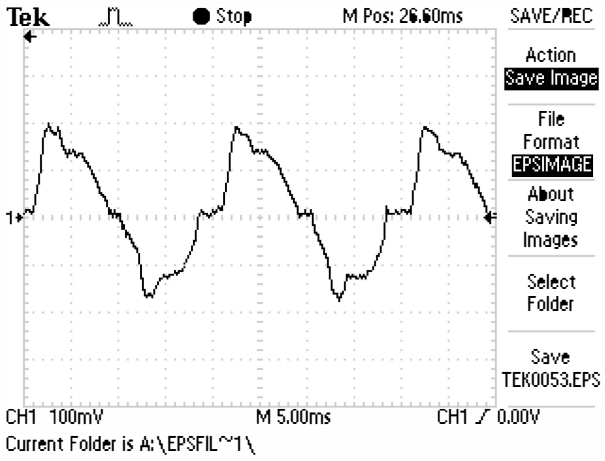


Fig. 9. The Practical Line Current Waveform of The Proposed Technique

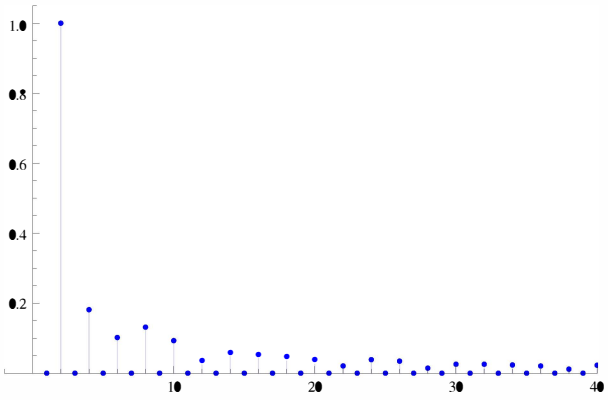


Fig. 10. The Frequency Spectrum of line Current of The Proposed Technique

DC side of the rectifier. The proposed technique provided a significant reduction in the size of the DC side capacitor. This reduction is depending on the selected design parameters and strongly depended on the value of DC reference level.

The harmonics analysis for the rectifier line current has been done using Woodward's notation applied to chopped waveforms. In this analysis the frequency spectrum showed that the frequency content has the following features:

1) Number of existing harmonics have a considerable amplitude. As there are just four harmonics orders beyond the fundamental. All harmonics beyond the 9th harmonic are below 6% of the fundamental.
2) Amplitude of the existing harmonics. As the amplitude of the existing harmonics is small compered to the fundamental.

Finally, the new architecture provided no switching action (switching free) in the path of the rectifier current. Switching is only required in the parallel branch. That makes the rectifier very useful when used in medium and high power applications as there is no more switching losses caused by extra switches in the path of the rectifier current.

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REFERENCES

[1] M. Khan, A. Pavel, M. Khan, and M. Choudhury, "Design of a single phase rectifier with switching on ac side for high power factor and low total harmonic distortion," in *Region 5 Technical Conference, 2007 IEEE*, april 2007, pp. 289 –292.

[2] A. Prasad, P. Ziogas, and S. Manias, "A novel passive waveshaping method for single-phase diode rectifiers," *Industrial Electronics, IEEE Transactions on*, vol. 37, no. 6, pp. 521 –530, dec 1990.

[3] J. Yanchao, L. Xiaobing, L. Zhuo, J. Jisheng, and L. Xinhua, "An improved passive input current waveshaping method for single-phase diode rectifier," in *Industrial Electronics, Control, and Instrumentation, 1996., Proceedings of the 1996 IEEE IECON 22nd International Conference on*, vol. 2, aug 1996, pp. 695 –699 vol.2.

[4] L. Moran, L. Dixon, and R. Wallace, "A three-phase active power filter operating with fixed switching frequency for reactive power and current harmonic compensation," *Industrial Electronics, IEEE Transactions on*, vol. 42, no. 4, pp. 402–408, 1995.

[5] S. Sahoo and H. Jariwala, "A new power factor correction technique using pfc boost converter," in *Environment and Electrical Engineering (EEEIC), 2012 11th International Conference on*, may 2012, pp. 819 –823.

[6] N. Hamzah, M. Hamzah, A. Hasim, and N. Rahman, "Single-phase shunt active power filter using single-switch incorporating boost circuit," in *Power and Energy Conference, 2008. PECon 2008. IEEE 2nd International*, dec. 2008, pp. 1112 –1117.

[7] A. Hasim and M. Hamzah, "Single-phase shunt active power filter using boost rectifier technique," in *Electric Machines Drives Conference, 2007. IEMDC '07. IEEE International*, vol. 2, may 2007, pp. 1294 –1299.

[8] A. Hasim and M. Saidon, "Development of a single-phase shunt active power filter using boost rectifier technique," in *Research and Development, 2006. SCOReD 2006. 4th Student Conference on*, june 2006, pp. 262 –265.

[9] C.-C. Hou, "A common single-phase diode rectifier for multi-load system with an auxiliary converter," in *Power Electronics Conference (IPEC), 2010 International*, june 2010, pp. 1586 –1589.

[10] B. Singh, K. Al-Haddad, and A. Chandra, "A universal active power filter for single-phase reactive power and harmonic compensation," in *Power Quality '98*, jun 1998, pp. 81 –87.

[11] Z. Hussien, N. Atan, and I. Abidin, "Shunt active power filter for harmonic compensation of nonlinear loads," in *Power Engineering Conference, 2003. PECon 2003. Proceedings. National*, dec. 2003, pp. 117 – 120.

[12] A. Bakhshai, H. Karimi, and M. Saeedifard, "A new adaptive harmonic extraction scheme for single-phase active power filters," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 3, may 2003, pp. III–268 – III–271 vol.3.

[13] B. Singh, A. Chandra, and K. Al-Haddad, "An improved single phase active power filter with optimum dc capacitor," in *Industrial Electronics, Control, and Instrumentation, 1996., Proceedings of the 1996 IEEE IECON 22nd International Conference on*, vol. 2, aug 1996, pp. 677 –682 vol.2.

[14] P. Woodward and I. Davies, "Information theory and inverse probability in telecommunication," *Proceedings of the IEE - Part III: Radio and Communication Engineering*, vol. 99, no. 58, pp. 37 –44, march 1952.

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High Power Factor Single Phase Rectification Technique with Reduced Line Current Harmonics

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High Power Factor Single Phase Rectification Technique with Reduced Line Current Harmonics

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***Abstract*—A single phase rectification technique with a new architecture and control scheme is proposed. The new circuit is constructed by connecting a single bidirectional switch and capacitor in parallel to the diode bridge rectifier. The control strategy is carefully designed to ensure the output voltage of the rectifier is above a chosen threshold and to maintain a high input power factor with reduced line current harmonics.**

Circuit configuration, design parameters, principles of operation and the mathematical analysis are presented. The proposed concept is verified by the experimental results over a range of cases studies. The experimental results are in accordance with the presented theory and confirmed the high input power factor with low harmonics content.

***Index Terms*—Single phase rectifier; Bidirectional switch; Power factor correction; Total harmonic distortion.**

I. INTRODUCTION

The widespread use of applications with switch mode power supply that connected to the utility power system in the recent years highlights the problem of the pulsating currents withdrawn by these non-linear loads.This result in huge harmonics on the AC side and thus reducing the power networks capacity and ability to manage loads. The current harmonics produced by non-linear loads tend to produce voltage harmonics on the AC side which have an effect on the harmonics characteristics of the line current of non-liner loads [1]. [2] Proposed a single MOSFET switch and series LC filter connected in series to the AC side of the bridge rectifier. This circuit used as an alternative path for the input current to keep it in continuous flow. [3] Presents an input filter in series to the AC power supply. The inductor and the capacitor of the passive circuit are connected in parallel. The size, cost, fixed compensation, resonance and losses considerations of the passive components remains the main drawbacks of both architectures [4]. Conventional single phase rectifier with a shunt active power filter are widely used in power factor correction (PFC) and harmonic current compensation applications. [5]–[7] follow the theme of using shunt PFC boosting techniques to compensate the harmonic current drawn by the conventional rectifier. [8]–[12] shared the key point of using shunt active power filter techniques to compensate for harmonic current of the rectifier. Various control schemes have been proposed and discussed in these research. Passive PFC valley fill circuit and a modified valley fill circuits presented by [13]–[15] which have the advantages of lower circuit complexity than the active PFC circuits.

II. THE PROPOSED TECHNIQUE

A. Circuit Configuration

The circuit configuration of the proposed single phase rectifier is shown in figure 1. It consists of a branch of one bidirectional switch and capacitor connected in parallel to the diode bridge rectifier.

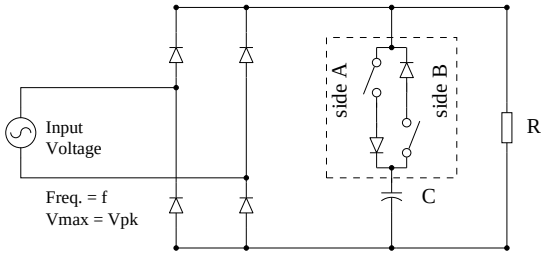


Fig. 1. The Circuit Configuration of The Proposed Rectifier

The circuit structure of the proposed bidirectional switch is shown in figure 2. This switch-cell uses two MOSFETs and a diode pair.

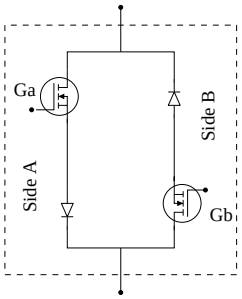


Fig. 2. The Structure of The Proposed Bidirectional Switch

The design parameters used to determine and evaluate the system performance of this technique are illustrated in table I.

TABLE I
THE DESIGN PARAMETERS

Parameter	Definition
V_{pk}	The peak value of A.C. supply voltage
V_{ref}	The selected reference D.C. voltage level
f	The supply voltage frequency
R	The applied load

B. Principles Of Operation

The principles of operation of the proposed rectifier can be illustrated as shown in figure 3. The control scheme that governs the action of the bidirectional switch has divided the operation of this rectifier into three operating conditions or three modes.

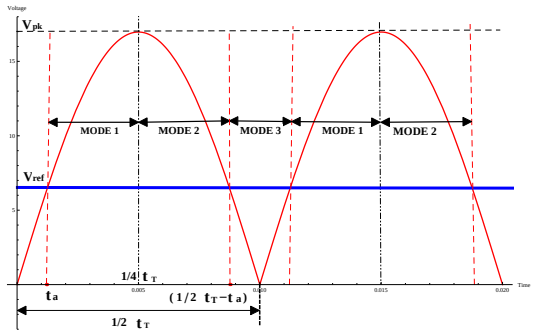


Fig. 3. The Operating Zones of The Proposed Technique

Modes are defined by the supply voltage (the output voltage from the bridge rectifier) in relation to the reference DC level V_{ref}.

MODE 1 : When the instantaneous value of the supply voltage is increasing and it is greater than or equal to the reference DC level. In this mode,

- The bidirectional switch (side A) is now turned On, and (side B) is Off.
- The load and the capacitor are now both connected to the supply voltage.

The equivalent circuit of the rectifier DC side in mode 1 is shown in figure 4.
Where I_s is the rectifier line current, I_c is the capacitor branch current, I_r is the load current, R_{oe} is the equivalent series resistance of the capacitor and MOSFETs.

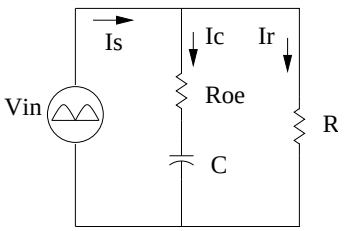


Fig. 4. The Equivalent Circuit of The Rectifier at Mode 1

It can be expressed the rectifier line current I_s of mode 1 in frequency domain as in (1).

$$I_s = \frac{\omega s V_{pk}}{R_{oe}\left(\omega^2 + s^2\right)(a+s)} - \frac{V_{ref}}{R_{oe}(a+s)} + \frac{\omega V_{pk}}{R\left(\omega^2 + s^2\right)} \quad (1)$$

Where,

$$a = \frac{1}{R_{oe}\ C} \quad (2)$$

$$R_{oe} = R_{DS(ON)} + ESR \quad (3)$$

$R_{DS(ON)}$ is the On state resistance of the used MOSFETs, ESR is the equivalent series resistance of the storage capacitor.
This mode continues until the instantaneous value of the supply voltage reaches it's maximum value.
MODE 2 : When the instantaneous value of the supply voltage is decreasing and it is greater than or equal to the reference DC level. In this mode,

- The bidirectional switch (side A and side B) are both off. The capacitor is disconnected from the supply and it is fully charged.
- The load is still connected to the supply voltage.

The equivalent circuit of this mode is just a resistive load connected to the bridge rectifier. The line current of the rectifier during mode 2 can be expressed as in (4).

$$I_s = \frac{V_{pk}}{R} \cdot \frac{\omega}{(\omega^2 + s^2)} \quad (4)$$

This mode continues until the instantaneous value of the supply voltage falls below the reference DC level.
MODE 3 : When the instantaneous value of the supply voltage is less than the reference DC level. In this Mode,

- The bidirectional switch (side B) is turned On, and (side A) is Off.
- The capacitor is connected to the load, and the load current is completely supplied by the capacitor, while the supply is automatically disconnected through the diodes of the bridge rectifier.

The equivalent circuit for this mode is a simple RC circuit and the rectifier current can be expressed as in (5). This mode continues until the instantaneous value of the supply voltage in the next incoming half cycle becomes greater than or equal to the reference DC level. Then **MODE 1** follows as shown in 3.

$$I_s = \frac{V_{ref}}{(R_{oe} + R) \cdot (b+s)} \quad (5)$$

Where,

$$b = \frac{1}{(R_{oe} + R) \cdot C} \quad (6)$$

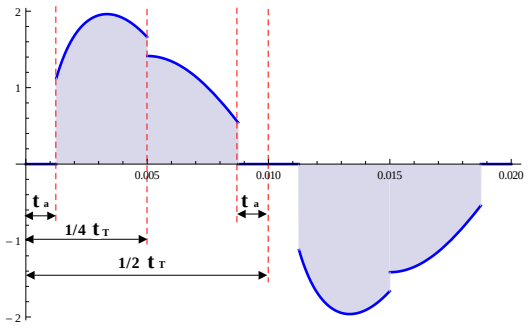


Fig. 5. The Analytical Line Current Waveform of The Proposed Rectifier

As a result of this circuit configuration and switching scheme the analytical line current waveform will be as shown in figure 5.

Where t_T is the full cycle time of the supply voltage, t_a is zero line current period in time and it's definition will be in the section III.

In comparison with the current waveform presented in [16] this current is more accurate and closer to reality as it came from the exact expression of the line current with no approximations or assumptions have been made.

It can be expressed the line current with it's three periods as in the following formula:

$$\mathrm{i}(t) \quad = \quad \begin{cases} I_1(t) & t_a \leq t < \frac{1}{4}t_T \\ I_2(t) & \frac{1}{4}t_T \leq t < \frac{1}{2}t_T - t_a \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

Where

$I_1(t)$ is the line current flowing during mode 1 and it's expression is given by (8), $I_2(t)$ is the line current flowing during mode 2 and it's expression is given by (9).

$$I_2(t) = I_{sk}\sin(\omega t) \tag{9}$$

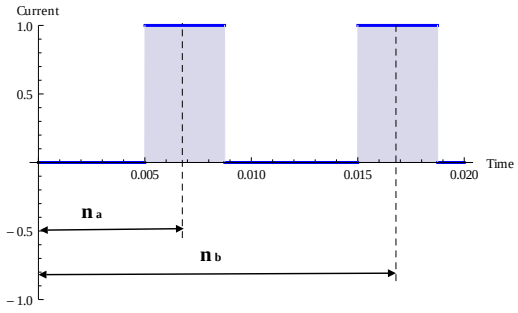
$$I_{sk} = \frac{V_{pk}}{R} \tag{10}$$

Where, I_{sk} is the peak value of line current in (mode 2), I_{pk} is the peak value of line current in (mode 1), $\omega = 2\pi f$, C is the capacitance of the storage capacitor.

III. AC Side Analysis

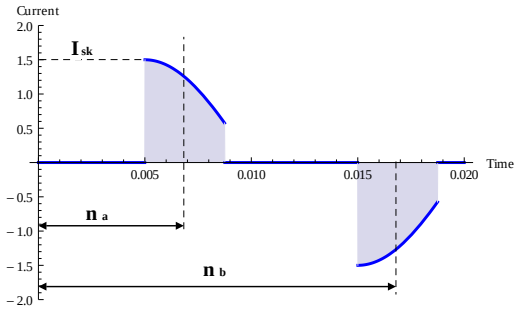
To clarify the frequency content of the AC side of the proposed rectifier the harmonics analysis of the line current has been done. In order to get the full and exact current formula for each of the current portions, the equivalent circuit of each mode in Laplace domain is determined and the rectifier current in frequency domain is obtained. The inverse Laplace transform is applied to get the full current formula in time domain. The representation of the rectifier current is done using Woodward's notation [17].AC side analysis also includes the calculations to determine the size of the DC bus capacitor, THD and the input power factor. This analysis is done using Wolfram Mathematica 9 and the results are verified by the experimental results of cases studies.

- The definitions of Woodward's notation are clearly illustrated in [16].
- The line current waveform shown in figure 5 can be built using two expressions. The first is for the portion of waveform that represent line current during mode 1. The second is for the portion of waveform that is a chopped sinusoid and represents the current during mode 2. The process of obtaining the expression for the chopped sinusoid is first described here and then it will be applied to the full current waveform.
  The waveform of a pure sinusoid is multiplied with a train of unity amplitude Rect function which shown in figure 6 that can lead to a chopped sinusoid as shown in figure 7.



$$\mathcal{R}\left(t, n_a, \mathcal{W}\right) + \mathcal{R}\left(t, n_b, \mathcal{W}\right)$$

Fig. 6. Unity Amplitude Rect Pulses



$$i_2\ (t) = I_2(t)\left[\mathcal{R}\left(t, n_a, \mathcal{W}\right) + \mathcal{R}\left(t, n_b, \mathcal{W}\right)\right]$$

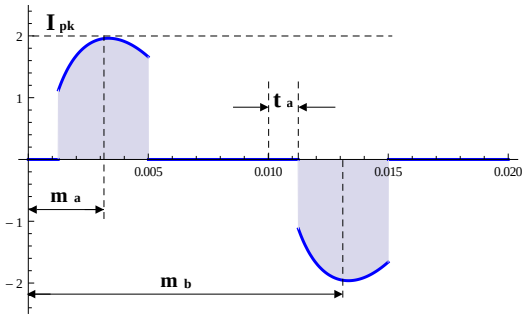
Fig. 7. Sinusoid Multiplied By Unity Amplitude Rect Pulses

The same process can be applied to get an expression for the current in mode 1. The line current waveform of mode 1 which described in (8) is multiplied with a train of unity amplitude Rect function. That can lead to the current waveform shown in figure 8.

The final waveform is a sum of the two waveforms portions $i(t) = i_1(t) + i_2(t)$ as shown in figure 5.

- The mathematical process that describes this procedure is as follows
  Given a design parameters, V_{pk}, V_{ref}, f, R.
  Defining

$$I_1(t) = \frac{a^2 R_{oe} V_{pk} \sin(\omega t) + \omega a R V_{pk} \cos(\omega t) + \omega^2 R V_{pk} \sin(\omega t) + \omega^2 R_{oe} V_{pk} \sin(\omega t)}{R R_{oe} \left(a^2 + \omega^2\right)} + \frac{e^{-at}\left(a^2(-V_{ref}) - \omega a V_{pk} - \omega^2 V_{ref}\right)}{R_{oe}\left(a^2 + \omega^2\right)} \tag{8}$$



$$i_1\ (t) = I_1(t)\left[\mathcal{R}\left(t, m_a, \mathcal{W}\right)\right] - I_1\left(t - \tfrac{1}{2}t_T\right)\left[\mathcal{R}\left(t, m_b, \mathcal{W}\right)\right]$$

Fig. 8. Rect Pulses

α is zero line current period in degree, t_a is zero line current period in time.

$$\alpha = \sin^{-1}\left(\frac{V_{ref}}{V_{pk}}\right) \tag{11}$$

$$t_a = \left[\left(\frac{\alpha}{90}\right)\left(\frac{1}{4\ f}\right)\right] \tag{12}$$

Defining

$$\mathcal{R}\left(t, a, W\right) = \text{Rect}\left[\frac{t-a}{W}\right] \tag{13}$$

In figure 6, 7 and 8.

$$n_a = \frac{1}{4f} + \frac{\mathcal{W}}{2} \tag{14}$$

$$n_b = \frac{3}{4f} + \frac{\mathcal{W}}{2} \tag{15}$$

$$\mathcal{W} = \left(\frac{1}{4f} - t_a\right) \tag{16}$$

$$m_a = \left[t_a + \frac{1}{4f}\right] 0.5 \tag{17}$$

$$m_b = \left[t_a + \frac{5}{4f}\right] 0.5 \tag{18}$$

This then leads to the following expression for the current waveform shown in figure 5.

$$\begin{aligned} i(t) =& I_1(t)\left[\mathcal{R}\left(t, m_a, \mathcal{W}\right)\right] - I_1\left(t - \frac{1}{2}t_T\right)\left[\mathcal{R}\left(t, m_b, \mathcal{W}\right)\right] + \\ & I_2(t)\left[\mathcal{R}\left(t, n_a, \mathcal{W}\right) + \mathcal{R}\left(t, n_b, \mathcal{W}\right)\right] \end{aligned} \tag{19}$$

Assuming the current is periodic, the spectral components at integer multiples of f are defined as

$$A(n) = \frac{2}{t_T}\int_0^{t_T} i(t)\cos(\omega n t) \tag{20}$$

$$B(n) = \frac{2}{t_T}\int_0^{t_T} i(t)\sin(\omega n t) \tag{21}$$

where n is an integer and this results in the following Fourier series expansion for $i(t, n)$

$$i_h(t, n) = \left[A(n)\cos(\omega n t) + B(n)\sin(\omega n t)\right] \tag{22}$$

Where i_h is the rms value of current of harmonic order n.

$$i(t, n) = \sum_{k=1}^{n} i_h(t, k) \tag{23}$$

And the magnitude of spectral component at n is given by

$$S(n) = \sqrt{A(n)^2 + B(n)^2} \tag{24}$$

- The THD can be derived from the above expression of line current in the time domain.
Using definition of THD,

$$THD = \sqrt{\sum_{h=2}^{40}\left(\frac{I_h}{I_1}\right)^2} \tag{25}$$

Where I_1 is the frequency spectra of the fundamental harmonic, I_h is the frequency spectra of the harmonic order h.
- The capacitance of the storage capacitor can be expressed as in the following formula

$$C = \frac{2\ t_a}{\ln(\frac{V_{pk}}{V_{ref}}) \cdot (R + R_{oe})} \tag{26}$$

- The input power factor PF can be derived as follows
Starting with

$$PF = \frac{P_{av}}{P_{va}} \tag{27}$$

Where P_{av} is the average input power, P_{va} is the Volt-Amperes.

$$P_{av} = \frac{1}{t_T}\int_0^{t_T} v(t) \cdot i(t)\ dt \tag{28}$$

Where $i(t)$ is as expressed in (19).
The Volt-Amperes

$$P_{va} = I_{rms} \cdot V_{rms} \tag{29}$$

Where

$$I_{rms} = \sqrt{\frac{1}{t_T}\int_0^{t_T} [i(t)^2]\ dt} \tag{30}$$

IV. THE EXPERIMENTAL SETUP

The prototype circuit of the proposed rectifier has been designed and fabricated. A single control circuit has been used to generate two different control signals which are used to fire two MOSFET driver circuits (both sides of the bidirectional switch circuit). Two N-channel MOSFETs have been used as switching devices with high-side MOSFET drivers to drive them. The function of the control circuit is to generate the control signals according to the intersection points between the instantaneous values of the full wave rectifier output voltage and the reference DC level. This ensures the implementation of the three operation modes mentioned earlier.

V. RESULTS AND DISCUSSION

To prove the validity of the proposed rectifier a range of cases studies have been undertaken. They includes the test of the prototype circuit and the AC side analysis of the test results obtained. The design parameters illustrated in table II have been applied in the experimental setup of the prototype circuit as one of these cases studies. The analysis in the case presented are verified by the experimental results.

TABLE II
APPLIED DESIGN PARAMETERS IN CASE STUDY

Parameter	Value
V_{pk}	$12\sqrt{2}\ V$
V_{ref}	$6.5\ V$
f	$50\ H_z$
R	$12\ \Omega$

The measured line current waveform is shown in figure 9. The three portions of line current which mentioned earlier in section II-B are very obvious in this figure.

The frequency spectrum of the analytical line current is shown in figure 10 which illustrates the harmonics content up to harmonic order of 40. In that figure there are just four harmonics orders beyond the fundamental (no remarkable harmonic beyond the 9th harmonic) and the amplitude of the existing harmonics is small compered to the fundamental. The input power factor is obtained by applying the derived expression of power factor in the AC side analysis and it computed as 0.95 for this case.

The performance of the proposed rectification techniques has been examined with different sets of design parameters. The system analysis is verified experimentally by the results of selected test points and they were in accordance with each other. .

- The input power factor variation against the voltage ratio (V_{ref}/V_{pk}) with different loading conditions is shown in figure 11. It is clear that the proposed rectifier maintain a nearly unity power factor up to 20% of this ratio.

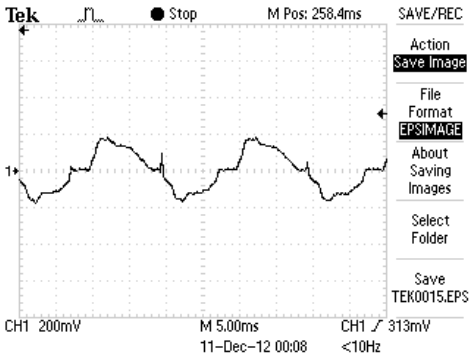


Fig. 9. The experimental Line Current Waveform of The Proposed Technique

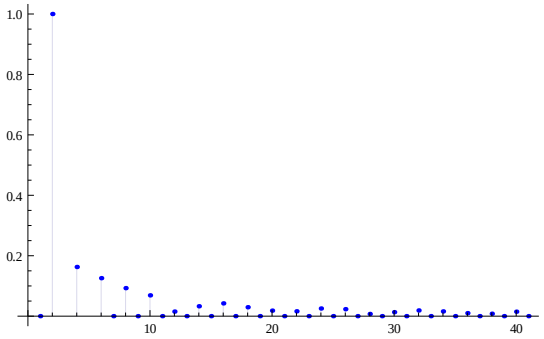


Fig. 10. The Frequency Spectrum of The Line Current of The Proposed Technique

- The required DC side capacitor in relation to the voltage ratio under different applied loads is shown in figure 12. The capacitor size is strongly depends on the voltage ratio and it is reasonably small up to 30% of this ratio.
- THD of the line current also in relation to the voltage ratio with variety loads is shown in figure 13. THD is nearly 3% at 10% and 10% at 20% of this ratio.

VI. CONCLUSION

A single phase rectification technique with a new architecture and control strategy is proposed in this paper. This technique is characterised by simplicity in design and reduced complexity in the control scheme. The prototype circuit has been designed, fabricated and tested. A range of cases studies have been undertaken.The results proved the ability of the new technique to obtain a high input Power Factor. This is obtained with a small capacitor in the DC side of the rectifier. The technique provided a significant reduction in the size of the DC side capacitor. This reduction is depending on the selected design parameters and strongly depended on the

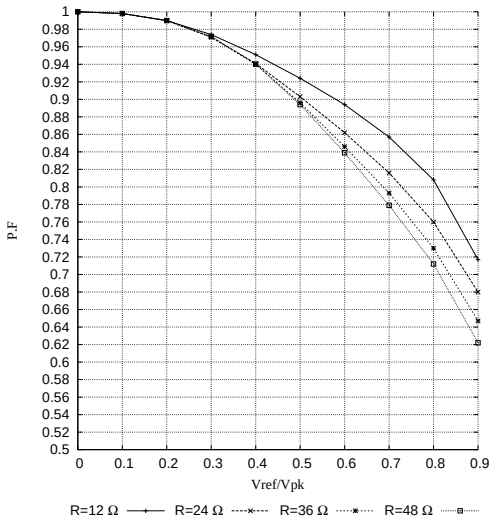


Fig. 11. The Power Factor vs The Voltage Ratio

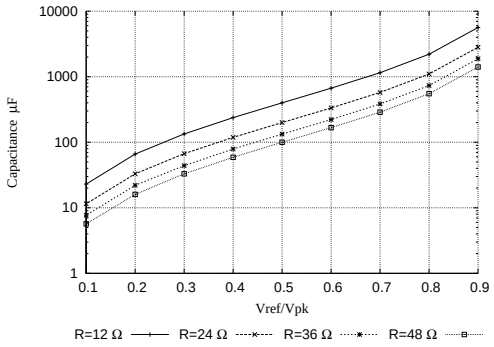


Fig. 12. The DC Side Capacitor Size vs The Voltage Ratio

value of DC reference level. Woodward's notation is used to represent the line current in the harmonics analysis of the AC side of the rectifier. The analysis showed a low harmonics contents of the main current with low THD. The performance of the proposed technique showed that the best results can be obtained from this rectifier with a lower values of the Voltage Ratio (V_{ref}/V_{pk}). This is very desirable for a wide variety of applications.

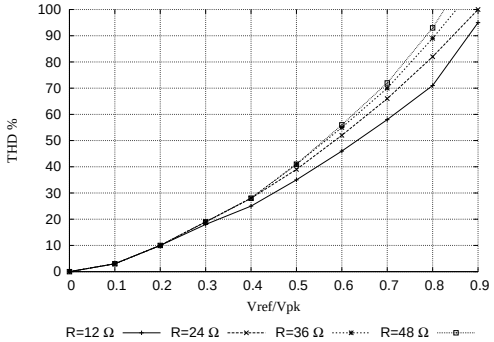


Fig. 13. The THD vs The Voltage Ratio

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REFERENCES

[1] A. Mansoor, W. Grady, R. Thallam, M. Doyle, S. Krein, and M. Samotyj, "Effect of supply voltage harmonics on the input current of single-phase diode bridge rectifier loads," *Power Delivery, IEEE Transactions on*, vol. 10, no. 3, pp. 1416 –1422, jul 1995.

[2] M. Khan, A. Pavel, M. Khan, and M. Choudhury, "Design of a single phase rectifier with switching on ac side for high power factor and low total harmonic distortion," in *Region 5 Technical Conference, 2007 IEEE*, april 2007, pp. 289 –292.

[3] A. Prasad, P. Ziogas, and S. Manias, "A novel passive waveshaping method for single-phase diode rectifiers," *Industrial Electronics, IEEE Transactions on*, vol. 37, no. 6, pp. 521 –530, dec 1990.

[4] L. Moran, L. Dixon, and R. Wallace, "A three-phase active power filter operating with fixed switching frequency for reactive power and current harmonic compensation," *Industrial Electronics, IEEE Transactions on*, vol. 42, no. 4, pp. 402–408, 1995.

[5] S. Sahoo and H. Jariwala, "A new power factor correction technique using pfc boost converter," in *Environment and Electrical Engineering (EEEIC), 2012 11th International Conference on*, may 2012, pp. 819 –823.

[6] N. Hamzah, M. Hamzah, A. Hasim, and N. Rahman, "Single-phase shunt active power filter using single-switch incorporating boost circuit," in *Power and Energy Conference, 2008. PECon 2008. IEEE 2nd International*, dec. 2008, pp. 1112 –1117.

[7] A. Hasim and M. Hamzah, "Single-phase shunt active power filter using boost rectifier technique," in *Electric Machines Drives Conference, 2007. IEMDC '07. IEEE International*, vol. 2, may 2007, pp. 1294 –1299.

[8] S. Pini and I. Barbi, "A single-phase high-power-factor rectifier, based on a two-quadrant shunt active filter," *Power Electronics, IEEE Transactions on*, vol. 26, no. 11, pp. 3131–3143, 2011.

[9] H. Fujita, "A single-phase active filter using an h-bridge pwm converter with a sampling frequency quadruple of the switching frequency," *Power Electronics, IEEE Transactions on*, vol. 24, no. 4, pp. 934–941, 2009.

[10] B. Han, "Single-phase active power filter using fft with harmonic phase-delay compensation," in *Power Energy Society General Meeting, 2009. PES '09. IEEE*, 2009, pp. 1–6.

[11] P. Kanjiya, V. Khadkikar, and H. Zeineldin, "Achieving maximum possible power factor with single-phase shunt active power filter under distorted supply condition," in *Power India Conference, 2012 IEEE Fifth*, 2012, pp. 1–6.

[12] G. Mishra and S. Gopalakrishna, "Design of passive high pass filter for shunt active power filter application," in *Circuits, Power and Computing Technologies (ICCPCT), 2013 International Conference on*, 2013, pp. 17–21.

[13] J. Lam and P. Jain, "A new passive valley fill dimming electronic ballast with extended line current conduction angle," in *Telecommunications Energy Conference, 2006. INTELEC '06. 28th Annual International*, 2006, pp. 1–7.

[14] J. Lam, S. Pan, and P. Jain, "A single switch valley-fill power factor corrected electronic ballast for compact fluorescent lightings with improved lamp current crest factor," pp. 1–1, 2013.

[15] J. Lam and P. Jain, "A modified valley fill electronic ballast having a current source resonant inverter with improved line-current total harmonic distortion (thd), high power factor, and low lamp crest factor," *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 3, pp. 1147–1159, 2008.

[16] S. Al-Zubaidi, M. Z. Ahmed, and P. Davey, "Design of single bidirectional switch single phase rectifier with reduced size dc side capacitor," in *Future Energy Electronics Conference (IFEEC), 2013 1st International*, 2013, pp. 18–23.

[17] P. Woodward and I. Davies, "Information theory and inverse probability in telecommunication," *Proceedings of the IEE - Part III: Radio and Communication Engineering*, vol. 99, no. 58, pp. 37–44, 1952.

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A Novel Buck-Boost DC-DC Converter Using Close-Coupled Inductors

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A Novel Buck-Boost DC-DC Converter Using Close-Coupled Inductors

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***Abstract*—A new step-up-down DC-DC converter architecture is proposed, which utilises the close inversely-coupled inductors topology in both its conversion stages (bucking and boosting stages). The new converter aims to reduce the switching noise by reducing the back e.m.f induced in the main inductor by maintaining a continuous current through it and delivered to the load. This results in an increase in a conversion efficiency for this kind of converter dealing with wide range of supply voltages and serves a wide variety of applications. Circuit configuration, principles of operation, transfer function, simulated results and the experimental results are presented. The proposed concept is verified by the experimental results of a range of cases studies.**

***Index Terms*—buck-boost converter; coupled-inductors; back e.m.f; CCM continuous conduction mode.**

I. INTRODUCTION

The use of conventional buck and boost circuits is usually accompanied by significant switching noise through switching transient in turn produces a voltage stress on the power switches of these circuits. The noise is a result of the back e.m.f induced in the coils of the buck and boost circuits, which is a consequences of discontinuous current in these coils during the switching transient. This e.m.f is a function of many factors like the coil size, load current and the switching frequency.

Coupled inductors considered a key solution to so many issues in DC-DC converter circuits. The control of the diode current falling rate; the diode reverse-recovery alleviation; the employing of the coupled inductors to operate in transformer mode to avoid the extreme duty cycle and to reduce the current ripple in high step-up or step-down conversion are some of these utilisation. [1].

Coupled inductors topology is a sort of special purposes transformers. Depending on the way that coupled inductor be implemented, there are various models of them. Directly or inversely coupled; loosely or interleaved and if they been on two magnetic cores or combining on the same magnetic component are some of these ways to implement the coupled inductors. The characteristics and the performance for each one of these models are different. It is valuable to have a look to the characteristics analysis and the performance evaluation for these various models of coupled inductors. A valuable studies have been made in these fields [2]–[5]. this research covered lots of these enquires and provided a comprehensive analysis about the subject.

Weinberg boost converter is presented in [6], this converter can offer a continuous output current with small current ripple. As a consequences of that a low switching losses and high efficiency converter obtained.

Close-coupled inductors topology can achieve a higher power density with reduced size, weight and losses in the magnetic components. These features are very desirable in electrical transport applications such as electric vehicles and railway traction [7]–[9].

The adoption of the integrating magnetic structure in a single core for the coupled inductors enables further reduction in the overall volume, weight and the copper usage of the magnetic components [10]–[12].

High step-up converter can be implemented by combining a charge pump capacitor with the coupled inductors. The voltage gain can be significantly increased and the turn ratio of the coupled inductor can be reduced [13]–[17]. High voltage gain converters are widely employed in many applications such a photovoltaic systems, fuel cell systems and electric vehicles. The voltage gain can be more extended with voltage doubler cells and diode-capacitor techniques combined with the coupled inductors. Different circuit configurations and designs are presented in [18]–[20].

The voltage stress of power switches and diodes can be reduced by adding a passive clamp circuits [21]–[23]. An active clamp circuit can be used for this purpose with a zero-voltage switching (ZVS) to avoid an extra switching loss as in [24]. ZVS technique can be also implemented to drive the power switch of boost converter which utilises coupled inductors topology [25].

II. THE PROPOSED BUCK-BOOST CONVERTER

A. Circuit Configuration

The circuit configuration of the proposed buck-boost converter is depicted in figure 1. The whole circuit can be represented as two phases or stages. The first phase is the buck stage which consists of the power switch S_1, the inductors L_{p1}, L_{s1} which they are inversely coupled inductors on the same ferrite core (primary and secondary windings of transformer T_1), input capacitor C_i, diodes D_1, D_2 and the main inductor L_2.

The boost phase follows the buck stage and therefore the two stages shared the main inductors L_2 and the diode D_2. The rest of the boost stage are the inductors L_{p3}, L_{s3} which they are also inversely coupled on the same core (primary and secondary windings of transformer T_3), power switch S_2, diodes D_3, D_4 and the output filter capacitor C_o.

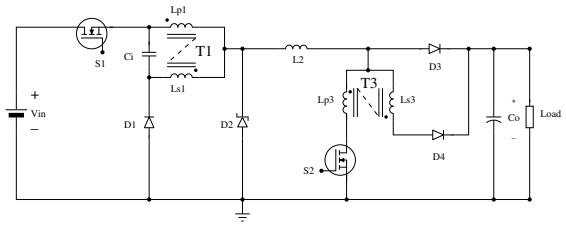

Fig. 1. The Circuit Configuration of the Proposed Converter

B. Principles of Operation

Depending on the applied sets of the duty cycles for the power switches S_1, S_2, the proposed converter can work as just a buck, boost or buck-boost converter.

The operating principles for buck-boost operation in continuous-conduction mode (CCM) is only discussed in this section. In order to clearly illustrate the principles of operation for the proposed converter, the following assumption have been made:

- The parasitic resistance and capacitance of all diodes and power switches are neglected.
- The parasitic resistance and capacitance of all passive components are neglected.
- The turn ratio n of the coupled inductors windings (transformers T_1, T_3) is unity.
- The leakage inductance of the coupled inductors and the main inductor are neglected.
- The magnetising inductance of the coupled inductors for both transformers have been integrated to the primary winding.

The circuit analysis can be simplified by representing the complete converter circuit as two sub-circuits or two stages. The first stage is the buck stage, the second is the boost stage. The circuits for buck and boost stages are shown in figures 2, 3 respectively.

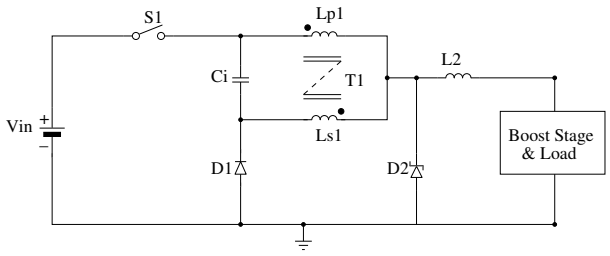

Fig. 2. The Buck Stage of the Proposed Converter

Buck stage : The buck stage is shown in figure 2, in this stage there are two states:

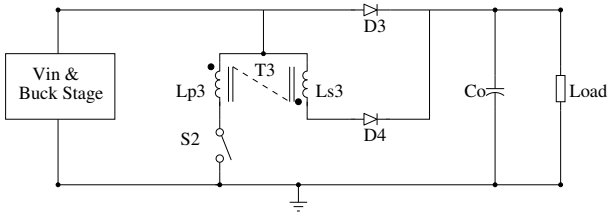

Fig. 3. The Boost Stage of the Proposed Converter

– On state, [S_1 on, D_1, D_2 off]: When the switch S_1 is turned on, the energy starts flowing through the primary winding of the coupled inductors L_{p1}, in the meanwhile the capacitor Ci provides a parallel path for energy to flow into the secondary winding of the coupled inductors L_{s1}. Both energy paths are merged together in the common point of the coupled inductor just at the main inductor L_2. As a consequences both diodes D_1 and D_2 are now off. Some energy is stored in both sides of the coupled inductors and the capacitor Ci. The equivalent circuit of this case with all currents paths is shown in figure 4. The current of the main inductor L_2 is the sum of the both sides of the coupled inductors currents.

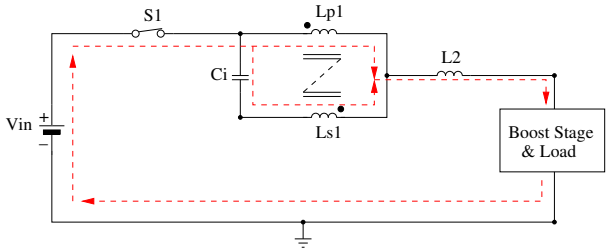

Fig. 4. On State of Buck Stage

– Off state, [S_1 off, D_1, D_2 on]: Once the switch S_1 is going to switch off, the energy releasing process is started. The capacitor Ci starts discharging it's energy instantaneously to the primary winding L_{p1}. The secondary winding L_{s1} releasing it's energy to the capacitor Ci, whilst the primary winding released some of the stored energy to the main inductor L_2. The time constant of discharging the capacitor is crucial to avoid any discontinuity of the current flowing to the primary winding L_{p1}. The capacitor in this case is much faster than any particular diode available to overcome the problem of delay in conduction due to the required conduction time by any used diode. Once the diode D_1 starts conduct it will provides with the capacitor Ci an additional path for current to flow alongside with the current path of the schottky diode D_2.
The equivalent circuit of this case with all currents paths is shown in figure 5. The current of the main inductor L_2 is the sum of both diodes currents D_1 and D_2. This arrangement ensure a continuous current

flowing in the coupled inductors and delivered to the main inductor even with off time of the duty cycle. As a results there is very small effect of the back e.m.f on the couple inductors and the main inductor L_2 of the buck stage. All actual currents waveforms are presented in V.

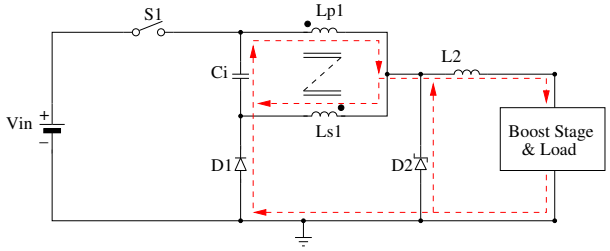

Fig. 5. Off State of Buck Stage

Boost stage : The boost stage is shown in figure 3. The output voltage and current of the buck stage now becomes the source of this stage. this stage also has two states:

– On state, [S_2, D_4 on, D_3 off]:
When the switch S_2 is turned on, the main current which is the output current of the buck stage will split into two. This is due to the effect of the transformer T_3 (the coupled inductors). The currents in both the primary winding L_{p3} and the secondary winding L_{s3} have the same magnitude. Once the voltage on the anode of the diode D_4 is equal to the output voltage, this diode becomes forwards biased. The secondary winding of the transformer T_3 now provides a path for energy to flow into the load side through D_4. This results in diode D_3 being turned off as the output voltage is now applied on it's cathode. The equivalent circuit of this case with all currents paths is clearly illustrated in figure 6.

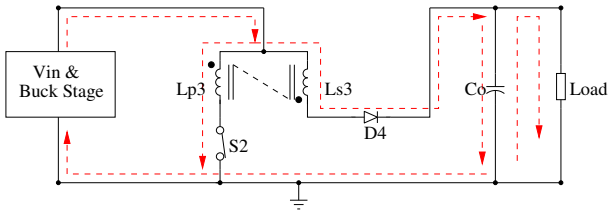

Fig. 6. On State of Boost Stage

– Off state, [S_2, D_4 off, D_3 on]:
When the switch S_2 is turned off, the diode D_3 becomes forwards biased once the voltage on it's anode is equal to the output voltage. The main current then goes directly to the load side through D_3. The output voltage is now applied on the cathode of diode D_4 which results in D_4 being turned off. The equivalent circuit of this case with all currents paths is shown in figure 7.

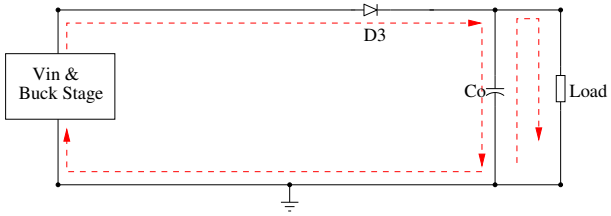

Fig. 7. Off State of Boost Stage

III. TRANSFER FUNCTION

This converter can work as just a buck, boost, or buck-boost converter depending on the applied set of the duty cycles for switches S_1 and S_2. The Transfer function of the buck-boost converter at steady state condition and CCM of operation is presented here. It can be derived by getting the rate of change of the converter current in four different cases. The converter current means the current flowing in the main inductor i_{L_2}.

These cases represents the logical probabilities of both power switches S_1 and S_2. By returning to the full circuit diagram of the proposed converter in figure 1, the four statuses can be described as follows

Starting with the definitions of the key variables in this derivation:

i_{max} is the maximum value of i_{L_2},
i_{min} is the minimum value of i_{L_2},
α, β are intermediate values of i_{L_2},
$\alpha > i_{min}$, $\beta < i_{max}$,
t_1 is the time duration of case 1,
t_2 is the time duration of case 2,
t_3 is the time duration of case 3,
t_4 is the time duration of case 4,
$t_1 + t_2 + t_3 + t_4 = T$,
T is the full time period of one frequency cycle.

- Case 1: [S_1: On, S_2: Off, $0 < t \leq t_1$],
When the switch S_1 is turned on during this period, the supply voltage is connected to the buck stage. Diodes D_1, D_2 and D_4 are all being turned off, while diode D_3 is being forwards biased. The input current here is equal to the output current.

$$i_{in} = i_{L_2} \tag{1}$$

$$V_{L2} = V_{in} - V_{out} = L_2 \frac{di_{in}}{dt} \tag{2}$$

$$L_2 \frac{di_{in}}{dt} = L_2 \frac{(\alpha - i_{min})}{t_1} \tag{3}$$

$$V_{in} - V_{out} = L_2 \frac{(\alpha - i_{min})}{t_1} \tag{4}$$

Where, i_{in} is the input current, V_{in} is the supply voltage, V_{out} is the output voltage, V_{L2} is the voltage across the main inductor L_2.

- Case 2: [S_1: On, S_2: On, $t_1 < t \leq t_2$],

When switches S_1 and S_2 are both turned on during this period, both the supply voltage and the boost stage are being connected. Due to the effect of the transformer T_3, the input current to the boost stage is splitted into two currents with the same magnitude. Diode D_4 is being forwards biased, while diodes D_1, D_2 and D_3 is are all being turned off during the period of case 2.

$$i_{in} = i_{L_2} \tag{5}$$

$$V_{L2} = V_{in} - \frac{V_{out}}{2} = L_2 \ \frac{di_{in}}{dt} \tag{6}$$

$$L_2 \ \frac{di_{in}}{dt} = L_2 \ \frac{(i_{max} - \alpha)}{t_2} \tag{7}$$

$$V_{in} - \frac{V_{out}}{2} = L_2 \ \frac{(i_{max} - \alpha)}{t_2} \tag{8}$$

- Case 3: [S_1: Off, S_2: On, $t_2 < t \leq t_3$],
When the switch S_1 is turned off during this period, the supply voltage is being disconnected from the the buck stage, while diodes D_1, D_2 are being forwards biased. The boost stage here is still connected as the status of switch S_2 would not change during this period. The situation of diodes D_3 and D_4 are also still unchanged during case 3.

$$i_{in} = i_{L_2} \tag{9}$$

$$V_{L2} = \frac{V_{out}}{2} = L_2 \ \frac{di_{in}}{dt} \tag{10}$$

$$L_2 \ \frac{di_{in}}{dt} = L_2 \ \frac{(i_{max} - \beta)}{t_3} \tag{11}$$

$$\frac{V_{out}}{2} = L_2 \ \frac{(i_{max} - \beta)}{t_3} \tag{12}$$

- Case 4: [S_1: Off, S_2 : Off, $t_3 < t \leq t_4$],
During this case, both the supply voltage and the boost stage are being disconnected. Diodes D_1, D_2 and D_3 are all being forwards biased, while diode D_4 is being reverse biased. The input current here is equal to the output current.

$$i_{in} = i_{L_2} \tag{13}$$

$$V_{L2} = V_{out} = L_2 \ \frac{di_{in}}{dt} \tag{14}$$

$$L_2 \ \frac{di_{in}}{dt} = L_2 \ \frac{(\beta - i_{min})}{t_4} \tag{15}$$

$$V_{out} = L_2 \ \frac{(\beta - i_{min})}{t_4} \tag{16}$$

For steady state condition with (CCM) of operation, the rise in current during case 1 and case 2 should equal the fall in current during case 3 and case 4.

$$[(\alpha - i_{min}) + (i_{max} - \alpha)] \ L_2 = [(i_{max} - \beta) + (\beta - i_{min})] \ L_2 \tag{17}$$

Dividing both sides of (17) by L_2 and by substitution in (4), (8), (12) and (16), the equation of (17) can be formulated as follow

$$\left[(V_{in} - V_{out}) \ t_1 + (V_{in} - \frac{V_{out}}{2}) \ t_2\right] = \left[(\frac{V_{out}}{2}) \ t_3 + (V_{out}) \ t_4\right] \tag{18}$$

Then,

$$(t_1 + t_2) \ V_{in} = \left[(t_1 + t_4) + \frac{1}{2}(t_2 + t_3)\right] \ V_{out} \tag{19}$$

Defining:
D_1, D_2 are the duty cycles of switches S_1, S_2 respectively, D_1, D_2 can be expressed as below

$$D_1 = \frac{(t_1 + t_2)}{(t_1 + t_2 + t_3 + t_4)} \tag{20}$$

$$D_2 = \frac{(t_2 + t_3)}{(t_1 + t_2 + t_3 + t_4)} \tag{21}$$

And,

$$(1 - D_2) = \frac{(t_1 + t_4)}{(t_1 + t_2 + t_3 + t_4)} \tag{22}$$

By Substitution of (20), (21) and (22) in (19)

$$D_1 \ V_{in} = (1 - D_2 + \frac{1}{2}D_2) \ V_{out} \tag{23}$$

The overall duty cycle of the proposed buck-boost converter can be expressed as in (24).

$$\frac{V_{out}}{V_{in}} = \frac{D_1}{(1 - \frac{D_2}{2})} \tag{24}$$

IV. EXPERIMENTAL SETUP

The prototype circuit of the new converter has been fabricated and tested. The practical results of buck-boost operation only is presented in this section. A single control circuit has been used to generate two different control signals used to fire two MOSFET driver circuits. Two N-channel MOSFETs have been used as switching devices S_1 and S_2 with high-side MOSFET driver to drive them. The function of the control circuit is to generate different sets of duty cycles D_1 and D_2. The sets started from 5% for both duty cycles and end up with 90% for the buck and 80% for the boost, step by 5% or 10%. A full range of the boost duty cycle (from 5% up to 80%) for each step of top-up for the buck duty cycle have been undertaken. This is to ensure a comprehensive understanding to the performance of the proposed converter. The parameters values of the converter circuit used in this experimental set-up are presented in table I.

TABLE I
EXPERIMENTAL SET-UP PARAMETERS

Parameter	Value
L_{p1}, L_{s1}	$98\mu H$
L_{p3}, L_{s3}	$234\mu H$
L_2	$3.54mH$
C_i	$4.8\mu F$
C_o	$112\mu F$

V. EXPERIMENTAL RESULTS OF CASE STUDY

In order to clarify the practical current waveforms of the proposed converter and to verify the principles of operation mentioned in II-B, a full case study is presented in this section. The applied supply voltage, duty cycles of switches S_1, S_2 and the applied load is presented in table II. The same values of parameters of the the converter circuit presented in table I have been used in this case study.

TABLE II
CASE STUDY TESTING CONDITIONS

Parameter	Value
V_{in}	$14V$
D_1	50%
D_2	50%
R_{load}	11Ω

In order to facilitate the follow up of energy flow process and currents distribution in the circuit, a full converter circuit diagram with all currents paths (with red arrows) are shown in figure 8.

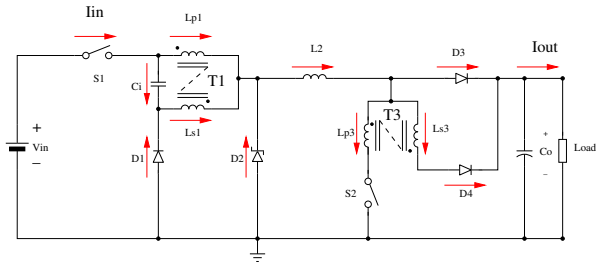

Fig. 8. The Circuit Configuration of the Proposed Converter

The experimental currents waveforms of the buck stage are shown in figures 9, 10 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure 11, while the current waveforms of the boost stage and the output current are all shown in figure 12. The measured efficiency for this particular case is 95.6%.

VI. SIMULATED RESULTS OF CASE STUDY

A simulation model for the circuit configuration of the new converter has been done using LT spice IV 4.22. The same design parameters of the prototype circuit have been used and the same testing conditions have been applied during the simulation of this model. The only difference is the current sensors are never been used in this model, current sensors

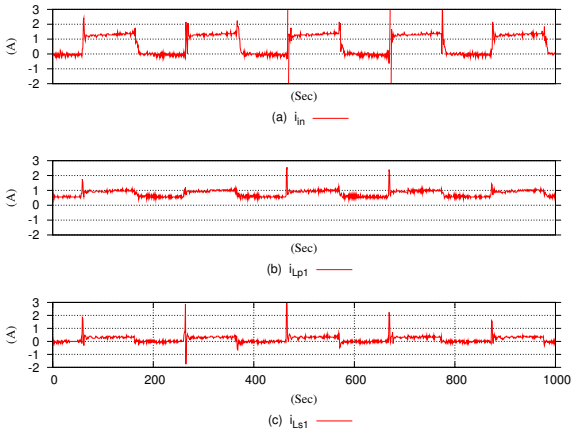

Fig. 9. Experimental Current Waveforms of Buck Stage: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

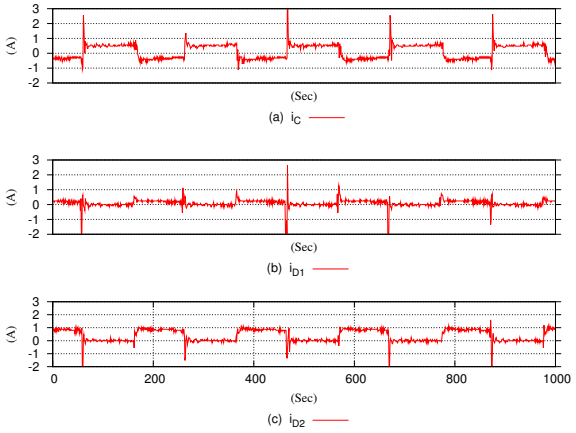

Fig. 10. Experimental Current Waveforms of Buck Stage: (a) capacitor C_i current, (b) diode current D_1, (c) diode current D_2,

are necessary in the prototype circuit in order to capture the current waveforms. This result in a slim margin between the practical and the simulated results.

The simulated results of the same case study presented in V is presented in this section. Figures 13, 14, 15 and 16 are the simulated currents waveforms of this case study. It is clear that the simulated results are in accordance with practical results and highly compatible.

VII. EXPERIMENTAL RESULTS AND DISCUSSION

The practical results of a range of cases (using 7 V input and a 22Ω load, 14 V input and a 44Ω, and 20 V input with 66Ω) at 100 KHz switching frequency is presented in figure 17. A full range of duty cycle sets for S_1 and S_2 as mentioned in IV has been used for each of these cases. The results confirm the validity of (24). The y axis represents the ratio $y = \frac{V_{out}}{V_{in}}$,

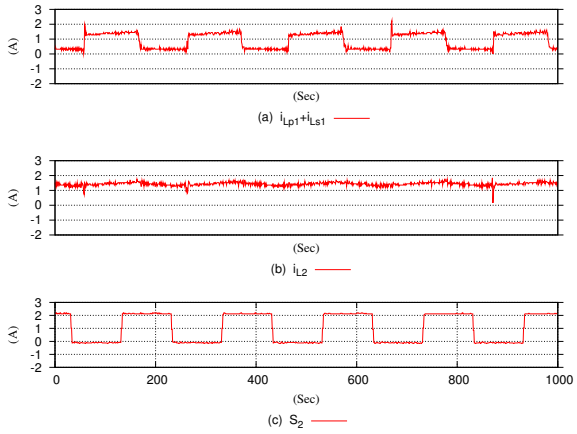

Fig. 11. Experimental Current Waveforms of Boost Stage: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

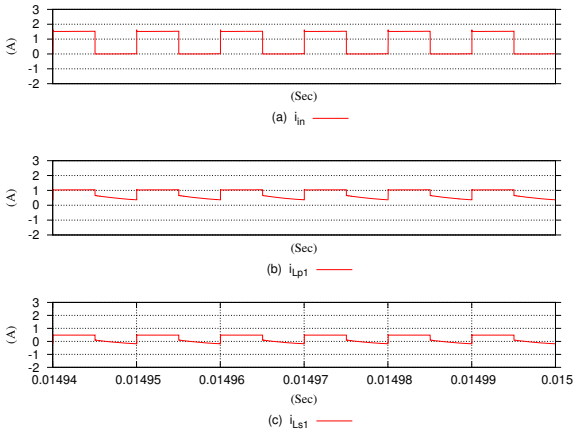

Fig. 13. Simulated Current Waveforms of Buck Stage: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

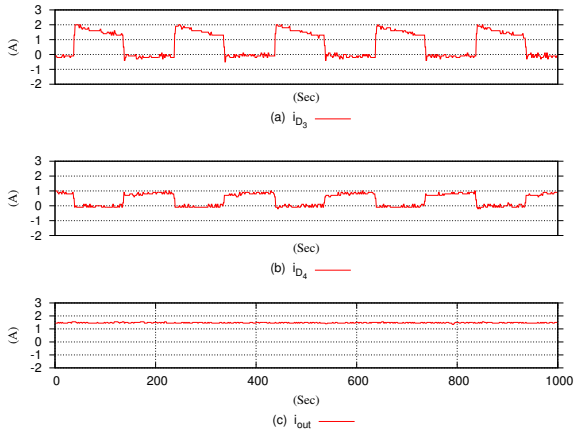

Fig. 12. Experimental Current Waveforms of Boost Stage: (a) diode current D_3, (c) diode current D_4, (d) output current i_{out}

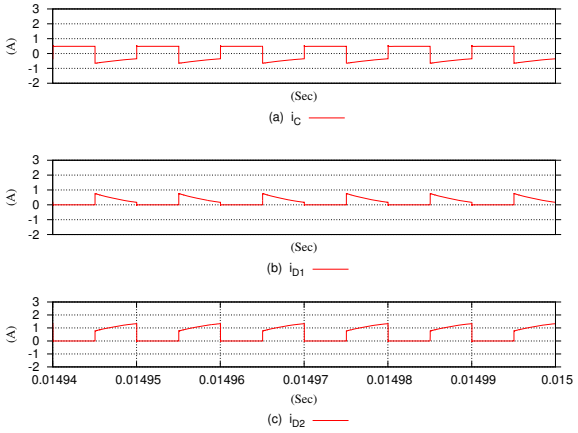

Fig. 14. Simulated Current Waveforms of Buck Stage: (a) capacitor C_i current, (b) diode current D_1, (c) diode current D_2,

whereas the x axis is the duty cycle. For clarity the line $y = x$, which represent (24) is also provided.

Figure 17 show clearly the linearity performance of the proposed system and how it works with a variety of duty cycles and loading conditions. Also it shows there is very small deviation in some tests points from the equality line of the analytical derived duty cycle. This deviation being more noticeable when the duty cycle of the boost switch S_2 skips the value of 50%. The results verified the compatibility between the analytical and practical results of the proposed converter. It also can be considered as a good indicator for the slim rate of noise and losses in this circuit.

The efficiency measurements for a selected case study from the above three cases (using 20 V input and a 66Ω load) have been done. The measured efficiency curve for this case under various output power is shown in figure 18.

VIII. The Transient Response

Figures 19, 20, are the turn On and the turn Off transient response of the proposed converter respectively. The same parameters values of table I have been used. The input voltage of 20 V and a load 66Ω at 100 KHz switching frequency with 30% duty cycle for both switches have been applied. It is clear that this topology has little or no transient overshoot even while switching at constant duty cycles and at a fixed switching frequency.

IX. Conclusion

This paper presents a new buck-boost architecture with its transfer function. This converter utilises close inversely-coupled inductors topology in both its conversion stages (buck

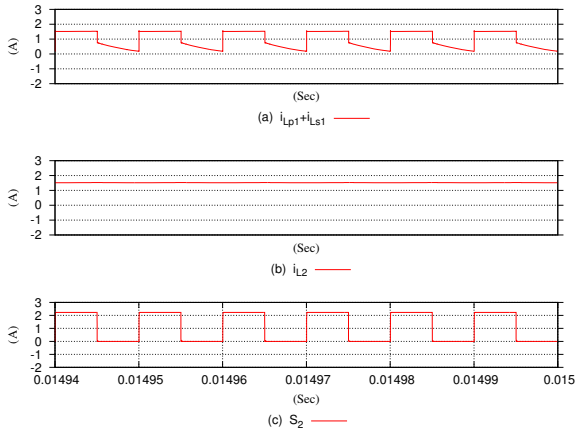

Fig. 15. Simulated Current Waveforms of Boost Stage: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

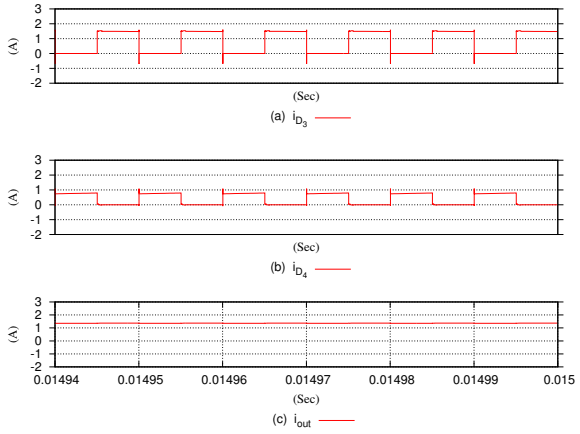

Fig. 16. Simulated Current Waveforms of Boost Stage: (a) diode current D_3, (c) diode current D_4, (d) output current i_{out}

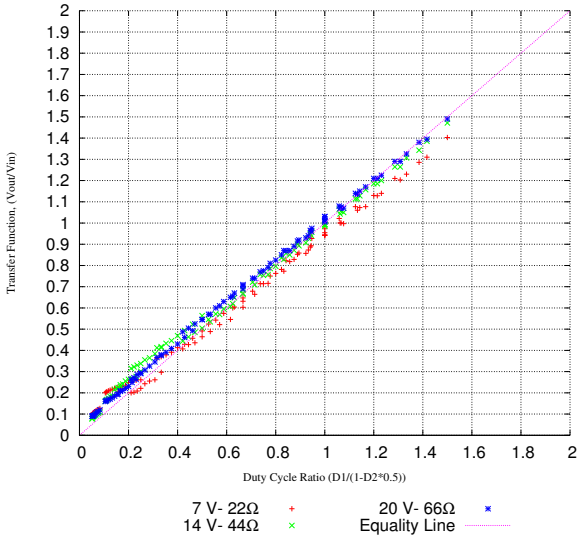

Fig. 17. Experimental Results

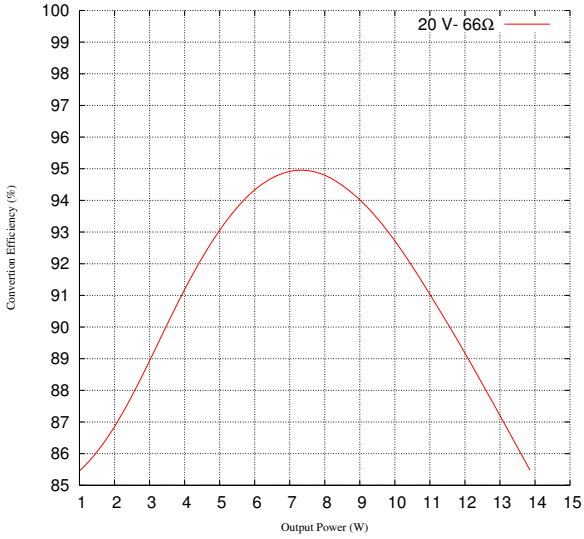

Fig. 18. Measured Efficiency Versus Output Power

and boost). It benefited from this topology in two different ways.

In the buck stage, this topology with additional passive component (capacitor) connected across the free terminals of coupled inductors can work as an ideal diode. This ensure a continuous current flow in this stage even with the off time of the buck switch S_1. This can be done by releasing and then recycling some of the stored energy in passive components of this configuration. The close coupled inductors arrangement also can be utilised in the boost stage to ensure a continuous output current by providing an alternative (parallel) path for energy to flow during the on time of boost switch.

The new topology strongly reduce the noise and thus the losses that usually accompanies the conventional buck and boost circuits. This result in an increase in the conversion efficiency of this kind of converters dealing with wide range of supply voltages and serves a wide variety of applications. It also provides a significant reduction in the voltage stress on the power switches.

This new architecture has little or no transient overshoot even while switching at constant duty cycles and at a fixed switching frequency.

The prototype circuit of the proposed converter has been fabricated and tested. The proposed architecture has been verified the simulated and the experimental results. The practical results confirmed the validity of the transfer function with a ranges of cases studies have been included in this work. The highest achieved efficiency observed in the experiments is 95.6% while the average efficiency for selected test points is 94.1%.

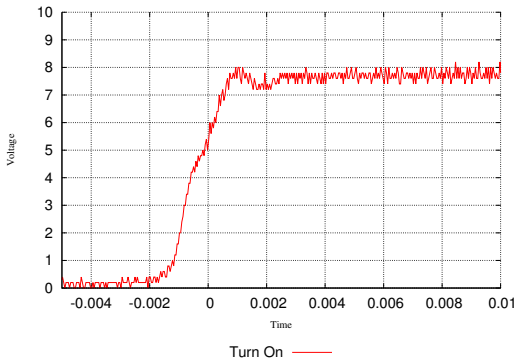

Fig. 19. Turn On Transient

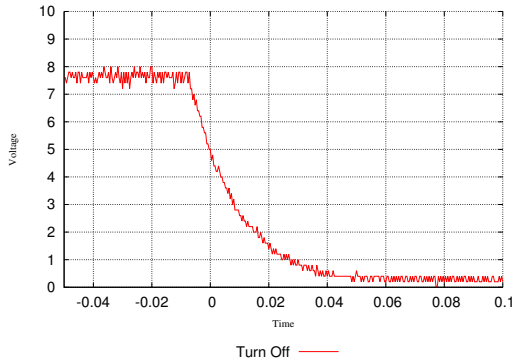

Fig. 20. Turn Off Transient

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REFERENCES

[1] Wuhua Li, Jianguo Xiao, Jiande Wu, Jun Liu, and Xiangning He. Application summarization of coupled inductors in dc/dc converters. In *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pages 1487–1491, Feb 2009.

[2] Guangyong Zhu, B. McDonald, and Kunrong Wang. Modeling and analysis of coupled inductors in power converters. *Power Electronics, IEEE Transactions on*, 26(5):1355–1363, May 2011.

[3] Po-Wa Lee, Y.-S. Lee, D.K.W. Cheng, and Xiu-Cheng Liu. Steady-state analysis of an interleaved boost converter with coupled inductors. *Industrial Electronics, IEEE Transactions on*, 47(4):787–795, Aug 2000.

[4] J. Imaoka, M. Yamamoto, K. Umetani, S. Arimura, and T. Hirano. Characteristics analysis and performance evaluation for interleaved boost converter with integrated winding coupled inductor. In *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, pages 3711–3718, Sept 2013.

[5] S. Kimura, J. Imaoka, and M. Yamamoto. Potential power analysis and evaluation for interleaved boost converter with close-coupled inductor. In *Power Electronics and Drive Systems (PEDS), 2013 IEEE 10th International Conference on*, pages 26–31, April 2013.

[6] A.K. Weinberg and P. Rueda Boldo. A high power, high frequency, dc to dc converter for space applications. In *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, pages 1140–1147 vol.2, Jun 1992.

[7] K. Martin, A. Rujas, I. Villar, I. Perez-de Arenaza, and I. Etxeberria-Otadui. Design of a 2.5kw pfc boost full-sic converter based on close-coupled inductors. In *Control and Modeling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on*, pages 1–7, June 2014.

[8] M. Hirakawa, Y. Watanabe, M. Nagano, K. Andoh, S. Nakatomi, S. Hashino, and T. Shimizu. High power dc/dc converter using extreme close-coupled inductors aimed for electric vehicles. In *Power Electronics Conference (IPEC), 2010 International*, pages 2941–2948, June 2010.

[9] M. Hirakawa, M. Nagano, Y. Watanabe, K. Andoh, S. Nakatomi, and S. Hashino. High power density dc/dc converter using the close-coupled inductors. In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pages 1760–1767, Sept 2009.

[10] Yanshen Hu, Yunxiang Xie, Huamin Xu, and Hao Tian. Design and implementation of two-channel interleaved boost converters with integrated coupling inductors. In *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, pages 625–630, Aug 2006.

[11] Fei Yang, Xinbo Ruan, Yang Yang, and Zhihong Ye. Design issues of interleaved critical conduction mode boost pfc converter with coupled inductor. In *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, pages 2245–2252, Sept 2010.

[12] Fei Yang, Xinbo Ruan, Yang Yang, and Zhihong Ye. Interleaved critical current mode boost pfc converter with coupled inductor. *Power Electronics, IEEE Transactions on*, 26(9):2404–2413, Sept 2011.

[13] S. Chen, M. Lao, Y. Shen, and T. Liang. A novel switched-coupled-inductor dc-dc step-up converter and its derivatives. *Industry Applications, IEEE Transactions on*, PP(99):1–1, 2014.

[14] K.I. Hwu, A.P. Tseng, and Jenn-Jong Shieh. High step-up converter based on multi-winding coupled inductor and charge pump capacitor. In *TENCON 2013 - 2013 IEEE Region 10 Conference (31194)*, pages 1–4, Oct 2013.

[15] K.I. Hwu and Y.T. Yau. Voltage-boosting converter based on charge pump and coupling inductor with passive voltage clamping. *Industrial Electronics, IEEE Transactions on*, 57(5):1719–1727, May 2010.

[16] Shih-Ming Chen, Tsorng-Juu Liang, Kai-Hui Chen, Man-Long Lao, and Yi-Chien Shen. A novel switched-coupled-inductor dc-dc step-up converter. In *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, pages 1830–1833, Sept 2013.

[17] Wensong Yu, C. Hutchens, Jih-Sheng Lai, Jianhui Zhang, G. Lisi, A. Djabbari, G. Smith, and T. Hegarty. High efficiency converter with charge pump and coupled inductor for wide input photovoltaic ac module applications. In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pages 3895–3900, Sept 2009.

[18] Xuefeng Hu and Chunying Gong. A high voltage gain dc-dc converter integrating coupled-inductor and diode-capacitor techniques. *Power Electronics, IEEE Transactions on*, 29(2):789–800, Feb 2014.

[19] Yi-Ping Hsieh, Jiann-Fuh Chen, Tsorng-Juu Liang, and Lung-Sheng Yang. Novel high step-up dc-dc converter with coupled-inductor and switched-capacitor techniques for a sustainable energy system. *Power Electronics, IEEE Transactions on*, 26(12):3481–3490, Dec 2011.

[20] Yi-Ping Hsieh, Jiann-Fuh Chen, Tsorng-Juu Liang, and Lung-Sheng Yang. A novel high step-up dc-dc converter for a microgrid system. *Power Electronics, IEEE Transactions on*, 26(4):1127–1136, April 2011.

[21] Tsai-Jie Lin, Jiann-Fuh Chen, and Yi-Ping Hsieh. A novel high step-up dc-dc converter with coupled-inductor. In *Future Energy Electronics Conference (IFEEC), 2013 1st International*, pages 777–782, Nov 2013.

[22] Rong-Jong Wai and Rou-Yong Duan. High step-up converter with coupled-inductor. *Power Electronics, IEEE Transactions on*, 20(5):1025–1035, Sept 2005.

[23] Moon-Hwan Keum, Yoon Choi, Sang-Kyoo Han, and Jeong il Kang. High efficiency voltage-clamped coupled-inductor boost converter. In *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, pages 828–833, Nov 2013.

[24] Tsai-Fu Wu, Yu-Sheng Lai, J.-C. Hung, and Yaow-Ming Chen. Boost converter with coupled inductors and buck-boost type of active clamp. *Industrial Electronics, IEEE Transactions on*, 55(1):154–162, Jan 2008.

[25] Xi Zhang, Lei Jiang, Junjun Deng, Siqi Li, and Zheng Chen. Analysis and design of a new soft-switching boost converter with a coupled inductor. *Power Electronics, IEEE Transactions on*, 29(8):4270–4277, Aug 2014.

[26] Mohammed Zaki Ahmed. Pb148498. *GB Patent*, 2014.

Appendix A

Woodward's notation and the Harmonic Analysis of the Conventional Single Phase Rectifier in Chapter 3

A.1 Woodward's notation.

The definitions of Woodward's notation is presented in the following formula:

$$\text{Rect}(t) = \mathcal{R}(t) = \begin{cases} 1 & -\frac{1}{2} < t < +\frac{1}{2} \\ \frac{1}{2} & t = \pm\frac{1}{2} \\ 0 & t < -\frac{1}{2} \text{ and } t > \frac{1}{2} \end{cases} \tag{A.1}$$

$$\text{Sinc}(f) = \mathcal{S}(f) = \begin{cases} \frac{\sin(\pi f)}{\pi f} & f \neq 0 \\ 1 & f = 0 \end{cases} \tag{A.2}$$

The Rect and Sinc waveform are shown in figures A.1, A.2 respectively.

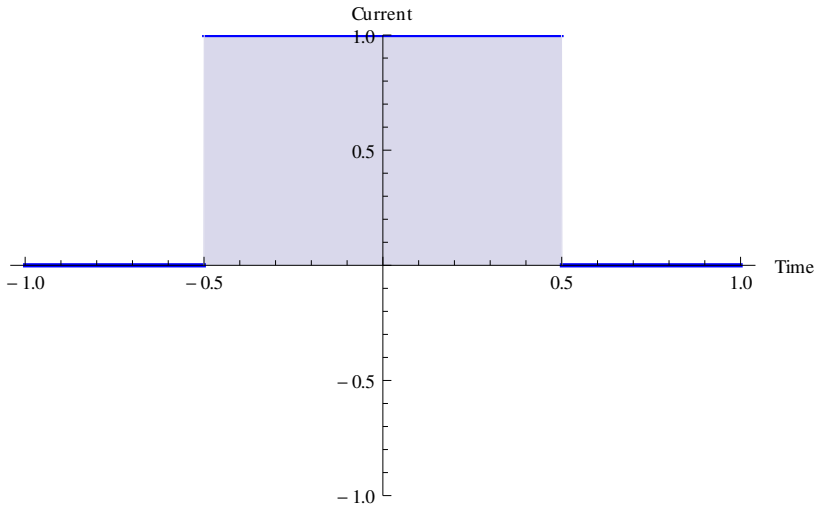

Figure A.1: The Rect Waveform

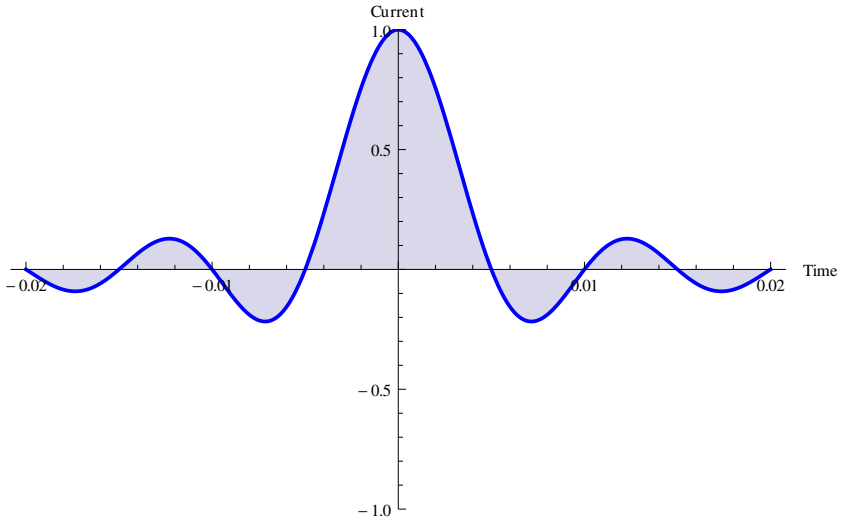

Figure A.2: The Sinc Waveform

The Fourier Transform of the Rect and Sinc pulse can then be expressed as follows

$$\text{Rect}(t) \quad \Leftrightarrow \quad \text{Sinc}(f) \tag{A.3}$$

$$\text{Rect}\left(\frac{t}{W}\right) \quad \Leftrightarrow \quad |W|\text{Sinc}(Wf) \tag{A.4}$$

$$\text{Rect}\left(\frac{t-a}{W}\right) \quad \Leftrightarrow \quad |W|\text{Sinc}(Wf)e^{-i2\pi af} \tag{A.5}$$

Where W is the pulse width in time, a is the pulse width centre in time, f is the frequency, i is the complex operator $i = \sqrt{-1}$.

A.2 Harmonic Analysis of the Conventional Single Phase Rectifier in Chapter 3

The analytical input current waveform of the conventional rectifier for the case study presented in 3.6.1, is shown in figure A.3.

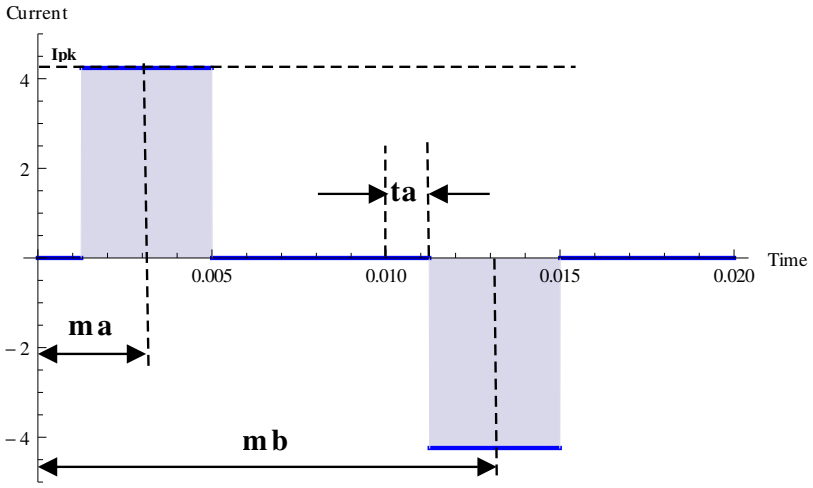

Figure A.3: Analytical Input Current Waveform of the Conventional Rectifier

In figure A.3, $I_{pk} = 4.24\ Amp.$, $\alpha = 21.6°$, $f = 50\ Hz$,

Starting with

$$t_a = \left[\left(\frac{\alpha}{90}\right)\left(\frac{1}{4\ f}\right)\right] \tag{A.6}$$

Defining

$$\mathcal{R}(t, a, W) = \text{Rect}\left[\frac{t-a}{W}\right] \tag{A.7}$$

$$\mathcal{S}(f, a, W) = |W|\ \text{Sinc}\ (Wf) \cdot e^{-i2\pi af} \tag{A.8}$$

And

$$m_a = \left(t_a + \frac{1}{4f}\right) 0.5 \tag{A.9}$$

$$m_b = \left(t_a + \frac{5}{4f}\right) 0.5 \tag{A.10}$$

$$\mathcal{W}_1 = \left(\frac{1}{4f} - t_a\right) \tag{A.11}$$

This then leads to the following expression for the current waveform shown in figure A.3 in the time domain,

$$i_1(t) = I_{pk} \left[\mathcal{R}\left(t, m_a, \mathcal{W}_1\right) - \mathcal{R}\left(t, m_b, \mathcal{W}_1\right)\right] \tag{A.12}$$

and the expression for the frequency domain spectra can then be obtained from inspection as

$$I_1(f) = I_{pk} \left[\mathcal{S}\left(f, m_a, \mathcal{W}_1\right) - \mathcal{S}\left(f, m_b, \mathcal{W}_1\right)\right] \tag{A.13}$$

Assuming the current is periodic, the spectral components at integer multiples of f are defined as

$$A(n) = \mathrm{Re}[I_1(fn)]2f \tag{A.14}$$

$$B(n) = -\,\mathrm{Im}[I_1(fn)]2f \tag{A.15}$$

where n is an integer, and this results in the following Fourier series expansion for $i_1(t, n)$

$$i_h(t, n) = [A(n)\cos(2\pi fnt) + B(n)\sin(2\pi fnt)] \tag{A.16}$$

Where i_h is the rms value of current of harmonic order n.

$$i_1(t, n) = \sum_{k=1}^{n} i_h(t, k) \tag{A.17}$$

The magnitude of spectral component at n is given by

$$S(n) = \sqrt{A(n)^2 + B(n)^2} \tag{A.18}$$

Appendix B

Wolfram Mathematica Codes

B.1 Inverse Laplace Transformation of the Rectifier Line Current in Chapter 3:

```
Simplify [
  InverseLaplaceTransform [(Vpk/Roe) * s * (2*Pi*f) / ((s+a) * (s^2 + ((2*Pi*f))^2)) -
      (V1 / Roe) / (s+a) + (Vpk/R) * (2*Pi*f) / (s^2 + (2*Pi*f)^2), s, t], t > 0]
```

$$\left(e^{-a t}\left(-R\left(a^2 V1 + 4 f^2 \pi^2 V1 + 2 a f \pi Vpk\right) + 2 a e^{a t} f \pi R Vpk \text{Cos}[2 f \pi t] + e^{a t}\left(a^2 Roe + 4 f^2 \pi^2 (R + Roe)\right) Vpk \text{Sin}[2 f \pi t]\right)\right) / \left(\left(a^2 + 4 f^2 \pi^2\right) R Roe\right)$$

```
InverseLaplaceTransform [(Vpk/Roe) * s * (2*Pi*f) / ((s+a) * (s^2 + ((2*Pi*f))^2)) -
    (V1 / Roe) / (s+a) + (Vpk/R) * (2*Pi*f) / (s^2 + (2*Pi*f)^2), s, t]
```

$$\frac{e^{-a t}\left(-a^2 V1 - 4 f^2 \pi^2 V1 - 2 a f \pi Vpk\right)}{\left(a^2 + 4 f^2 \pi^2\right) Roe} + \left(2 a f \pi R Vpk \text{Cos}[2 f \pi t] + 4 f^2 \pi^2 R Vpk \text{Sin}[2 f \pi t] + a^2 Roe Vpk \text{Sin}[2 f \pi t] + 4 f^2 \pi^2 Roe Vpk \text{Sin}[2 f \pi t]\right) / \left(\left(a^2 + 4 f^2 \pi^2\right) R Roe\right)$$

B.2 Performance Analysis of the Conventional Single Phase Rectifier Case Study in Chapter 3:

```
The voltage is (12 V) rms , the current is defined using a piecewise function.

v[t_] := 12 * Sqrt[2] * Sin[2 * Pi * 50 * t];
i[t_] := Piecewise[{{4.24, 1.2/1000 < t < 5/1000}, {-4.24,
  11.2/1000 < t < 15/1000}, {4.24, 21.2/1000 < t < 25/1000}, {-4.24,
  31.2/1000 < t < 35/1000}, {4.24, 41.2/1000 < t < 45/1000}}, 0];

The root mean squared value of the voltage waveform is computed
  after identifying the period of the squared voltage waveform ,
both voltage and voltage squared are plotted. The expression
  N[Vrms ] displays the Numerical value of Vrms .

Plot[v[x], {x, 0, 20/1000}, PlotStyle -> {Thick, Red},
 AxesLabel -> {Time , Voltage}]
Plot[{v[x] * v[x]}, {x, 0, 20/1000}, PlotStyle -> {Thick, Red},
 AxesLabel -> {Time , Squared Voltage}, Filling-> Axis]
T = 10/1000;
Vrms  = Sqrt[1/T * ∫_0^T v[x] * v[x] dx];
N[Vrms ]
```

The root mean squared value of the current waveform is computed
after identifying the period of the squared current waveform .

```
Plot[i[x], {x, 0, 50/1000}, PlotStyle -> {Thick, Blue},
 AxesLabel -> {Sec, Amps }, Filling-> Axis]
Plot[i[x]*i[x], {x, 0, 20/1000}, PlotStyle -> {Thick, Blue},
 AxesLabel -> {Sec, Amps }, PlotRange -> Full, Filling-> Axis]
T = 10/1000;
Irms  = Sqrt[1/T * ∫_0^T i[x]*i[x] dx];
N[Irms ]
```

The input current and voltage waveforms .

```
Plot[{v[x], i[x]}, {x, 0, 20/1000}, PlotStyle -> {Thick, Red},
 AxesLabel -> {Time , Voltage, Current}, Filling-> Axis]
```

The instantaneous power can be obtained using the voltage and current,
and from the RMS values of voltage and current,
and the average value of the instantaneous power waveform ,
the power factor of this power system can be evaluated. This power factor can
be further analysed into the Displacement factor and the Distortion factor.

```
Plot[{v[x]*i[x]}, {x, 0, 20/1000}, Filling-> Axis,
 PlotStyle -> {Thick, Blue}, AxesLabel -> {Sec, Watt}, PlotRange -> Full]

T = 10/1000;
Pav = 1/T * ∫_0^T v[x]*i[x] dx;
N[Pav]

pf = Pav/(Vrms *Irms );
N[pf]

DispFactor = Cos[FundamentalHarmonicAngle  /180*Pi];
N[DispFactor]

DistortionFactor= pf/DispFactor;
N[DistortionFactor]
```

The periodic current can be broken down into frequency components (or into its harmonics)
These components are computed using Woodward's notations as below

```
Ipk := 4.24
```

```
alpha := 21.6
f := 50
ta := (alpha/90) *1/(4*f)
sinc[x_] := Sinc[x*Pi]
rect[t_, a_, w_] := HeavisidePi[(t - a) /w];
mysinc [f_, a_, w_] := w*sinc[(f*w)] *E^(-I*2*Pi*a*f)
ma  := (ta + 1/(4*f)) *0.5
mb  := (ta + 5/(4*f)) *0.5
width := (1/(4*f) - ta)
ia[t_] := Ipk* (rect[t, ma , width] - rect[t, mb , width]);
Ia[f_] := Ipk* (mysinc [f, ma , width] - mysinc [f, mb , width])
A[n_] := Re[Ia[f*n]] *2*f
B[n_] := -1*Im [Ia[f*n]] *2*f

Plot[i[t], {t, 0, 1/f}, Filling-> Axis]
aexact = Table[A[x], {x, 0, 1000}];
bexact = Table[B[x], {x, 0, 1000}];

ListPlot[{Sqrt[aexact^2 + bexact^2]}, Filling-> Axis,
 PlotRange -> {{0, 40}, {0, 4.0}}, PlotStyle -> Blue]


HarmonicCurrent [t_, n_] :=
 aexact[[n + 1]] *Cos[2*Pi*50*n*t] + bexact[[n + 1]] *Sin[2*Pi*50*n*t];

iapprox[t_, n_] := Sum [HarmonicCurrent [t, k], {k, 1, n}];

Plot[iapprox[t, 1000], {t, 0, 1/f}]

Plot[{iapprox[t, 1], iapprox[t, 3], iapprox[t, 5], iapprox[t, 7],
 iapprox[t, 9], iapprox[t, 11], iapprox[t, 1000]}, {t, 0, 1/f}]
h := Sqrt[aexact^2 + bexact^2]
ListPlot[{h}, Filling-> Axis, PlotRange -> {{0, 40}, {0, 4.0}},
 PlotStyle -> Blue]

v[t_] := 12*Sqrt[2]*Sin[2*Pi*50*t];

Plot[Abs[Ia[f]], {f, 50, 1000}, PlotRange -> All]


Both voltage and the fundamental  current can be plotted together
  (with an amplitude  of 1) in order to see the displacement  angle between them
  as shown below. This angle in degrees is the FundamentalHarmonicAngle

FundamentalHarmonicAngle
Plot[{v[x] / (12*Sqrt[2]), iapprox[x, 1]/h[[2]]}, {x, 0, 20/1000}]
```

B.3 Performance Analysis of the Proposed Single Phase Rectifier Case Study in Chapter 3:

```
The voltage is (12 V) rms , the current is defined using a piecewise function.

v[t_] := 12 * Sqrt[2] * Sin[2 * Pi * 50 * t];
i[t_] := Piecewise[{{1.76, 1.25 / 1000 <= t <= 5 / 1000}, {1.28 * Sin[2 * Pi * 50 * t],
  5 / 1000 < t < 8.75 / 1000}, {-1.76,
  11.25 / 1000 <= t <= 15 / 1000}, {1.28 * Sin[2 * Pi * 50 * t],
  15 / 1000 < t <= 18.75 / 1000}, {1.76,
  21.25 / 1000 <= t <= 25 / 1000}, {1.28 * Sin[2 * Pi * 50 * t],
  25 / 1000 < t < 28.75 / 1000}, {-1.76,
  31.25 / 1000 <= t <= 35 / 1000}, {1.28 * Sin[2 * Pi * 50 * t],
  35 / 1000 < t <= 38.75 / 1000}, {1.76,
  41.25 / 1000 <= t <= 45 / 1000}, {1.28 * Sin[2 * Pi * 50 * t],
  45 / 1000 < t < 48.75 / 1000}}, 0];

The root mean squared value of the voltage waveform is computed after identifying
  the period of the squared voltage waveform . Both voltage and voltage squared
  are plotted. The expression N[Vrms ] displays the Numerical value of Vrms .

Plot[v[x], {x, 0, 20 / 1000}, PlotStyle -> {Thick, Red},
 AxesLabel -> {Time , Voltage}]
Plot[{v[x] * v[x]}, {x, 0, 20 / 1000}, PlotStyle -> {Thick, Red},
 AxesLabel -> {Time , Squared Voltage}]
T = 10 / 1000;
Vrms  = Sqrt[1 / T * ∫_0^T v[x] * v[x] dx];
N[Vrms ]

The root mean squared value of the current waveform is computed
  after identifying the period of the squared current waveform .

Plot[i[x], {x, 10 / 1000, 50 / 1000}, PlotStyle -> {Thick, Blue},
 AxesLabel -> {Sec, Amps }, PlotRange -> {-4.2, 4.2}, Filling-> Axis]
Plot[i[x] * i[x], {x, 0, 20 / 1000}, PlotStyle -> {Thick, Blue},
 AxesLabel -> {Sec, Amps }, PlotRange -> {0, 18}, Filling-> Axis]
T = 10 / 1000;
Irms  = Sqrt[1 / T * ∫_0^T i[x] * i[x] dx];
N[Irms ]

The input current and voltage waveforms .

Plot[{v[x], i[x]}, {x, 0, 20 / 1000}, PlotStyle -> {Thick, Red},
```

```
AxesLabel -> {Time , Voltage, Current}, Filling-> Axis]
```

The instantaneous power can be obtained using the voltage and current,
and from the RMS values of voltage and current,
and the average value of the instantaneous power waveform ,
the power factor of this power system can be evaluated. This power factor can
be further analysed into the Displacement factor and the Distortion factor.

```
Plot[{v[x] * i[x]}, {x, 0, 20 / 1000}, Filling-> Axis,
 PlotStyle -> {Thick, Blue}, AxesLabel -> {Sec, Watt}, PlotRange -> {0, 72}]

T = 10 / 1000;
Pav = 1 / T * ∫_0^T v[x] * i[x] dx;
N[Pav]


pf = Pav / (Vrms * Irms );
N[pf]



DispFactor = Cos[FundamentalHarmonicAngle * Pi / 180]
DistortionFactor= pf / DispFactor
```

The periodic current can be broken down into its
frequency components (or into its harmonics). These
components are computed using Woodward's notation as below

```
Ipk := 1.76
Ipksin := 1.28
alpha := 22.5
f := 50
ta := (alpha / 90) * 1 / (4 * f)
sinc[x_] := Sinc[x * Pi]
rect[t_, a_, w_] := HeavisidePi[(t - a) / w];

mysinc [f_, a_, w_] := w * sinc[(f * w)] * E^(-I * 2 * Pi * a * f)
newMySinc[f_, a_, w_, d_] :=
 w * sinc[(f + d) * w] * E^(-I * 2 * Pi * a * (f + d)) * I / 2 -
  w * sinc[(f - d) * w] * E^(-I * 2 * Pi * a * (f - d)) * I / 2;

ma  := (ta + 1 / (4 * f)) * 0.5
mb  := (ta + 5 / (4 * f)) * 0.5
```

```
width := (1/(4*f) - ta)
am  := 1/(4*f) + width/2
bm  := 3/(4*f) + width/2
ia[t_] := Ipk*(rect[t, ma , width] - rect[t, mb , width]) +
 Ipksin*Sin[2*Pi*f*t]*(rect[t, am , width] + rect[t, bm , width])
Plot[i[t], {t, 0, 1/f}]

Ia[f_] := Ipk*(mysinc [f, ma , width] - mysinc [f, mb , width]) +
 Ipksin*(newMySinc[f, am , width, 50] + newMySinc[f, bm , width, 50])
A[n_] := Re[Ia[f*n]]*2*f
B[n_] := -1*Im [Ia[f*n]]*2*f


aexact = Table[A[x], {x, 0, 1000}];
bexact = Table[B[x], {x, 0, 1000}];
ListPlot[{Sqrt[aexact^2 + bexact^2]}, Filling-> Axis,
 PlotRange -> {{0, 40}, {0, 4.0}}, PlotStyle -> Blue]

HarmonicCurrent [t_, n_] :=
 aexact[[n + 1]]*Cos[2*Pi*50*n*t] + bexact[[n + 1]]*Sin[2*Pi*50*n*t];

iapprox[t_, n_] := Sum [HarmonicCurrent [t, k], {k, 1, n}];


Plot[{iapprox[t, 1], iapprox[t, 3], iapprox[t, 5], iapprox[t, 7],
 iapprox[t, 9], iapprox[t, 1000], i[x]}, {t, 0, 1/f}]
h := Sqrt[aexact^2 + bexact^2]
ListPlot[{h}, Filling-> Axis, PlotRange -> {{0, 40}, {0, 4.0}},
 PlotStyle -> Blue]

Both voltage and the fundamental  current can be plotted together
  (with an amplitude of 1) in order to see the displacement  angle between them
  as shown below. This angle in degrees is the Fundamental  Harmonic Angle.

FundamentalHarmonicAngle
Cos[FundamentalHarmonicAngle  *Pi/180]
Plot[{v[x] / (12*Sqrt[2]), iapprox[x, 1]/h[[2]]}, {x, 0, 20/1000}]
```

Appendix C

The Layout of the Prototype Circuits in Chapter 3

The layout of the prototype circuit of the proposed single phase rectifier is shown in figure C.1.

The layout of the prototype circuit of the proposed control scheme for the new single phase rectifier system is shown in figure C.2.

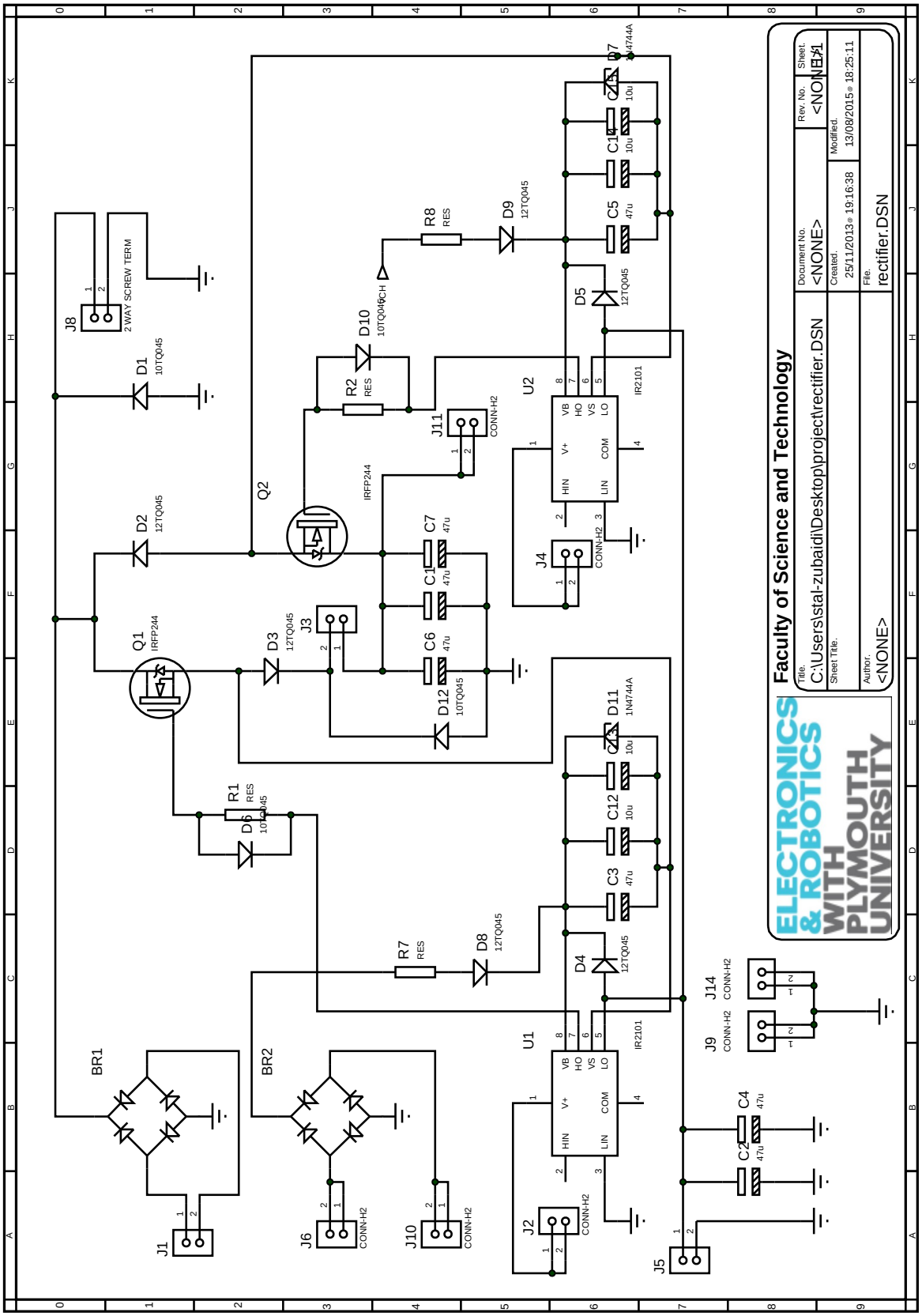

Figure C.1: The Layout of the Prototype Circuit of the Proposed Single Phase Rectifier

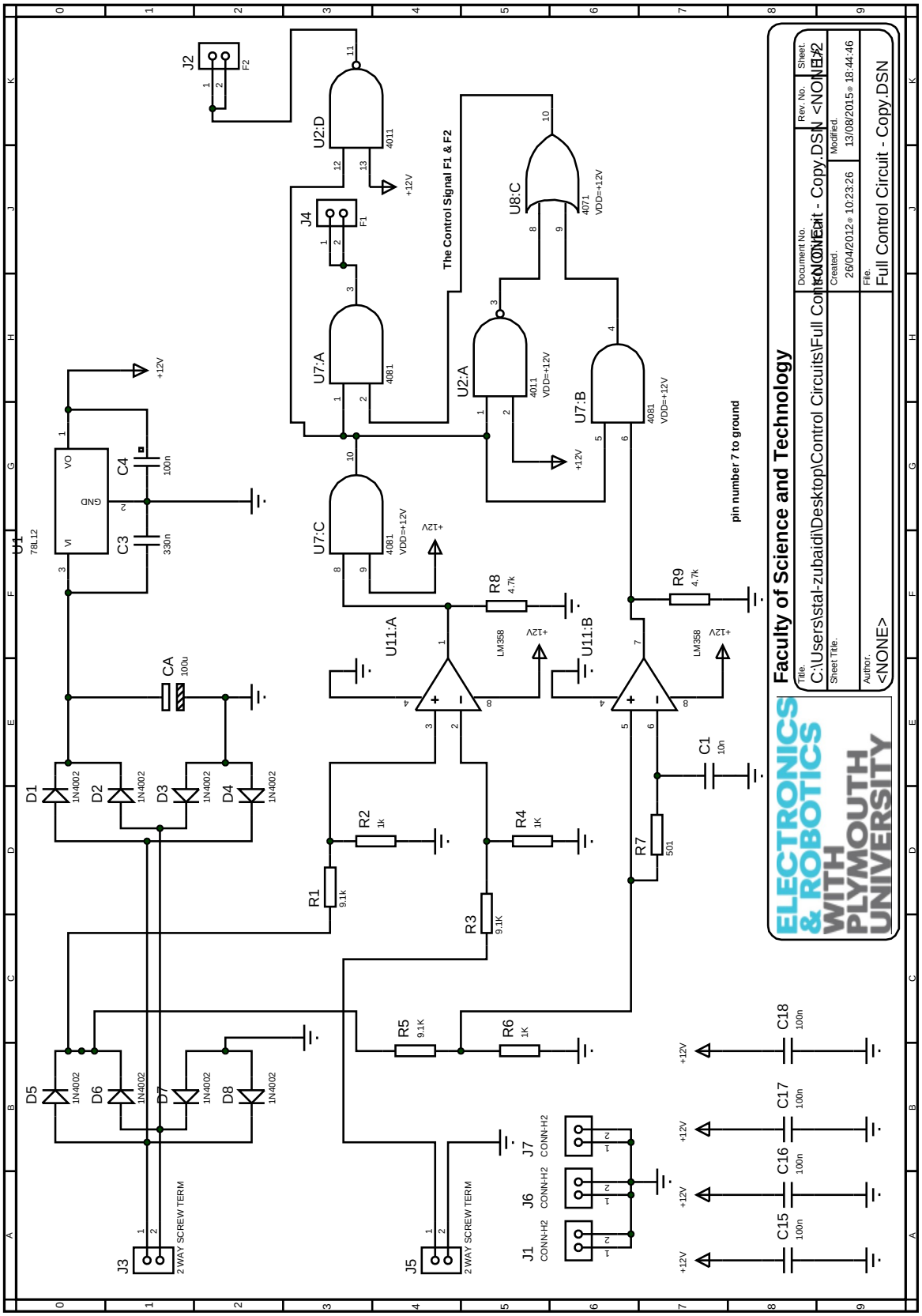

Figure C.2: The Layout of the Prototype Circuit of the Proposed Control Scheme for the New Rectifier System

Appendix D

The Layout of the Prototype Circuit and the Simulation Model in Chapter 4

The layout of the prototype circuit of the proposed buck-boost DC-DC converter is shown in figure D.1.

The layout of the simulation model of the proposed buck-boost DC-DC converter using LT spice IV 4.22 is shown in figure D.2.

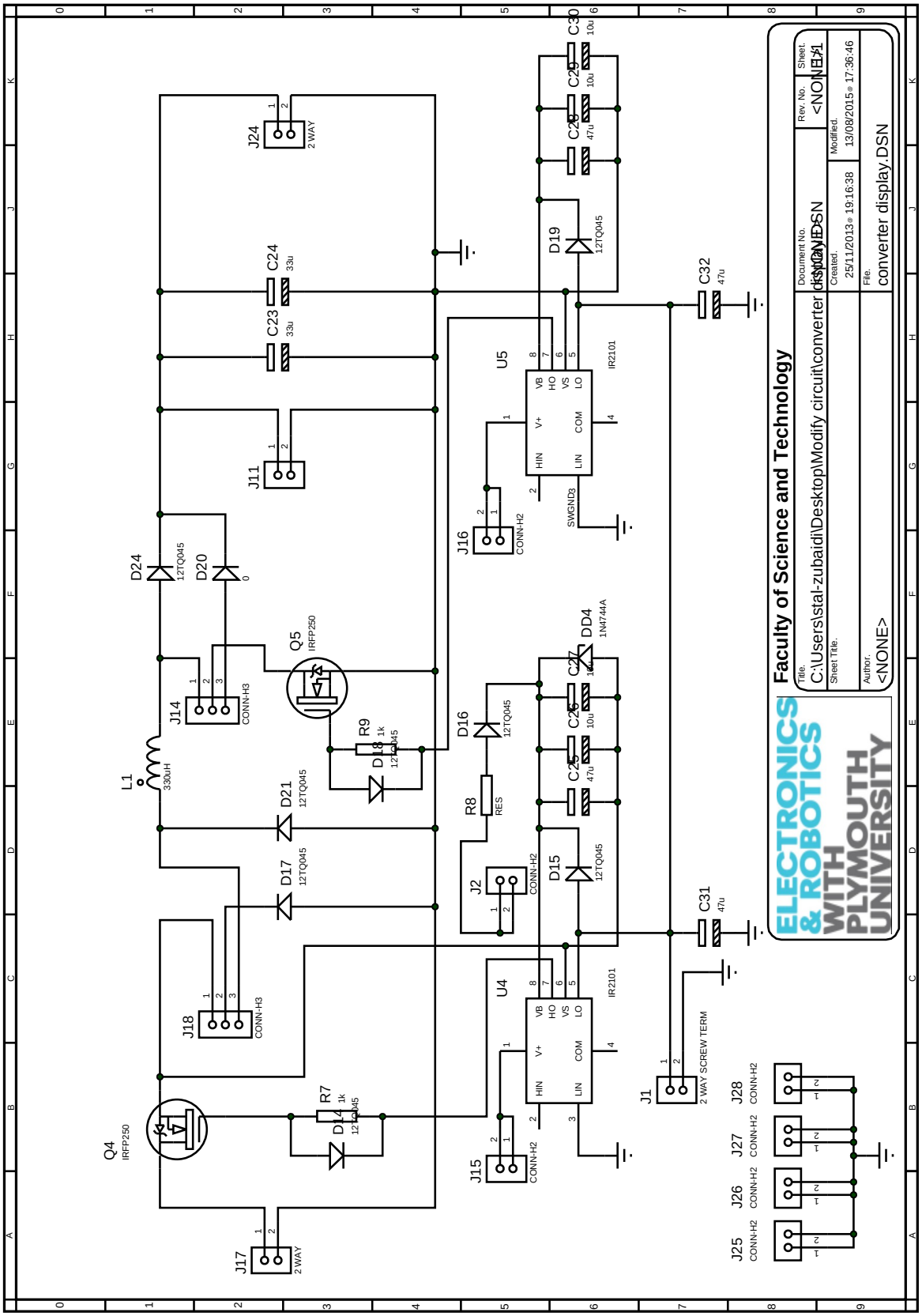

Figure D.1: The Layout of the Prototype Circuit of the Proposed Buck-Boost DC-DC Converter

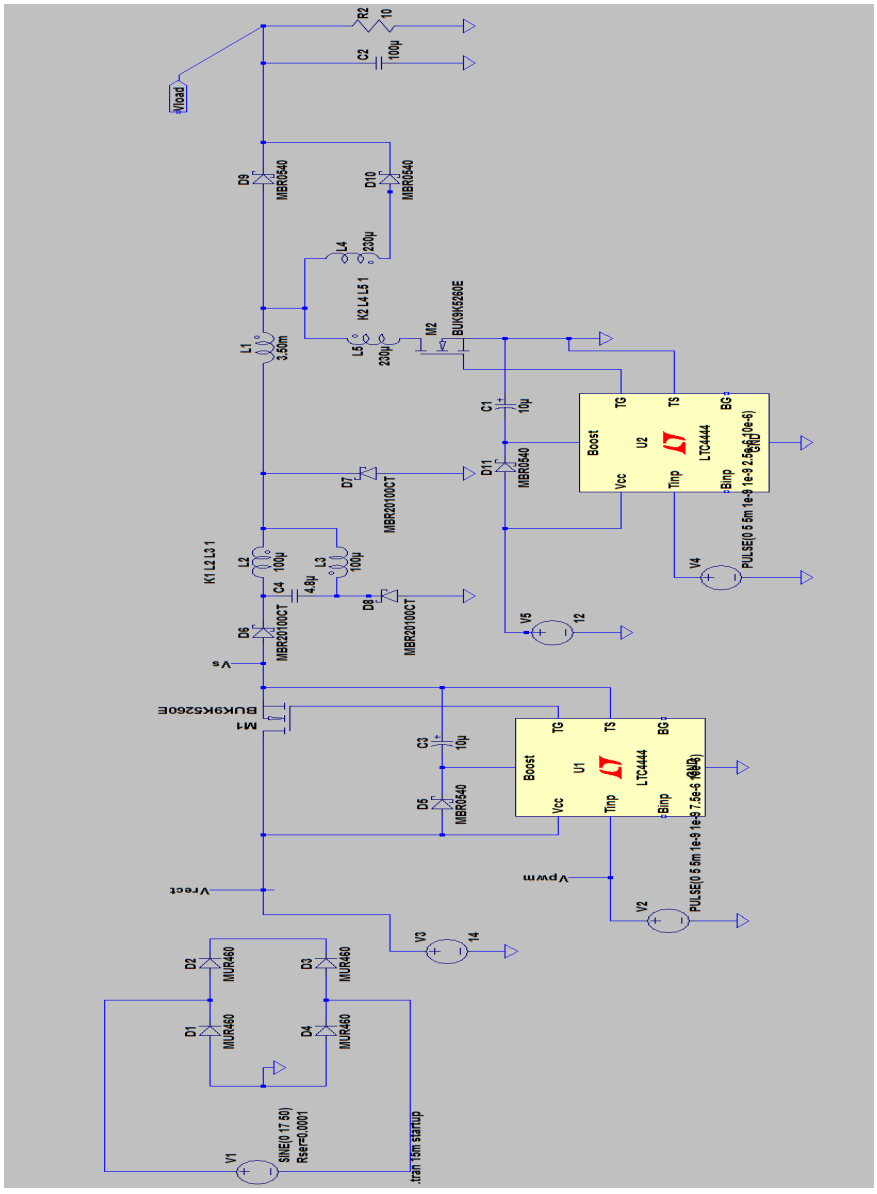

Figure D.2: The Layout of the Simulation Model of the Proposed Buck-Boost DC-DC Converter

Appendix E

Practical case studies of the proposed buck-boost DC-DC converter in Chapter 4

E.1 Case Study 3

The experimental current waveforms of the buck stage are shown in figures E.1, E.2 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure E.3, while the current waveforms of the boost stage and the output current are all shown in figure E.4. The measured efficiency for this particular case is 97.7%.

E.2 Case Study 4

The experimental current waveforms of the buck stage are shown in figures E.5, E.6 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure E.7, while the current waveforms of the boost stage and the output current are all shown in figure E.8. The measured efficiency for this particular case is 95.2%.

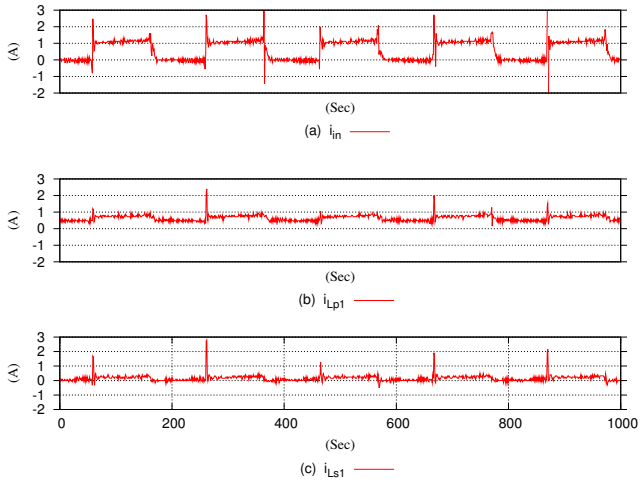

Figure E.1: Experimental Current Waveforms of Case Study 3: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

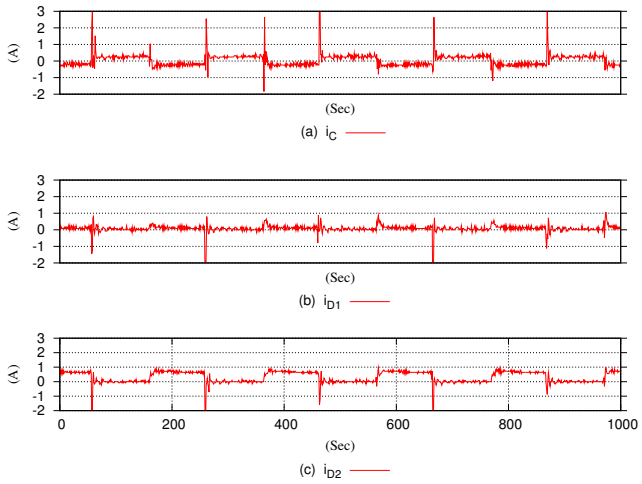

Figure E.2: Experimental Current Waveforms of Case Study 3: (a) current of capacitor C_i, (b) current of diode D_1, (c) current of diode D_2,

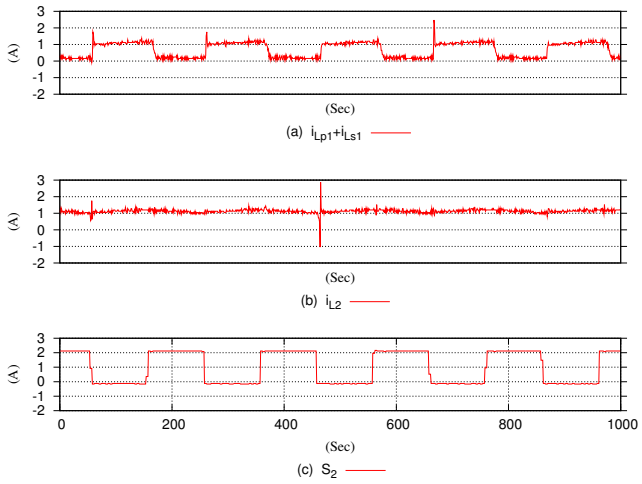

Figure E.3: Experimental Current Waveforms of Case Study 3: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

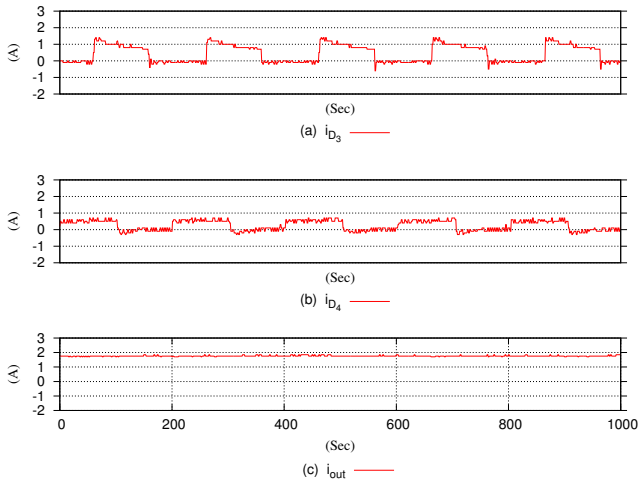

Figure E.4: Experimental Current Waveforms of Case Study 3: (a) current of diode D_3, (b) current of diode D_4, (c) output current i_{out}

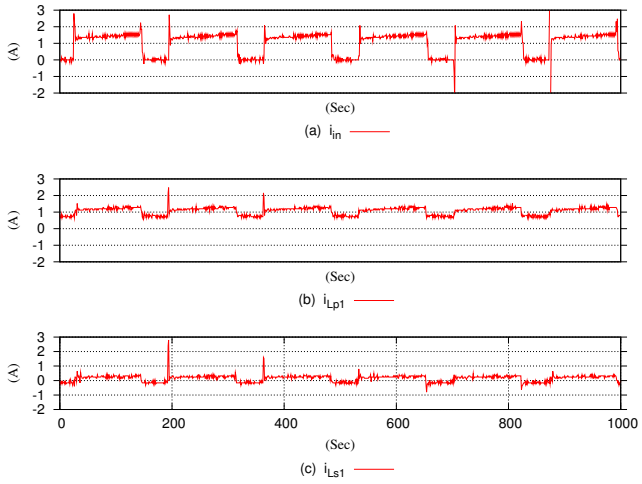

Figure E.5: Experimental Current Waveforms of Case Study 4: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

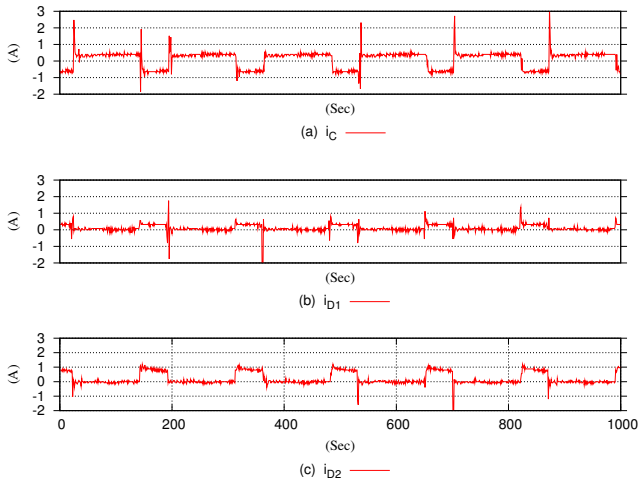

Figure E.6: Experimental Current Waveforms of Case Study 4: (a) current of capacitor C_i, (b) current of diode D_1, (c) current of diode D_2,

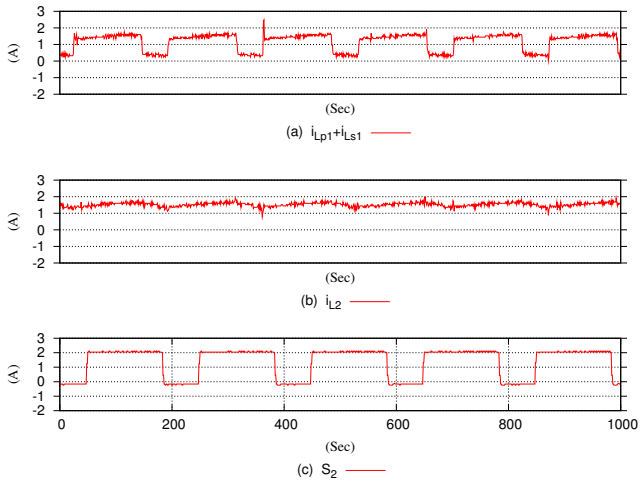

Figure E.7: Experimental Current Waveforms of Case Study 4: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

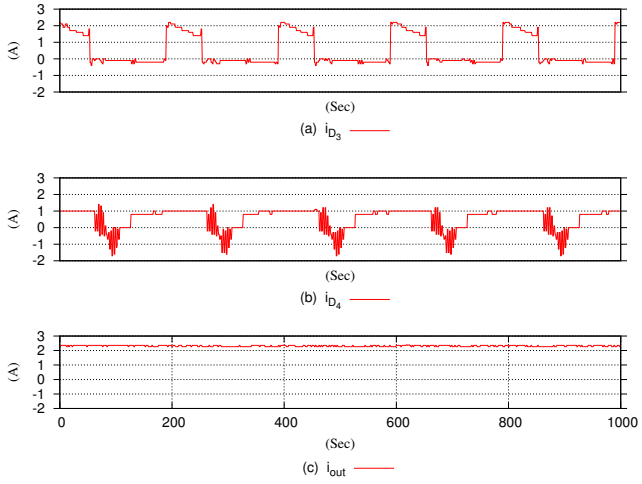

Figure E.8: Experimental Current Waveforms of Case Study 4: (a) current of diode D_3, (b) current of diode D_4, (c) output current i_{out}

Appendix F

Simulated case studies of the proposed buck-boost DC-DC converter in Chapter 4

F.1 Case Study 3

The simulated current waveforms of the buck stage are shown in figures F.1, F.2 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure F.3, while the current waveforms of the boost stage and the output current are all shown in figure F.4.

F.2 Case Study 4

The simulated current waveforms of the buck stage are shown in figures F.5, F.6 respectively. The primary and secondary winding currents of T_1, main inductor current and the gate signal of switch S_2 are shown in figure F.7, while the current waveforms of the boost stage and the output current are all shown in figure F.8.

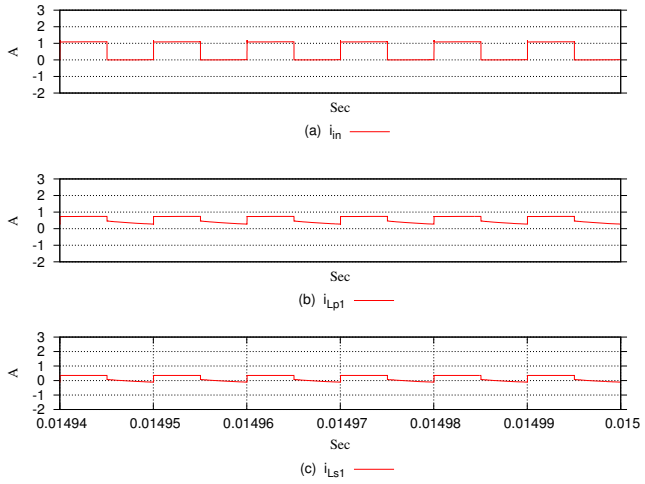

Figure F.1: Simulated Current Waveforms of Case Study 3: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

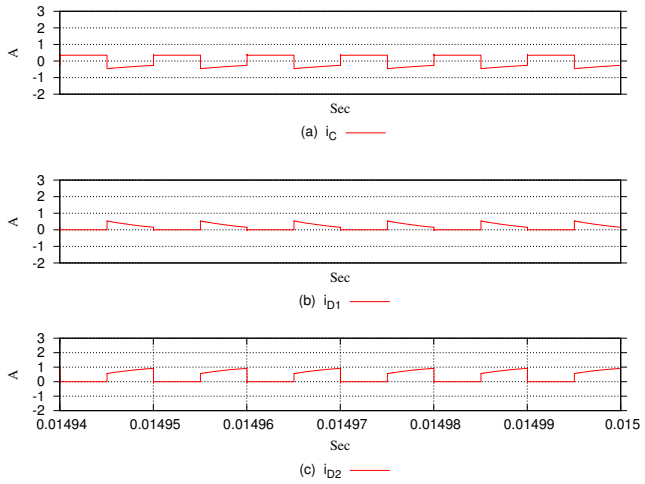

Figure F.2: Simulated Current Waveforms of Case Study 3: (a) current of capacitor C_i, (b) current of diode D_1, (c) current of diode D_2,

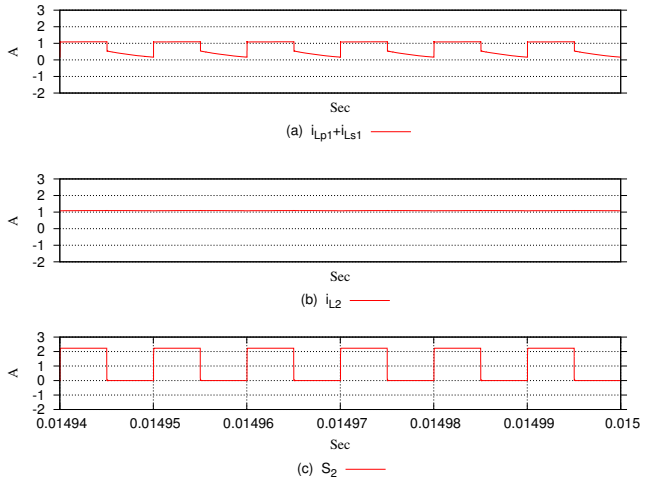

Figure F.3: Simulated Current Waveforms of Case Study 3: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

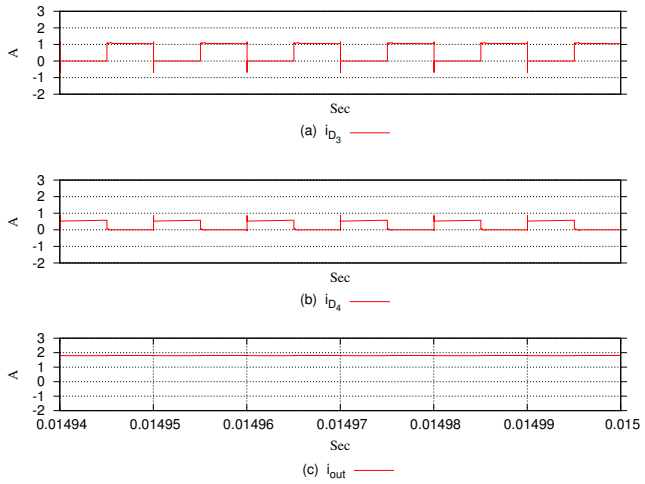

Figure F.4: Simulated Current Waveforms of Case Study 3: (a) current of diode D_3, (b) current of diode D_4, (c) output current i_{out}

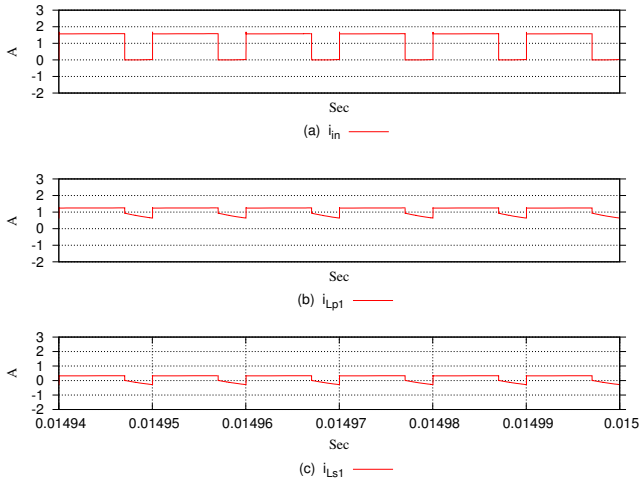

Figure F.5: Simulated Current Waveforms of Case Study 4: (a) input current, (b) primary winding current of T_1, (c) secondary winding current of T_1

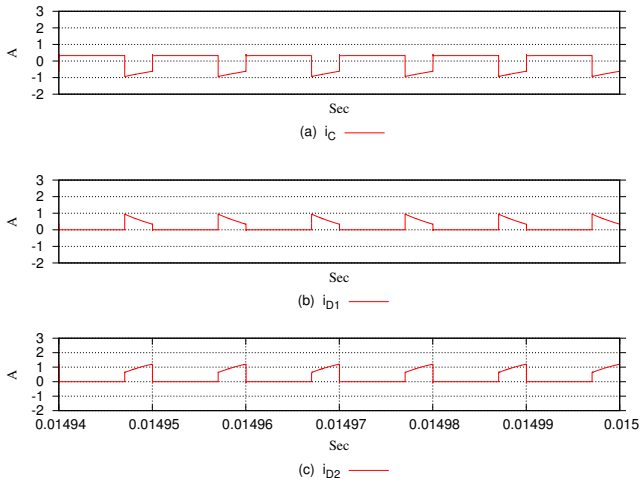

Figure F.6: Simulated Current Waveforms of Case Study 4: (a) current of capacitor C_i, (b) current of diode D_1, (c) current of diode D_2,

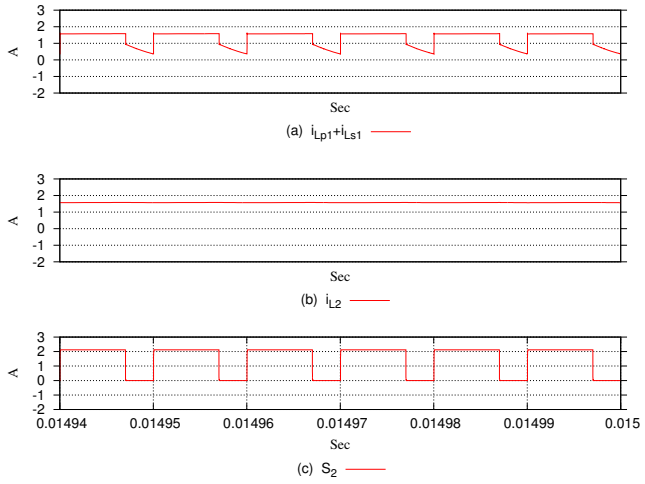

Figure F.7: Simulated Current Waveforms of Case Study 4: (a) primary and secondary winding currents of T_1, (b) main inductor current L_2, (c) switching signal of switch S_2

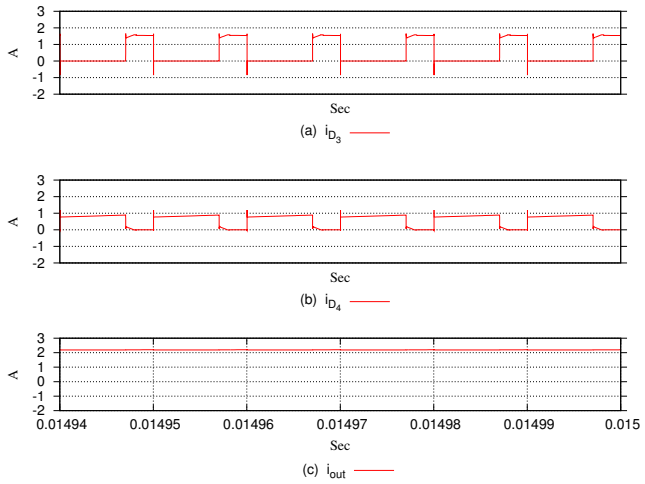

Figure F.8: Simulated Current Waveforms of Case Study 4: (a) current of diode D_3, (b) current of diode D_4, (c) output current i_{out}

Appendix G

A New Three Phase Buck Converter Using Three-Single Modules of Single Phase Buck Converters

G.1 Introduction

Three phase AC-DC step-down converters employ three phase diode bridge rectifiers are widely used in many applications due to the low cost and the simplicity in construction. Switching power supplies; adjustable speed AC motor drivers; and many others industrial systems are some of these applications.

Three phase AC-DC converters connected to the mains AC supply are injected a considerable amount of harmonics due to the pulsating line current particularly in big scale loads as in the commercial and industrial loads. Harmonics are responsible for many problems facing the AC power networks. Low input power factor and the mains voltage distortion are some of these serious consequences of high harmonic content of the line current of such non-linear loads.

Many techniques have been proposed to alleviate the effects of these non-linear loads on the mains. These techniques involved many attempts to shape the input current to be in a sinusoidal waveform and in-phase with the input voltage. Power factor correction

techniques are also used to reduce the effects of the conventional three phase rectifier system on the utility.

A brief survey can be presented to the main ideas of some of these techniques.

Lin et al. [86] proposed a three phase four-wire rectifier, the proposed circuit configuration consists of one conventional three phase diode bridge rectifier; three power switches with half DC voltage stress; three boost inductors on the AC side and two capacitors on the DC side. The experimental results confirmed the performance of the proposed technique at correcting the input power factor and eliminating the neutral current.

Mehl and Barbi [87] presented a three phase bridge rectifier with three low-power bidirectional switches and two capacitors in the DC side of the rectifier. The third harmonic component in this architecture is eliminated as there is no connection needed to the AC system neutral wire. The bidirectional switches are fired at low frequency with simple gating circuit, thus the switching loss is low. The proposed circuit achieved a high input power factor over an extending output power range.

The same circuit configuration of [87] is proposed in [88], but with a different control approach. The prototype circuit of the bidirectional switch consists of four diodes and one IGBT or MOSFET. The results proved the ability of the proposed control scheme to improve the input power factor and stabilise the output voltage against the load changes.

A three phase single-switch quadratic buck converter architecture proposed in [89–91]. It is the equivalent of two cascaded buck converters. The relationship between the output and the input voltage in this converter is proportional to D^2 instead of just D. This means that for lower output voltage, the switch does not require to remain open for as long a time as it does for the conventional buck converter. The main feature of this converter is the capability to operate with an input power factor correction over a wider range of operating conditions than the conventional three phase single switch buck converter. This is because it is a quadratic converter and it can operate with a smaller variation in duty cycle over a wide variation in input voltage with lower switch peak voltage. Balanced three phase sinusoidal input currents are produced with a satisfactory power factor correction is obtained by this converter.

A three phase two switch buck converter with LC filter in the AC side is presented in [92]. The voltage stress of the AC side capacitor is limited to the peak value of the phase voltages rather than the line voltage in the conventional converter (operates with almost half the switch voltage stress in the conventional converter). The feasibility of the proposed converter is verified with the experimental results of the prototype circuit.

An isolated three phase buck converter presented in [93]. This converter is based on the Scott transformer and two-single modules of single phase buck converter. Two single-phase single switch buck converters connected in series with a balanced split DC bus. The low-pass input filter is obtained with the leakage inductance of the Scott transformer, thus it is not necessary to add an input inductors. The output inductors are coupled, which reduces the size of the converter. The resulting input line currents are nearly sinusoidal with a unity input power factor is obtained.

The same topology of using the Scott transformer and two-single modules of single phase buck converter is presented in [94]. A new series connection technique is performed in this architecture and each buck module is rated for half of the output power. The resulting input currents are nearly sinusoidal with low harmonic distortion and unity input power factor are achieved. The same circuit concept in [94] is proposed in [95], but with two interleaved modules of single phase buck converters and one diode less. Carbone et al. [96] proposed a new three phase rectifier consists of three-single modules of single phase bridge rectifier connected in series on the DC side. The power factor can be corrected by means of simple passive circuit at the AC side of each of the rectifier circuits.

A three phase buck converter is presented in this chapter. The main idea of this project was essentially proposed by MD. R. Islam as his final year project in Plymouth University 2011. Some modifications has been added to the control scheme and the prototype circuit in order to make this circuit operates more reliable and efficiently.

G.2 Three-Phase Buck Converter Using Three-Single Modules of Single-Phase Buck Converters

G.2.1 Circuit Configuration

The circuit configuration of the proposed three-phase converter is illustrated in figure G.1

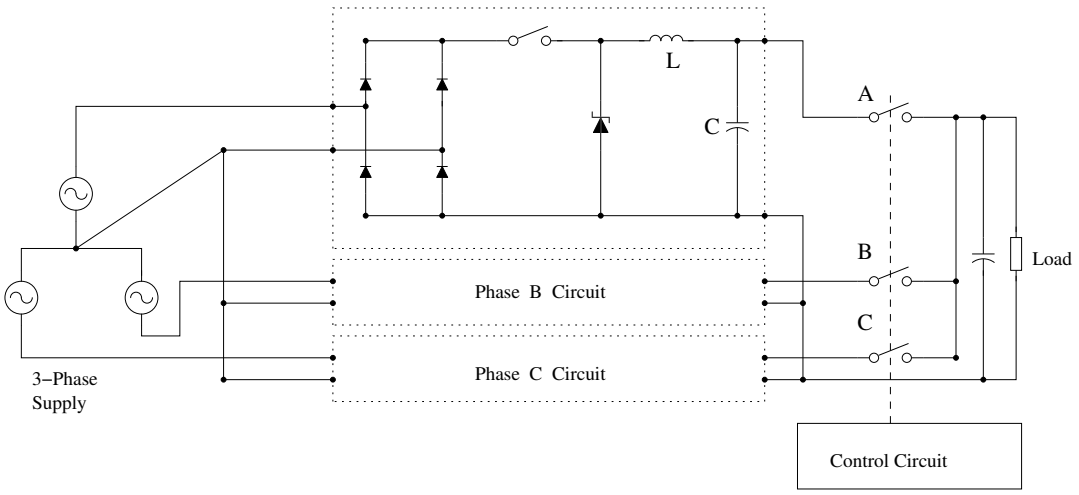

Figure G.1: Proposed Three-Single Phase Buck-Type Converter

This converter consists of three-single modules of single phase buck-type converters and a switching circuit. The switching circuit is built-up of three switches which connecting the DC side of the three-single modules from one side with the DC bus of the converter from the other side of the switch. The proposed control method is designed to ensure a fair participation of each single module in serving the connected load. This can be done by depending a cycle-order manner with a suitable switching frequency. Different switching frequencies can be applied, this is strongly depends on the type of the used switching devices and the control scheme.

The main aims of the new converter architecture is to increase the efficiency of the conventional three phase buck converter. This converter also provides a margin of reliability for the three-phase power supply as in case of failure or interruption of one phase of the three phase system or being out of service for any other reason, the rest of two phases still serving the connected load without the need to cut off the service. That can

be done easily by using simple live line detector for each phase with simple modification in the control scheme that control the action of the switching circuit.

This converter can be also used for the unbalanced distribution networks if it is follows by appropriate inverting system to restore the balance status [97].

G.2.2 Principles of Operation

The principle of operation of the new converter circuit can be demonstrated as follow

- A three phase four-wire power supply (star connection) feeds three-single phase buck-type converters. These three modules is clearly illustrated in figure G.1.
- The DC link of each of the three modules is connected to the switching circuit. The switching circuit consists of three MOSFETs switches (A, B, C) with one switch for each single module as indicated in the same figure.
- The action of these three switches is controlled by the proposed control scheme, which has been designed to drive the switches in cycle-order manner, in order to ensure a symmetrical and equal participation of each single module in serving the connected load.

G.3 The Experimental Set-up

The prototype circuits of the new converter and the conventional three phase converter have been designed, fabricated, and tested. In order to prove the validity of the new converter in terms of system efficiency, a comparison between the performances of the new and the conventional converters has been done. Two cases studies have been undertaken:

- Conventional three phase buck converter.
- Proposed three phase buck converter.

In both cases, identical loading condition of 24 Ω resistive load has been applied. Two input power supply have been used:

1. Three phase 24 V (rms) for the conventional converter.

2. Three single-phase 24 V (rms) for the proposed converter.

This is considered the main limitation in this comparison, as the two prototype circuits have been fed by two different power supplies. This is because the non availability of three phase four-wires power supply during the experiment (logistical limitations). In order to make a fair comparison between the two cases, both converters should be fed by the same power supply.

G.4 Experimental Results of Cases Studies

G.4.1 Conventional three-phase buck converter

The layout of the prototype circuit of the conventional three phase converter is shown in figure G.2.

This circuit is designed to get an output DC voltage of 12 V, 0.5 Amp, from a 24 V (rms) supply voltage. The practical results of this case study are illustrated below:

$$V_i = 24V \ ; \ I_i = 0.33A$$

$$P_i = 13.7W$$

$$V_o = 11.8 \ V \ DC \ ; \ I_o = 0.49 \ A \ DC$$

$$P_o = 5.8 \ W$$

$$Efficiency = \frac{P_o}{P_i} = 42\%$$

From the value of the observed efficiency, this system causes significant losses. A solution to address the power losses in the conventional system is discussed in the new converter system.

G.4.2 Proposed three-phase buck converter

The entire prototype circuit of the new converter is built-up of three separate prototypes circuits:

- The first prototype circuit consists of three-single phase rectifiers. The layout of the prototype circuit of the three-single modules of single phase rectifiers is shown in figure G.3.
- The second prototype circuit consists of three-single phase buck converters. The layout of the prototype circuit of a single phase buck converter is shown in figure G.4.
- The third prototype circuit is included the control circuit and the three-switch arrangement.

  The layout of the prototype circuit of the proposed control scheme for the new three phase converter system is shown in figure G.5.

In order to study the performance of the new converter in terms of efficiency, many tests points have been done with different operating conditions as follows:

1. Phase A, B, and C are all turned On.

   - AC side test results:

     $V_a = V_b = V_c = 24V$.

     I_a, I_b, I_c, are: $0.177, 0.021$, and $0.101A$ respectively.

     P_a, P_b, P_c, are: $4.24, 0.50$, and $2.42W$ respectively.

     $P_i = 4.24 + 0.50 + 2.42 = 7.16W$.

   - DC side test results:

     V_a, V_b, V_c, are: $12, 12.09$, and $12.03V$ respectively.

     I_a, I_b, I_c, are: $0.32, 0.01$, and $0.18A$ respectively.

     P_a, P_b, P_c, are: $3.84, 0.12$, and $2.16W$ respectively.

     $P_o = 3.84 + 0.12 + 2.16 = 6.12W$.

The overall system efficiency for this test point is found to be 85.4%.

2. Phase A & B On, Phase C turned Off.

   The system efficiency for this test point is found to be 89%.

3. Phase A & C On, Phase B turned Off.

   The system efficiency for this case is found to be 85.18%.

4. Phase B & C On, Phase A turned Off.

   The system efficiency for this test point is found to be 76.32%.

G.5 Summary and Conclusions

- A new three phase buck converter is presented in this appendix.
- The circuit configuration and the principles of operation of the new converter is presented.
- The architecture of the new converter is composed of three-single modules of single phase buck-type converters.
- The DC link of each of the three-single modules is connected to the DC link of the main converter by a switch.
- A control circuit has been designed to control the action of the switching circuit which is composed of three switches.
- The function of the control circuit is to drive the switches in cycle-order manner, in order to ensure a symmetrical and equal participating of each single module in serving the connected load.
- The prototype circuits of the proposed and the conventional converters have been designed, fabricated and tested.

- A comparison between the performances of the conventional and the new converters in terms of efficiency have been done by conducting two case studies under identical testing conditions.

- The experimental results proved the ability of the new converter to improve the system efficiency by 50% compared to that in the conventional buck converter.

- The results also showed in case of one phase of the three phase system being out of service for any reason, the new converter continues working with a reasonable efficiency compared to the conventional converter. This considered another feature for the proposed converter because it provides a margin of the reliability and continuity for the three phase power supplies.

- The results also showed an inequality sharing between the three-single modules to serve the connected load. This considered a very undesirable case, as that can lead to leave the balance status in the three phase system. The reasons for that are listed below:

  - The use of the same single phase power supply to feed the three-single modules of the single phase converters, while it should be fed by a three phase four-wire power supply (star connected).

  - The inaccurate operation of the proposed switching circuit because there is some delay and interference in the work of the switching devices in this circuit.

- It is easy to overcome the first reason when a three phase four-wire power supply with a sufficient output rating becomes available. The second reason has to be taken into the consideration in any future attempt to design the switching circuit of this converter, in order to make this circuit work more precisely and efficiently.

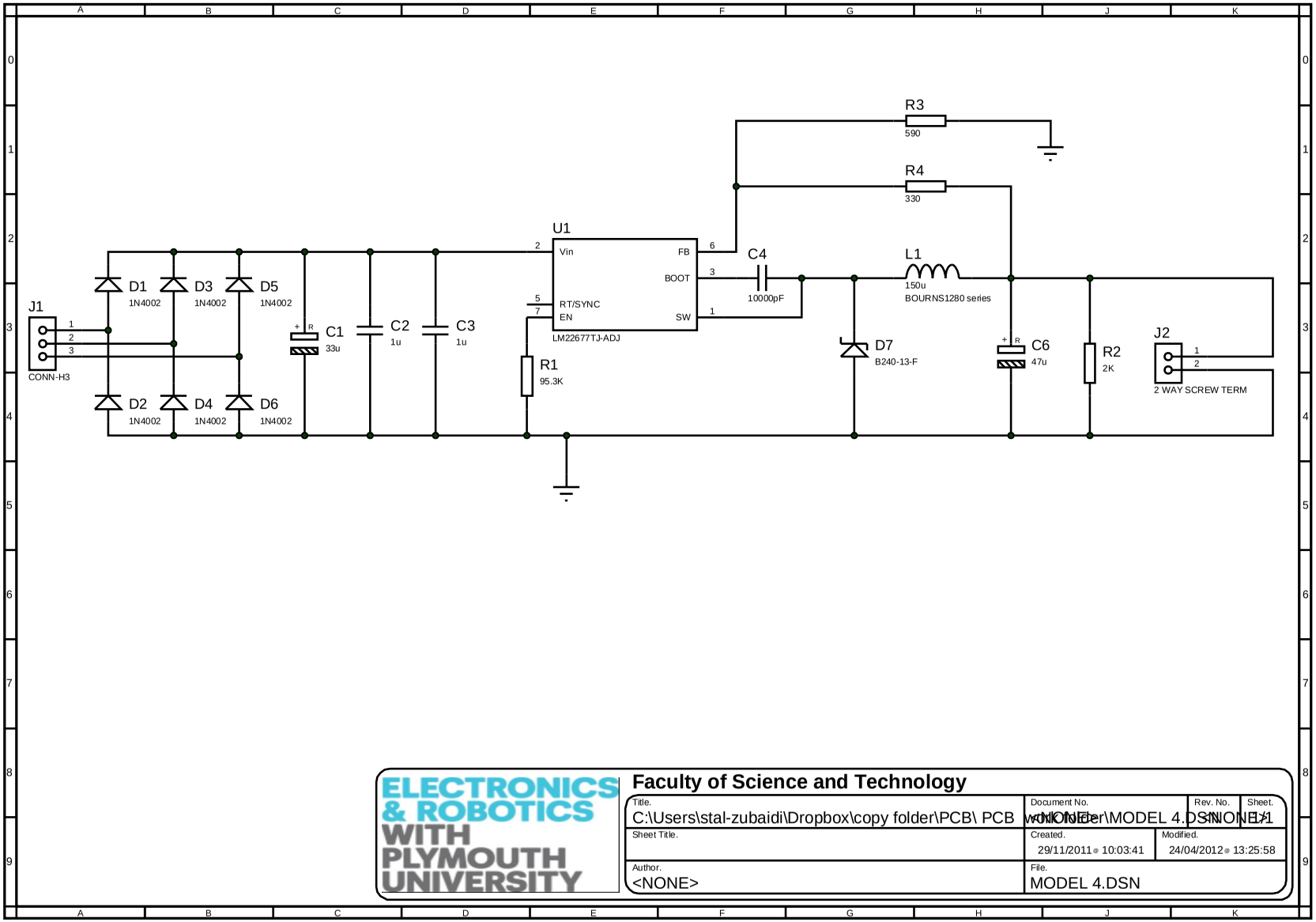

Figure G.2: The Layout of the prototype circuit of the Conventional Three Phase Converter

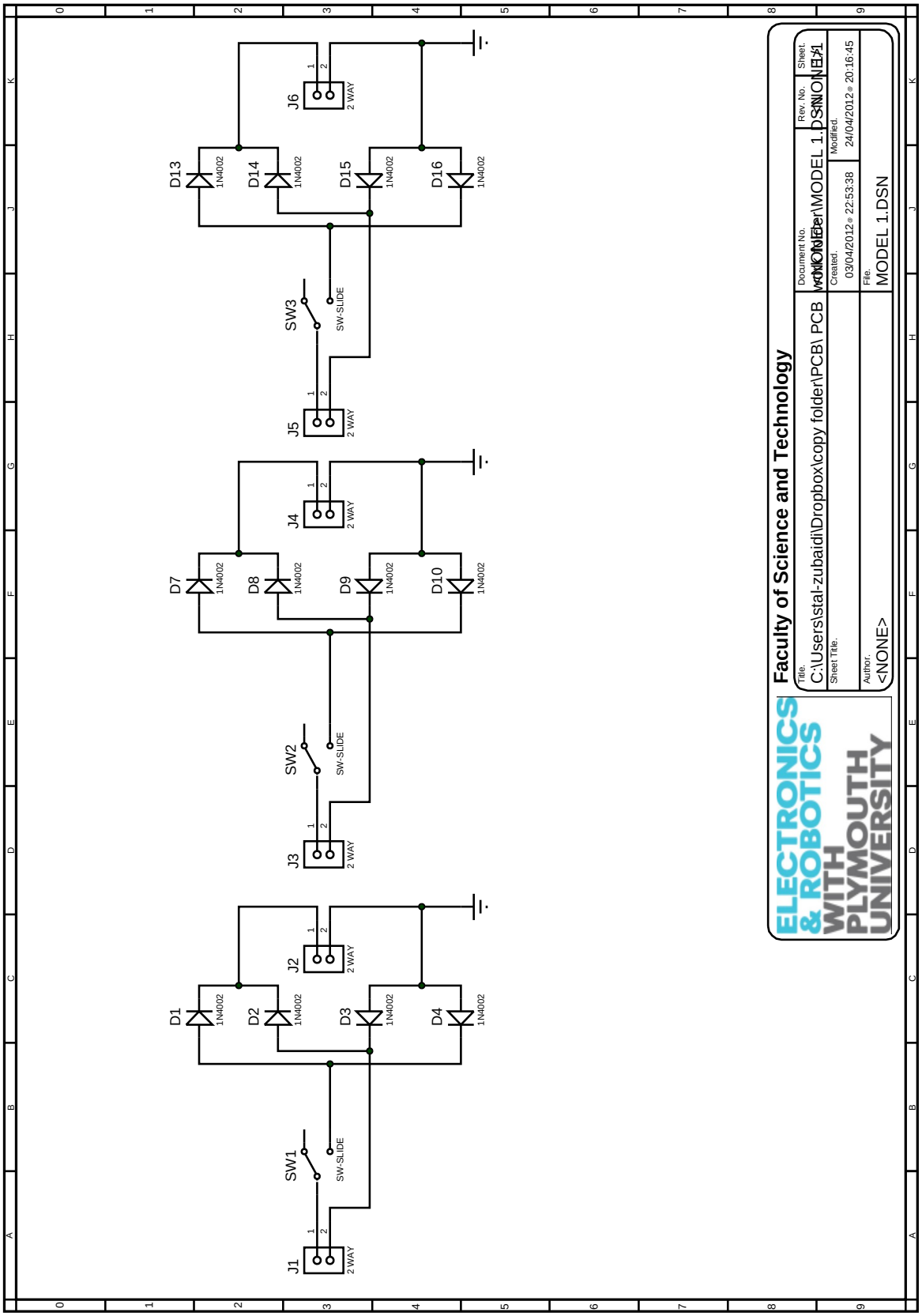

Figure G.3: The Layout of the Prototype Circuit of the Three-Single Modules of Single Phase Rectifiers

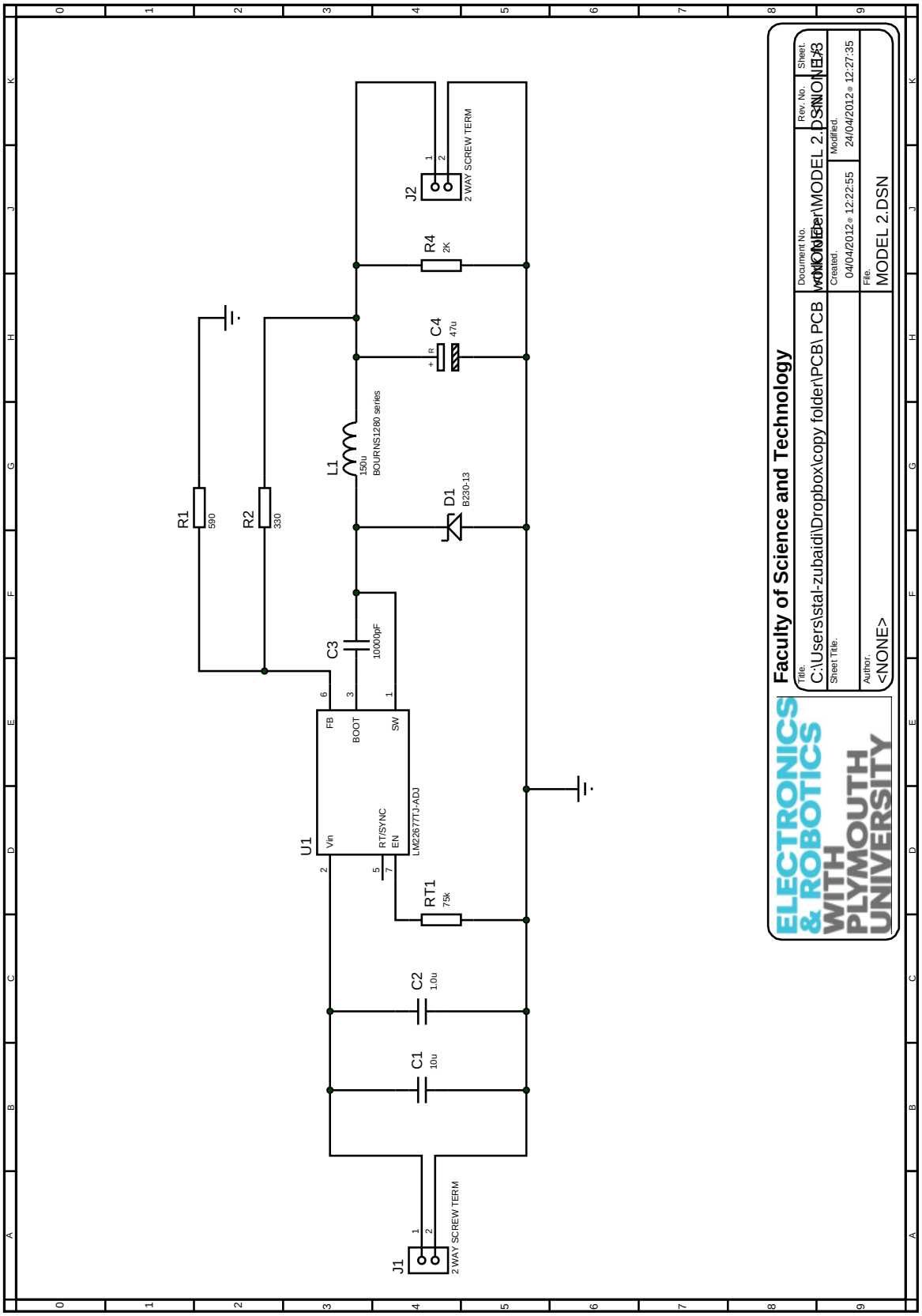

Figure G.4: The Layout of the Prototype Circuit of a Single Phase Buck Converter

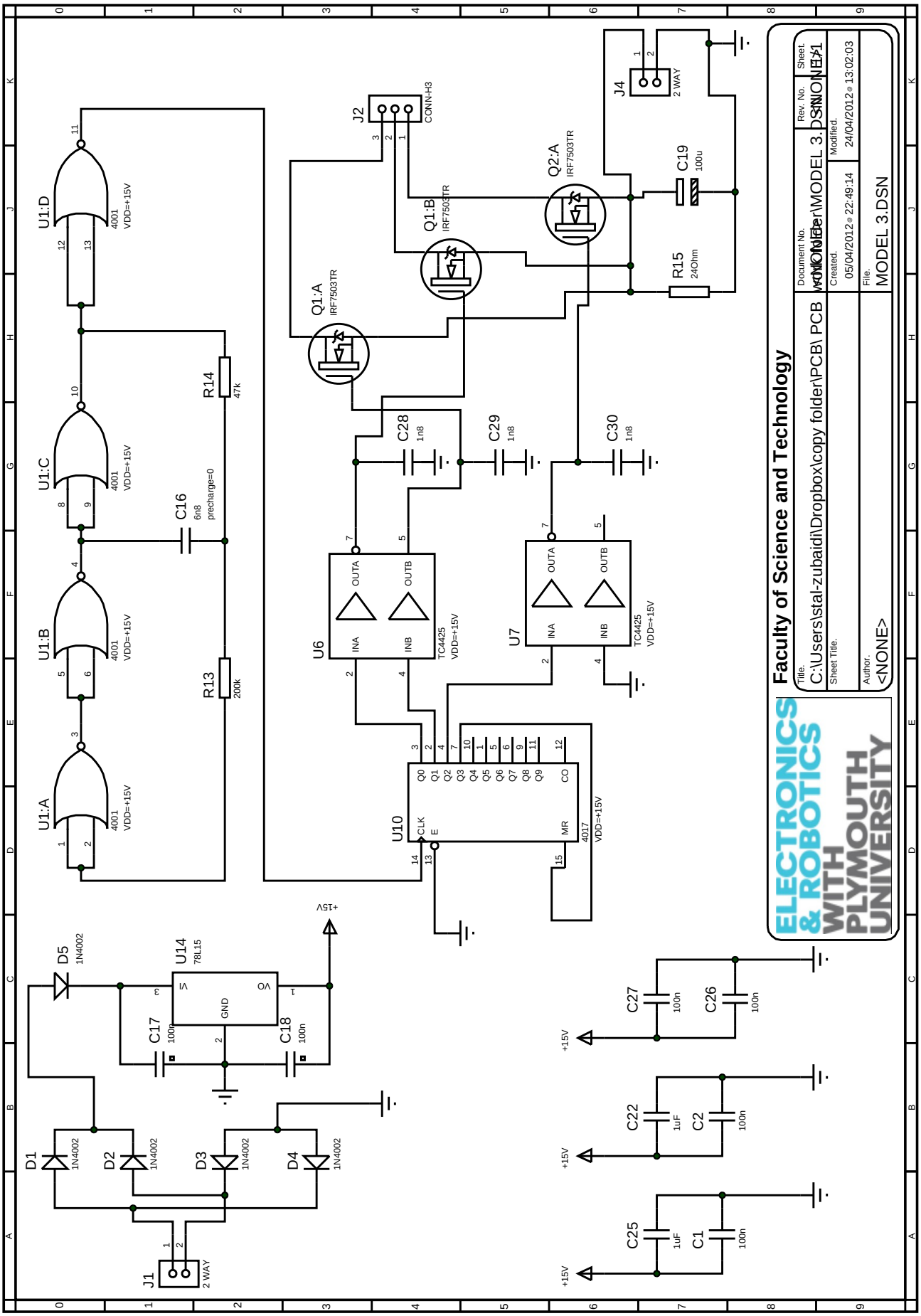

Figure G.5: The Layout of the Prototype Circuit of the Proposed Control Scheme for the New Converter System

Bibliography

[1] Muhammad H. Rashid. *Power Electronics Ciruits, Devices, and Applications.* Prentice-Hall International, USA, 2 edition, 1993.

[2] George C. Verghese John G. Kassakian, Martin F. Schlecht. *Principles of Power Electronics.* Addison-Wesley, USA, 1991.

[3] Tore M. Undeland Ned Mohan and William P. Robbins. *Power Electronics Converters, Applications and Design.* John Wiley and sons, USA, 2 edition, 1995.

[4] Cyril W. Lander. *Power Electronics.* Mc Graw-Hill, UK, 3 edition, 1993.

[5] J.N.Ross. *The essence of power electronics.* Prentice Hall Europ, UK, 1997.

[6] Mohammed Zaki Ahmed. *ELEC 214, Electromagnetic Compatability and Power Electronics Notes.* Plymouth University, UK, 2004.

[7] D.A.G.Pedder B.M.Bird, K.G.King. *An Introduction to Power Electronics.* John Wiley and sons, UK, 2 edition, 1993.

[8] PC Sen. *Power Electronics.* Tata Mc Graw-Hill, India, 2 edition, 1987.

[9] Richard A. Pearman. *Solid State Industrial Electronics.* Reston Publishing Company, Inc. A Prentice-Hall, USA, 2 edition, 1984.

[10] F.F.Mazda. *Power Electronics Handbook Components, Circuits and Applications.* Butterworths, UK, 1990.

[11] Keith Billings. *Switch Mode Power Supply Handbook.* Mc Graw-Hill, USA, 2 edition, 1999.

[12] Marvin J. Fisher. *Power Electronics*. PWS-KENT publishing company, USA, 1991.

[13] A.K. Weinberg and P. Rueda Boldo. A high power, high frequency, dc to dc converter for space applications. In *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, pages 1140–1147 vol.2, Jun 1992.

[14] M. Hirakawa, M. Nagano, Y. Watanabe, K. Andoh, S. Nakatomi, and S. Hashino. High power density dc/dc converter using the close-coupled inductors. In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pages 1760–1767, Sept 2009.

[15] A. Mansoor, W.M. Grady, R.S. Thallam, M.T. Doyle, S.D. Krein, and M.J. Samotyj. Effect of supply voltage harmonics on the input current of single-phase diode bridge rectifier loads. *Power Delivery, IEEE Transactions on*, 10(3):1416–1422, Jul 1995.

[16] M.A. Khan, A.A. Pavel, M.R. Khan, and M.A. Choudhury. Design of a single phase rectifier with switching on ac side for high power factor and low total harmonic distortion. In *Region 5 Technical Conference, 2007 IEEE*, pages 289 –292, april 2007.

[17] A.R. Prasad, P.D. Ziogas, and S. Manias. A novel passive waveshaping method for single-phase diode rectifiers. *Industrial Electronics, IEEE Transactions on*, 37(6):521 –530, dec 1990.

[18] Ji Yanchao, Liang Xiaobing, Liu Zhuo, Jin Jisheng, and Liu Xinhua. An improved passive input current waveshaping method for single-phase diode rectifier. In *Industrial Electronics, Control, and Instrumentation, 1996., Proceedings of the 1996 IEEE IECON 22nd International Conference on*, volume 2, pages 695 –699 vol.2, aug 1996.

[19] L.A. Moran, L.W. Dixon, and R.R. Wallace. A three-phase active power filter operating with fixed switching frequency for reactive power and current harmonic compensation. *Industrial Electronics, IEEE Transactions on*, 42(4):402–408, 1995.

[20] S.K. Sahoo and H.R. Jariwala. A new power factor correction technique using pfc boost converter. In *Environment and Electrical Engineering (EEEIC), 2012 11th International Conference on*, pages 819 –823, may 2012.

[21] N.R. Hamzah, M.K. Hamzah, A.S.A. Hasim, and N.F.A.A. Rahman. Single-phase shunt active power filter using single-switch incorporating boost circuit. In *Power and Energy Conference, 2008. PECon 2008. IEEE 2nd International*, pages 1112 –1117, dec. 2008.

[22] A.S.A. Hasim and M.F. Saidon. Development of a single-phase shunt active power filter using boost rectifier technique. In *Research and Development, 2006. SCOReD 2006. 4th Student Conference on*, pages 262 –265, june 2006.

[23] Z.F. Hussien, N. Atan, and I.Z. Abidin. Shunt active power filter for harmonic compensation of nonlinear loads. In *Power Engineering Conference, 2003. PECon 2003. Proceedings. National*, pages 117 – 120, dec. 2003.

[24] A.R. Bakhshai, H. Karimi, and M. Saeedifard. A new adaptive harmonic extraction scheme for single-phase active power filters. In *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, volume 3, pages III–268 – III–271 vol.3, may 2003.

[25] B. Singh, A. Chandra, and K. Al-Haddad. An improved single phase active power filter with optimum dc capacitor. In *Industrial Electronics, Control, and Instrumentation, 1996., Proceedings of the 1996 IEEE IECON 22nd International Conference on*, volume 2, pages 677 –682 vol.2, aug 1996.

[26] S.H. Pini and I. Barbi. A single-phase high-power-factor rectifier, based on a two-quadrant shunt active filter. *Power Electronics, IEEE Transactions on*, 26(11):3131–3143, 2011.

[27] J. Miret, M. Castilla, J. Matas, J.M. Guerrero, and J.C. Vasquez. Selective harmonic-compensation control for single-phase active power filter with high har-

monic rejection. *Industrial Electronics, IEEE Transactions on*, 56(8):3117–3127, 2009.

[28] M. Cirrincione, M. Pucci, G. Vitale, and A. Miraoui. Current harmonic compensation by a single-phase shunt active power filter controlled by adaptive neural filtering. *Industrial Electronics, IEEE Transactions on*, 56(8):3128–3143, 2009.

[29] H. Fujita. A single-phase active filter using an h-bridge pwm converter with a sampling frequency quadruple of the switching frequency. *Power Electronics, IEEE Transactions on*, 24(4):934–941, 2009.

[30] M.S. Golsorkhi, H. Binandeh, J.S. Moghani, G.B. Gharehpetian, and H. Hosseinian. Harmonic current compensation by a single-phase shunt active power filter based on least compensation current control method. In *Power and Energy (PECon), 2010 IEEE International Conference on*, pages 125–128, 2010.

[31] P. Kanjiya, V. Khadkikar, and H.H. Zeineldin. Achieving maximum possible power factor with single-phase shunt active power filter under distorted supply condition. In *Power India Conference, 2012 IEEE Fifth*, pages 1–6, 2012.

[32] M. Salehifar, H.A. Mohammadpour, A.H. Moghadasi, and A. Shoulaie. Harmonic elimination in single phase systems by means of a hybrid series active filter (hsaf). In *Power Electronic Drive Systems Technologies Conference (PEDSTC), 2010 1st*, pages 423–428, 2010.

[33] Wenlong Qi, Hui Wang, Xingguo Tan, Guangzhu Wang, and K.D.T. Ngo. A novel active power decoupling single-phase pwm rectifier topology. In *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, pages 89–95, March 2014.

[34] W. Ming, Q. Zhong, and X. Zhang. Transformerless single-phase rectifiers with significantly reduced capacitance. *Power Electronics, IEEE Transactions on*, PP(99):1–1, 2015.

[35] Y. Ohnuma and J.-i. Itoh. A control method for a single-to-three-phase power converter with an active buffer and a charge circuit. In *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, pages 1801 –1807, sept. 2010.

[36] Hojoon Shin and Jung-Ik Ha. Active dc-link circuit for single-phase diode rectifier system with small capacitance. In *Electronics and Application Conference and Exposition (PEAC), 2014 International*, pages 875–880, Nov 2014.

[37] Yeongrack Son and Jung-Ik Ha. Efficiency improvement in motor drive system with single phase diode rectifier and small dc-link capacitor. In *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, pages 3171–3178, Sept 2014.

[38] Ruxi Wang, Fei Wang, D. Boroyevich, R. Burgos, Rixin Lai, Puqi Ning, and K. Rajashekara. A high power density single-phase pwm rectifier with active ripple energy storage. *Power Electronics, IEEE Transactions on*, 26(5):1430 –1443, may 2011.

[39] Souhib Harb and Robert S. Balog. Single-phase pwm rectifier with power decoupling ripple-port for double-line-frequency ripple cancellation. In *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pages 1025–1029, March 2013.

[40] G.B. Lima, D. Rodrigues, L.C. De Freitas, Jr. Vieira, J.B., E. A A Coelho, V.J. Farias, and L. C G Freitas. Dsp-based implementation of input line current imposition strategy for a single-phase hybrid rectifier. In *Power Electronics Conference (COBEP), 2011 Brazilian*, pages 568–574, 2011.

[41] S. Umesh, L. Venkatesha, and A. Usha. Active power factor correction technique for single phase full bridge rectifier. In *Advances in Energy Conversion Technologies (ICAECT), 2014 International Conference on*, pages 130–135, Jan 2014.

[42] A.R. Seidel, F.E. Bisogno, D. Pappis, M.A. Dalla Costa, and R.N. do Prado. Simple valley-fill self-oscillating electronic ballast with low crest factor using pulse-frequency modulation. In *Industry Applications Conference, 2003. 38th IAS Annual Meeting. Conference Record of the*, volume 2, pages 779–784 vol.2, Oct 2003.

[43] C. Branas, F.J. Azcondo, and S. Bracho. Evaluation of an electronic ballast circuit for hid lamps with passive power factor correction. In *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]*, volume 1, pages 371–376 vol.1, Nov 2002.

[44] M.A. Dalla Costa, R.N. do Prado, A. Campos, and A.R. Seidel. An analysis about valley fill filters applied to electronic ballasts. In *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*, volume 1, pages 509–514 vol.1, Nov 2003.

[45] S.N. Rahman, F. Rabbi, and M.Z.R. Khan. Reduction of line-current total harmonic distortion (thd) of a valley fill electronic ballast. In *Electronic Devices, Systems and Applications (ICEDSA), 2011 International Conference on*, pages 131–136, 2011.

[46] J.C.W. Lam, S. Pan, and P.K. Jain. A single switch valley-fill power factor corrected electronic ballast for compact fluorescent lightings with improved lamp current crest factor. *Industrial Electronics, IEEE Transactions on*, PP(99):1–1, 2013.

[47] Jooho Song, Joong-Ho Song, I. Choy, and Ju-Yeop Choi. Improving crest factor of electronic ballast-fed fluorescent lamp current using pulse frequency modulation. *Industrial Electronics, IEEE Transactions on*, 48(5):1015–1024, Oct 2001.

[48] J.C.W. Lam, Shangzhi Pan, and P.K. Jain. A single-switch valley-fill power-factor-corrected electronic ballast for compact fluorescent lightings with improved lamp current crest factor. *Industrial Electronics, IEEE Transactions on*, 61(9):4654–4664, Sept 2014.

[49] J. Lam and P.K. Jain. A new passive valley fill dimming electronic ballast with extended line current conduction angle. In *Telecommunications Energy Conference, 2006. INTELEC '06. 28th Annual International*, pages 1–7, 2006.

[50] J.C.W. Lam and P.K. Jain. A modified valley fill electronic ballast having a current source resonant inverter with improved line-current total harmonic distortion

(thd), high power factor, and low lamp crest factor. *Industrial Electronics, IEEE Transactions on*, 55(3):1147–1159, 2008.

[51] Wuhua Li, Jianguo Xiao, Jiande Wu, Jun Liu, and Xiangning He. Application summarization of coupled inductors in dc/dc converters. In *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pages 1487–1491, Feb 2009.

[52] Guangyong Zhu, B. McDonald, and Kunrong Wang. Modeling and analysis of coupled inductors in power converters. *Power Electronics, IEEE Transactions on*, 26(5):1355–1363, May 2011.

[53] Po-Wa Lee, Y.-S. Lee, D.K.W. Cheng, and Xiu-Cheng Liu. Steady-state analysis of an interleaved boost converter with coupled inductors. *Industrial Electronics, IEEE Transactions on*, 47(4):787–795, Aug 2000.

[54] J. Imaoka, M. Yamamoto, K. Umetani, S. Arimura, and T. Hirano. Characteristics analysis and performance evaluation for interleaved boost converter with integrated winding coupled inductor. In *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, pages 3711–3718, Sept 2013.

[55] S. Kimura, J. Imaoka, and M. Yamamoto. Potential power analysis and evaluation for interleaved boost converter with close-coupled inductor. In *Power Electronics and Drive Systems (PEDS), 2013 IEEE 10th International Conference on*, pages 26–31, April 2013.

[56] K. Martin, A. Rujas, I. Villar, I. Perez-de Arenaza, and I. Etxeberria-Otadui. Design of a 2.5kw pfc boost full-sic converter based on close-coupled inductors. In *Control and Modeling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on*, pages 1–7, June 2014.

[57] M. Hirakawa, Y. Watanabe, M. Nagano, K. Andoh, S. Nakatomi, S. Hashino, and T. Shimizu. High power dc/dc converter using extreme close-coupled inductors

aimed for electric vehicles. In *Power Electronics Conference (IPEC), 2010 International*, pages 2941–2948, June 2010.

[58] Yanshen Hu, Yunxiang Xie, Huamin Xu, and Hao Tian. Design and implementation of two-channel interleaved boost converters with integrated coupling inductors. In *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, pages 625–630, Aug 2006.

[59] Fei Yang, Xinbo Ruan, Yang Yang, and Zhihong Ye. Design issues of interleaved critical conduction mode boost pfc converter with coupled inductor. In *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, pages 2245–2252, Sept 2010.

[60] Fei Yang, Xinbo Ruan, Yang Yang, and Zhihong Ye. Interleaved critical current mode boost pfc converter with coupled inductor. *Power Electronics, IEEE Transactions on*, 26(9):2404–2413, Sept 2011.

[61] Xuefeng Hu and Chunying Gong. A high voltage gain dc-dc converter integrating coupled-inductor and diode-capacitor techniques. *Power Electronics, IEEE Transactions on*, 29(2):789–800, Feb 2014.

[62] Liping Zhou, Dongyuan Qiu, Wenxun Xiao, and Bo Zhang. A single-switch high step-up dc-dc converter with coupled inductor. In *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, pages 4251–4256, Sept 2014.

[63] Shih-Ming Chen, Man-Long Lao, Yi-Hsun Hsieh, Tsorng-Juu Liang, and Kai-Hui Chen. A novel switched-coupled-inductor dc-dc step-up converter and its derivatives. *Industry Applications, IEEE Transactions on*, 51(1):309–314, Jan 2015.

[64] K.I. Hwu, A.P. Tseng, and Jenn-Jong Shieh. High step-up converter based on multi-winding coupled inductor and charge pump capacitor. In *TENCON 2013 - 2013 IEEE Region 10 Conference (31194)*, pages 1–4, Oct 2013.

[65] Shih-Ming Chen, Tsorng-Juu Liang, Kai-Hui Chen, Man-Long Lao, and Yi-Chien Shen. A novel switched-coupled-inductor dc-dc step-up converter. In *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, pages 1830–1833, Sept 2013.

[66] Wensong Yu, C. Hutchens, Jih-Sheng Lai, Jianhui Zhang, G. Lisi, A. Djabbari, G. Smith, and T. Hegarty. High efficiency converter with charge pump and coupled inductor for wide input photovoltaic ac module applications. In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pages 3895–3900, Sept 2009.

[67] A. Farooq, Chao He, Henglin Chen, and Guozhu Chen. A high step-up dc-dc converter with intermediate capacitor and coupled inductors. In *Industrial Electronics and Applications (ICIEA), 2014 IEEE 9th Conference on*, pages 1791–1797, June 2014.

[68] Yi-Ping Hsieh, Jiann-Fuh Chen, Tsorng-Juu Liang, and Lung-Sheng Yang. Novel high step-up dc-dc converter with coupled-inductor and switched-capacitor techniques for a sustainable energy system. *Power Electronics, IEEE Transactions on*, 26(12):3481–3490, Dec 2011.

[69] Yi-Ping Hsieh, Jiann-Fuh Chen, Tsorng-Juu Liang, and Lung-Sheng Yang. A novel high step-up dc-dc converter for a microgrid system. *Power Electronics, IEEE Transactions on*, 26(4):1127–1136, April 2011.

[70] Jian Fu, Bo Zhang, and Dongyuan Qiu. A high-efficiency high step-up dc-dc converter with passive clamped coupled-inductor and voltage double cells. In *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, pages 3333–3340, Sept 2014.

[71] A. Ajami, H. Ardi, and A. Farakhor. A novel high step-up dc/dc converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications. *Power Electronics, IEEE Transactions on*, 30(8):4255–4263, Aug 2015.

[72] Tsai-Jie Lin, Jiann-Fuh Chen, and Yi-Ping Hsieh. A novel high step-up dc-dc converter with coupled-inductor. In *Future Energy Electronics Conference (IFEEC), 2013 1st International*, pages 777–782, Nov 2013.

[73] Rong-Jong Wai and Rou-Yong Duan. High step-up converter with coupled-inductor. *Power Electronics, IEEE Transactions on*, 20(5):1025–1035, Sept 2005.

[74] Moon-Hwan Keum, Yoon Choi, Sang-Kyoo Han, and Jeong il Kang. High efficiency voltage-clamped coupled-inductor boost converter. In *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, pages 828–833, Nov 2013.

[75] T.-F. Wu, Y.-S. Lai, J.-C. Hung, and Y.-M. Chen. An improved boost converter with coupled inductors and buck-boost type of active clamp. In *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, volume 1, pages 639–644 Vol. 1, Oct 2005.

[76] Tsai-Fu Wu, Yu-Sheng Lai, J.-C. Hung, and Yaow-Ming Chen. Boost converter with coupled inductors and buck-boost type of active clamp. *Industrial Electronics, IEEE Transactions on*, 55(1):154–162, Jan 2008.

[77] Sheng-Kai Kao, Jiann-Fuh Chen, and Yi-Ping Hsieh. Zero voltage switching high step-up dc-dc converter with coupled-inductor. In *Future Energy Electronics Conference (IFEEC), 2013 1st International*, pages 199–204, Nov 2013.

[78] Xi Zhang, Lei Jiang, Junjun Deng, Siqi Li, and Zheng Chen. Analysis and design of a new soft-switching boost converter with a coupled inductor. *Power Electronics, IEEE Transactions on*, 29(8):4270–4277, Aug 2014.

[79] M. Khalilzadeh, M. Mahdipour, and K. Abbaszadeh. High step-up dc-dc converter based on three-winding coupled inductor. In *Power Electronics, Drives Systems Technologies Conference (PEDSTC), 2015 6th*, pages 195–200, Feb 2015.

[80] Kuo-Ching Tseng, Jang-Ting Lin, and Chi-Chih Huang. High step-up converter with three-winding coupled inductor for fuel cell energy source applications. *Power Electronics, IEEE Transactions on*, 30(2):574–581, Feb 2015.

[81] H. Liu and F. Li. Novel high step-up dc-dc converter with active coupled-inductor network for a sustainable energy system. *Power Electronics, IEEE Transactions on*, PP(99):1–1, 2015.

[82] P.M. Woodward and I.L. Davies. Information theory and inverse probability in telecommunication. *Proceedings of the IEE - Part III: Radio and Communication Engineering*, 99(58):37–44, 1952.

[83] S. Al-Zubaidi, M.Z. Ahmed, and P. Davey. Design of single bidirectional switch single phase rectifier with reduced size dc side capacitor. In *Future Energy Electronics Conference (IFEEC), 2013 1st International*, pages 18–23, Nov 2013.

[84] S. Al-Zubaidi, M.Z. Ahmed, and P. Davey. High power factor single phase rectification technique with reduced line current harmonics. In *Control and Modeling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on*, pages 1–6, June 2014.

[85] S. Al-Zubaidi, M.Z. Ahmed, and P. Davey. A novel buck-boost dc-dc converter using close-coupled inductors. In *Power Electronics for Distributed Generation Systems (PEDG), 2015 IEEE 6th International Symposium on*, pages 1–8, June 2015.

[86] B.R. Lin, T.Y. Yang, and Y.C. Lee. Three-phase high-power-factor rectifier with three ac power switches. In *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, volume 3, pages III–256 – III–259 vol.3, may 2003.

[87] E.L.M. Mehl and I. Barbi. An improved high-power factor and low-cost three-phase rectifier. *Industry Applications, IEEE Transactions on*, 33(2):485 –492, mar/apr 1997.

[88] Hong-Hee Lee, B. Sergey, Van-Tung Phan, and Tae-Won Chun. A novel control strategy for three-phase rectifier with high power factor. In *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, pages 2255 –2261, nov. 2006.

[89] J. Shah and G. Moschopoulos. Three-phase rectifiers with power factor correction. In *Electrical and Computer Engineering, 2005. Canadian Conference on*, pages 1270–1273, May.

[90] S. Bassan and G. Moschopoulos. A comparative study of three-phase single-switch buck converters. In *Electrical and Computer Engineering, 2008. CCECE 2008. Canadian Conference on*, pages 000317–000320, May.

[91] J. Shah and G. Moschopoulos. A new three-phase single-switch rectifier with stepped down output voltage near unity power factor and extended operating range. In *Telecommunications Energy Conference, 2004. INTELEC 2004. 26th Annual International*, pages 462–467, Sept.

[92] S.K. Bassan, D.S. Wijeratne, and G. Moschopoulos. A three-phase reduced-switch high-power-factor buck-type converter. *Power Electronics, IEEE Transactions on*, 25(11):2772–2785, Nov.

[93] A.A. Badin and I. Barbi. Three-phase series-buck rectifier with split dc-bus based on the scott transformer. In *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pages 516–522, June.

[94] A.A. Badin and I. Barbi. Unity power factor isolated three-phase rectifier with two single-phase buck rectifiers based on the scott transformer. *Power Electronics, IEEE Transactions on*, 26(9):2688–2696, Sept 2011.

[95] A.A. Badin and I. Barbi. High power factor three-phase rectifier with two interleaved single-phase buck rectifier. In *Power Electronics Conference (COBEP), 2011 Brazilian*, pages 183–188, Sept 2011.

[96] R. Carbone, P. Corsonello, and A. Scappatura. A three-phase diode rectifier with low current harmonics. In *Industrial Technology, 2003 IEEE International Conference on*, volume 2, pages 642–647 Vol.2, Dec.

[97] R. Stoicescu, K. Miu, C.O. Nwankpa, D. Niebur, and Xiaoguang Yang. Three-phase converter models for unbalanced radial power-flow studies. *Power Systems, IEEE Transactions on*, 17(4):1016–1021, Nov.