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# DIGITAL ENCODING OF TELEVISION SIGNALS USING THE PULSE WIDTH MODULATOR

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DIGITAL ENCODING OF TELEVISION SIGNALS USING  
THE PULSE WIDTH MODULATOR

A thesis presented for the research degree of

DOCTOR OF PHILOSOPHY

of the

COUNCIL FOR NATIONAL ACADEMIC AWARDS

by

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## ABSTRACT

An attempt is made to quantify the circuit complexity and mean circuit speed of linearly quantized straight PCM video encoding techniques. Any significant reduction in circuit complexity (i.e. the number of active and passive devices to be integrated) is considered important since this determines chip area and yield if the encoder is to be fully integrated. Analysis indicates that the complexity of the more highly developed straight PCM video encoders can be reduced by typically a factor 3 using either non-programmed sequential encoding, pulse width modulator encoding or programmed sequential encoding (closed loop successive approximation).

The encoder studied in this work is an 8-bit pulse width modulator video encoder using a 2-step production-line technique and a detailed design procedure for a prototype encoder is given. This encoder is considered to achieve 7-bit resolution at a sampling rate of 13.3MHZ.

A mathematical model of the encoder-decoder system is developed for numerical evaluation of the effect of encoder errors and white Gaussian noise upon a coded and decoded video signal. A triangular wave test is applied to examine the effect of encoder errors upon the static transfer characteristic of the encoder. Dynamic errors are investigated by simulating colour subcarrier at the model input and observing the phase and gain errors at the filtered codec output. Using differential phase and gain, an attempt is made to determine a circuit design and alignment criterion such that most practical codecs will fall within specific bounds on these parameters (taken as  $\pm 6^\circ$  and  $\pm 6\%$  respectively). In the absense of dither, Monte Carlo analysis indicates that the maximum voltage error incurred by each encoder error source should have a high probability (95%) of being less than a half quantum if 85 - 90% of codecs measured are to fall within the above bounds. If white Gaussian noise is used as a simple dither signal then the probability of a codec falling within the above bounds may increase to about 95%.

Improvements to the encoder are discussed, including several automatic error correction techniques which combat instrumental errors and give a more robust PWM encoder. Also, by predetermining the most significant bit for each set of 4 coded bits it is possible to halve the encoder clock frequency (to 133MHZ) without significantly changing the encoder complexity.

## Glossary of symbols and abbreviations

### symbols

|                       |                                                                             |
|-----------------------|-----------------------------------------------------------------------------|
| $q$                   | quantum interval (except where otherwise stated)                            |
| $W$                   | Weber fraction                                                              |
| $n$                   | number of bits per sample (except where otherwise stated)                   |
| $E$                   | equipment complexity, in uc (except where otherwise stated)                 |
| $N$                   | number of sequential unit operations, in uo (except where otherwise stated) |
| $f_s$                 | sampling frequency                                                          |
| $f_c$                 | clock frequency                                                             |
| $f_{sc}$              | PAL subcarrier frequency                                                    |
| $t_s$                 | sampling interval                                                           |
| $t_a$                 | acquisition time of sampling gate                                           |
| $t_{pd}$              | propagation delay                                                           |
| $\longleftrightarrow$ | corresponds to                                                              |
| $Sa(x)$               | sampling function, $\sin x/x$                                               |
| $p_d$                 | differential phase                                                          |
| $\mathcal{E}_d$       | differential gain                                                           |
| $\mu$                 | mean value                                                                  |
| $\sigma$              | standard deviation                                                          |
| $p(x)$                | probability density function $x$                                            |
| $R_{xy}(\tau)$        | crosscorrelation function                                                   |
| $V(x)$                | variance $x$                                                                |
| $E(x)$                | expectation $x$                                                             |
| $\chi$                | chi-square distribution                                                     |
| $\Gamma$              | the gamma function                                                          |

### abbreviations

|     |                       |
|-----|-----------------------|
| SNR | signal to noise ratio |
|-----|-----------------------|

|     |                             |
|-----|-----------------------------|
| ECL | emitter coupled logic       |
| PWM | pulse width modulator       |
| LSB | least significant bit       |
| MSB | most significant bit        |
| SRD | step recovery diode         |
| EBU | European Broadcasting Union |
| FS  | full scale                  |
| int | integer part                |
| uo  | unit operation              |
| uc  | unit of complexity          |

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CHAPTER 1: INTRODUCTION1.0 REVIEW OF VIDEO ENCODING SYSTEMS

The incentive behind the evolution of video encoding systems stems from the fundamental advantages of PCM as a modulation system<sup>9,10,11</sup>. Essentially, it gives an exponential increase in receiver SNR with transmission channel bandwidth (the theoretically ideal trade-off relation) and performance is largely independent of distance since channel noise is not additive. Neither of these advantages apply to earlier uncoded systems such as AM, FM, PAM, PPM.

By 1950 electronic devices had progressed sufficiently to merit the application of PCM to television<sup>12</sup> and the most obvious approach is to ignore any sample to sample correlation and to treat each sample independently; this will be referred to as 'straight PCM'. Two other factors combine to give a rather inefficient but nevertheless very useful system. Firstly, it is plausible on a first analysis to assume that the video signal has a uniform amplitude distribution and, secondly, a linear quantizing law is the most obvious and simplest law to implement. Thus it seems that in a simple straight PCM video system with linear quantization the probability  $p_i$  of the  $i^{\text{th}}$  code character occurring must be about the same for all  $m$  characters so that the system is capable of transmitting the maximum possible average information

$H$  from a source, i.e.

$$H = \sum_{i=1}^m p_i \log_2 \left( \frac{1}{p_i} \right) = \log_2 m \quad \text{bits/sample} \quad (1.1)$$

Using the  $n$ -digit binary number code proposed by REEVES<sup>9</sup> this corresponds to a serial data rate of  $nf_s$  bits/sec where  $f_s$  is the sampling frequency. Early experiments with broadcast quality monochrome television using straight PCM showed that at least 6-bits per sample are required corresponding to a



serial data rate of 70 or 80Mb/s. This is very high compared with PCM telephony systems for example, and prompted research into data-rate reduction techniques. In 1952 KRETZMER<sup>16</sup> published work on the statistics of television signals and showed that in the average picture there is significant sample to sample correlation. In this case all the  $p_i$  are not equal and the picture source entropy is less than  $\log_2 m$  bits per sample. Hence, although straight PCM is capable of handling the maximum possible source entropy KRETZMER showed that this is inefficient since the actual picture source entropy is invariably less than the maximum possible. The excess capacity in straight PCM is being used to transmit redundant information.

Assuming the statistical correlation of picture signals, KRETZMER considered the entropy of a simple differential signal by applying eqn. (1.1) to the probability distribution for the difference between the video signal and its delayed replica. He showed that for a number of pictures the corresponding differential signals had an entropy of only about 3 bits per (difference) sample. Hence this 'statistical' coding scheme appeared to give very considerable data compression compared with straight PCM. By 1952 the importance of differential PCM (DPCM) was firmly established in a patent by CUTLER<sup>18</sup> and by the papers of OLIVER<sup>28</sup> and HARRISON<sup>29</sup>. However, as SCHREIBER<sup>6</sup> later pointed out, any data compression achieved by pure statistical coding is in general somewhat limited since the statistical correlations tend to be reduced by noise and only prevail under certain conditions. A significant advance in DPCM systems was made by GRAHAM<sup>30</sup> in 1958. GRAHAM published work on the perceptual properties of the human viewer and showed that the eye is more tolerant of quantizing error located at black-white interfaces than in quasi-uniform regions of the picture. He noted that this perceptual effect can be incorporated into a DPCM system by the use of a non-linear or tapered quantizing characteristic such that large difference

samples are quantized coarsely and small difference samples are finely quantized. (This is very similar to the band-split idea of KRETZMER<sup>81</sup> described a few years earlier in which the signal was split into two bands; a low-band component was finely quantized whilst the high-band component was coarsely quantized.) The non-linear quantizing characteristic permitted the use of fewer quantizing levels resulting in lower information per sample and a significant saving in channel bandwidth. GRAHAM demonstrated that 3-bits/sample DPCM with non-uniform quantizing gave markedly better pictures than straight 3-bit PCM with uniform quantization. Thus, DPCM exploits both the statistical properties of the signal and the psychophysical properties of the human viewer in order to achieve significant data compression.

As further confirmation of the work by KRETZMER<sup>16</sup>, in 1962 ROBERTS<sup>4</sup> showed that for monochrome pictures comparable improvements could be obtained in a straight PCM system by simply adding random noise to the signal before encoding. This breaks up objectionable contouring and ROBERTS claimed that with added noise 3- or 4-bits/sample PCM was comparable in performance to 6-bit PCM without noise. ROBERTS' work was later extended by THOMPSON<sup>65</sup> who generated multi-level 'noise' by decoding various pseudo-random binary sequences.

In 1965 J.B. O'NEAL<sup>17</sup> published a detailed study of DPCM to assess its feasibility in television applications. O'NEAL showed that a DPCM system based on previous sample prediction gave at least 12dB improvement in signal to quantizing noise ratio over straight PCM for the same bit-rate. This means that a 6-bit DPCM system would have a comparable SNR to that of an 8-bit straight PCM system but requires only 75% of the channel capacity. Delta modulation (one digit DPCM) was also studied by O'NEAL who concluded that for high quality television, that is for a signal to quantizing noise ratio above approximately 50dB, it has little or no advantage over straight PCM.

The advantages of DPCM over straight PCM must be weighed against the intrinsic limitations of DPCM, particularly 'slope overload distortion'. This occurs since there is a limit to the time derivative of the input signal which can be followed accurately by the coder. For example, a DPCM system designed for monochrome signals i.e. signals with falling frequency response would give a severe loss of colour saturation on PAL colour signals since the chrominance signal would cause the coder to be continually in a state of slope overload. Similar arguments apply to Delta modulation systems so that straight PCM systems were considered to be better suited for the encoding of colour signals<sup>20</sup>, at least for studio applications.

Solid-state technology advanced rapidly in the 1960's and resulted in very significant advances in straight PCM encoder development. In 1962 BROWN<sup>22</sup> attempted a solid-state straight PCM encoder for television although, surprisingly, he used a cascaded or sequential encoding technique and so required extremely fast circuitry. SCHINDLER<sup>41</sup> in 1963 described a hybrid encoding technique for wideband signals and the use of this inherently faster technique together with high speed circuitry resulted in a 6-bit straight PCM encoder capable of sampling at a 50MHZ rate; a quite significant achievement. In 1965 EDSON and HENNING<sup>21</sup> published details of a high-speed solid state 9-bit PCM encoder; this sampled at 12MHZ and could handle NTSC colour signals. By 1970 a number of straight PCM encoding systems had appeared in the literature<sup>23-25</sup> and an attempt had even been made to apply the relatively slow technique of closed loop successive approximation to video encoding<sup>26</sup>. In contrast, the inherent problems of DPCM seem to have restricted its application to relatively low definition monochrome systems<sup>27,67</sup>. A report of particular relevance to this thesis was published by the B.B.C. in 1971<sup>31</sup>. This report concluded that straight 8-bit PCM (using binary number code) is probably the most useful digital format for

general use in broadcasting on the grounds that DPCM normally coarsely quantizes high frequency information (subcarrier) and that signal processing involving arithmetic operations is easier in straight PCM. It was also concluded that the use of dither gives up to 1-bit per sample reduction in data rate for colour signals and that since a digital system will at first have to interface with the analog system a coder should be capable of handling a composite colour signal.

Meanwhile the search continued for a video encoding system which provided some degree of data compression (apart from the obvious technique of eliminating the redundant samples that occur during line and field blanking). In 1967 ROBINSON and CHERRY<sup>68</sup> published the results of their prototype 'run-length' coder. Basically, successive samples of the same amplitude are located and the length of the 'run' is transmitted along with the corresponding amplitude or brightness of the run. Run length probability measurements indicated a falling exponential distribution and in fact run lengths were restricted to a small number of standard runs, typically 4 corresponding to a run length code of 2-bits. The amplitudes of these 'standard' runs were then converted into straight PCM, stored and then read out at a reduced data rate. Clearly this statistical encoding technique introduces error due to run length restriction although the authors suggest that the positional accuracy could be satisfactory for broadcast quality pictures.

BROWN and KING<sup>34</sup> showed that a moderate degree of compression can be achieved by reducing the sampling frequency in straight 9-bit PCM (one parity bit) to 11.9MHz. This enables the serial data rate to be reduced from about 120Mb/s to 107Mb/s, but the pre-sampling and interpolation filter design now becomes critical. By the early 1970's more promising compression possibilities seemed to lie with DPCM since by now the problems of applying



DPCM to broadcast quality colour television were being overcome. For example, in 1971 GOLDING and GARLOW<sup>32</sup> proposed a novel coding scheme in which a composite NTSC colour signal is decoded into Y, I and Q components and each component is sampled at a sub-Nyquist rate. The inevitable aliased components interleave between the required components in the sampled signal and can be removed by comb filters. Each signal is encoded using DPCM and the overall system gives a useful compression ratio (compared with straight PCM) of about 3. With reference to a later report<sup>69</sup> the Y signal is coded to 5-bit DPCM and 4-bit DPCM is used for the chrominance signals. At the sub-Nyquist rates suggested in the report the final bit rate of the multiplexed video signals is only 33.4Mb/s. The slope overload problems were reduced by an 'edge-recoding' technique which essentially extended the coding range if overload occurred.

An alternative approach to the slope overload problem is to sample at exactly 3 times subcarrier frequency and to use every third sample as the prediction signal<sup>72</sup>; that is, the delay in the DPCM encoder feedback loop is 225.75ns for PAL signals. In this case the prediction will be near ideal in areas of constant colour and luminance so that any difference signal should be very small for low frequency chrominance signals and these could therefore be coded very accurately. In 1973 DEVEREUX<sup>71</sup> showed that 5-bit DPCM using third previous sample prediction and tapered quantization can give broadcast quality pictures and in 1974 he described how this could be modified for sampling at twice subcarrier frequency (corresponding to a bit rate for PAL signals of only 44.3Mb/s). Also in 1974 THOMPSON<sup>73</sup> described a prediction algorithm which enabled the previous sample rather than the third previous sample to be used. Clearly this gives a better prediction for luminance steps but the chrominance is  $2\pi/3$  radians out of phase. THOMPSON corrected the chrominance phase by taking combinations of samples on

the previous line, resulting in a form of two-dimensional prediction.

Attempts have also been made to transform straight PCM television signals into a form more suitable for applying data compression techniques<sup>74-78</sup>. A Hadamard transformation is applied which results in a time waveform which corresponds to the frequency spectrum of the signal. For a Hadamard matrix of order  $K$  the signal can effectively be split into  $K$  discrete frequency bands and samples falling into any particular band would be quantized subsequently according to the subjective importance of those frequencies. As an example, those transformed samples representing the chrominance band could be given more quantizing levels than samples corresponding to intermediate frequencies (2-3MHz). The technique therefore exploits the viewers' perception and might be expected to produce similar encoding efficiencies to DPCM<sup>73</sup>.

### 1.1 THE CONTRIBUTION OF THIS THESIS

It is apparent from the preceding review that there have been at least two major aspects to the development of digital encoding systems suitable for broadcast quality television. Firstly, great emphasis has been placed upon data compression and this has resulted in statistical and psychophysical encoding techniques. The incentive here appears to be basically economic; an efficient information transmission system is sought in that only essential information is transmitted in order to save bandwidth (or, conversely, to reduce the time taken for a specific message to be transmitted over a given bandwidth).

Secondly, a number of different straight PCM encoding systems have been tried and there has been some tendency to apply the slower but less complex encoding techniques as technological advances make this possible. This tendency is not unreasonable; less complex and therefore physically smaller encoders would have obvious advantages if, for example, three encoders

were to be incorporated into a three tube camera. Furthermore, reduced complexity could yield simpler encoder alignment, increased reliability and eventually lower cost. The economic aspect is particularly important; for example, a typical colour television studio comprising 5 colour cameras and 2 other sources might require 21 video encoders and in 1972 (at the commencement of this work) the cost of these encoders was about 90% of the total cost of converting the studio to digital working<sup>36</sup>.

As a result of these considerations a study was made of a straight PCM encoding system for colour television signals which has inherently low, perhaps minimal, complexity. The proposed encoding system is particularly relevant to studio applications as distinct from transmission applications so the corresponding encoder parameters, such as coding law, resolution and sampling frequency are based upon the recommendations given in reference 31. These points are considered briefly in section 1.2.

## 1.2 PARAMETERS OF THE PROPOSED ENCODING SYSTEM

Initially digital systems will have to handle composite PAL signals as they interface with parts of the analog system and so the encoder was designed with this view in mind. We should also consider the use of a non-linear quantizing characteristic, as used in telephony. This has the advantage of accomodating a large dynamic range whilst at the same time tending to optimise the distribution of a fixed number of quantizing levels for a signal of known amplitude probability in order to achieve minimum quantizing noise or maximum information. However, whilst it is true that the video signal has a large dynamic range (typically 50dB) and that the amplitude probability is non-uniform, for colour signals the distribution probably does not deviate far enough from uniformity to make companding worthwhile. Furthermore, a linear coding law is approximately optimal when encoding  $\gamma$ -corrected signals<sup>31</sup>.

The effects of linear quantization are well known e.g. 'contouring' can occur, particularly for monochrome signals, and differential phase and gain and 'patterning'<sup>52</sup> can occur for colour signals. Fortunately, given a specific resolution the visibility of all these effects can be reduced and the picture quality improved by the addition of a dither signal to the video signal before encoding. The SNR of the decoded signal is slightly degraded by doing this but providing the ratio exceeds the appropriate CCIR recommendation for analog signals<sup>38</sup> then the addition of dither is preferable to increasing the resolution and therefore the serial data rate. For continuous random noise the recommendation states that the weighted luminance SNR (defined as peak-peak luminance to rms noise in the band 10KHZ to 5.0MHZ) should be greater than 52dB.

As an illustration, suppose a composite video signal, comprising 100/0/100/0 colour bars is to be encoded and that a simple dither effect is obtained from a superimposed white Gaussian noise component  $e_n(t)$ . To a good approximation quantization noise and the encoder input noise can be added on an rms basis<sup>51</sup> so that the rms noise  $E_n(t)$  in the decoded and filtered output is given by

$$E_n^2(t) = \frac{q^2}{12} + \overline{e_n^2(t)}$$

Subjective tests<sup>31</sup> have indicated that contouring and patterning are substantially eliminated if  $e_n(t)$  has an rms amplitude larger than about  $0.35q$ . Hence if the video signal just fills the quantizing range (giving a luminance range of  $0.568 \cdot 2^n$  quanta) the SNR of the decoded output is

$$SNR = 6.02n + 2 \text{ dB} \quad (1.2)$$

This is the maximum SNR that can be achieved for a resolution of  $n$ -bits per sample if contouring and beat patterns are to be masked by white Gaussian



noise at the encoder input. Eqn. (1.2) assumes that the low-pass filter following the decoder has a sharp cut-off frequency equal to half the sampling frequency  $w_s$  such that the total quantizing noise power  $q^2/12$  appears in the baseband. Therefore, taking the spectrum of the sampled quantizing noise to be flat over the baseband, and assuming for convenience that the input noise is bandlimited to  $w_s/2$  then the reduction of the bandwidth to the 5.0MHZ limit gives 1.2dB reduction in output noise power (taking  $w_s/2\pi = 13.3\text{MHZ}$ ). Finally the luminance weighting factor for flat noise is 6.5dB so that the weighted luminance SNR after decoding and filtering is

$$SNR = 6.02n + 9.7 \text{ dB} \quad (1.3)$$

For a noiseless input signal this becomes  $6.02n + 13.6\text{dB}$ . Eqn. (1.3) shows that 7-bit coding is almost adequate using Gaussian dither, and in fact it is adequate if a more deterministic dither is used<sup>31</sup> since then the SNR is only degraded by about 1dB instead of by nearly 4dB for Gaussian noise. In general however, to allow for multiple coding and decoding operations 8-bit resolution is required<sup>31</sup> and an 8-bit encoder is described in this thesis.

It is interesting to note that this result is in reasonable agreement with visual perception experiments<sup>39</sup>. These have shown that the eye can detect a brightness change  $\Delta B$  of about 2% of the background brightness  $B$  and that  $\Delta B/B$  (the WEBER fraction,  $W$ ) is approximately constant over a large range of  $B$ . It follows that the ratio of the analog voltage error  $\Delta V$  to the 'background' voltage  $V$  that is permitted before a brightness error or step is perceptible can be given as

$$\frac{\Delta V}{V} = \frac{W}{\gamma}$$

where  $\gamma$  defines the mean display nonlinearity. Hence, to avoid a visible brightness step for a slowly changing background brightness centred around half full scale we have a permissible voltage error of about  $1/280$  of full scale and this corresponds to about 8-bits per sample. A background signal of 25% of full scale corresponds to 9-bits per sample although clearly these results will also depend upon parameters such as the viewing distance, the SNR of the displayed signal and also picture content.

In 1970 a letter published by DORWARD<sup>52</sup> attributed the patterning effects observed on coded and decoded colour signals to a beat between the spurious components produced by quantization and the original components. He showed experimentally that patterning can be eliminated if the sampling frequency  $w_s$  is locked to subcarrier frequency, usually 3 times subcarrier frequency, and DORWARD's results were later verified by VERHOVEN<sup>53</sup>. For a large area of colour the chrominance signal approximates to a sinewave at subcarrier frequency  $w_{sc}$  and analysis shows that quantization and subsequent sampling of this signal gives spurious components

$$w_{mn} = |mw_s \pm nw_{sc}| \quad m, n = 1, 2, 3 \dots$$

Clearly, if  $w_s$  is locked to  $w_{sc}$  then any spurious components coincide exactly with subcarrier harmonics and so no patterning can occur. A further advantage of sampling at an integral multiple of subcarrier frequency is that it aids error concealment techniques e.g. a 9<sup>th</sup> (parity) bit could be used to detect transmission errors. If an error is detected the 3<sup>rd</sup> previous sample could then be used to replace the erroneous sample since this is in the same subcarrier phase. On the other hand, the amplitude of the beat component reduces by 6dB for each additional bit and it has been concluded<sup>31,53</sup> that for straight 8-bit PCM without dither it is not necessary to lock the sampling frequency to subcarrier frequency. Moreover, for signal processing applications

(where exact line delays may be required) it may be advantageous to sample at an integral multiple of line frequency.

In principle therefore the 8-bit encoding system under investigation need not have a locked sampling frequency. In practice however, instrumental imperfections inevitably prevent perfect 8-bit coding from being achieved and, in the absence of dither it becomes necessary to lock the sampling frequency to subcarrier. These facts were born in mind in the encoder design.

## CHAPTER 2: EVALUATION OF STRAIGHT PCM VIDEO ENCODING SYSTEMS

### 2.0 A QUANTITATIVE APPROACH

This work is concerned with straight PCM encoding systems, that is systems which simply sample and quantize in contrast to statistical or psychophysical encoders. Furthermore, if discussion is restricted to the application of video encoders within a studio complex the most appropriate code for the arithmetic operations of fading, aperture correction, gamma correction etc. is a weighted code, the binary number code. Some encoding systems readily give this code whereas others require additional encoding logic or even code translation. Encoding systems falling within the above bounds are frequently only compared on a qualitative basis but it is enlightening to attempt a quantitative comparison. Two parameters of particular interest are the relative complexity and relative circuit speed required by different systems to achieve the same specification. As will be seen, technological advances giving increased logic speed can be exploited to achieve a considerable reduction in circuit complexity and the pulse width modulator principle is particularly relevant in this respect.

A suitable basis for quantitative comparison must be found; EULER<sup>58</sup> for example attempted a comparison of encoding speed but was criticised<sup>51</sup> for making misleading comparisons because he assumed that the various circuit operations, such as voltage comparison and counting take the same time. A more realistic approach is to break a circuit down into its least complex function and then to express each encoding system in terms of multiples of this function. Complexity for example can be quantified by defining a unit of complexity,  $uc$ , and the complexity of any other element is then expressed as a multiple of this basic unit. One  $uc$  is taken as the complexity of the least complex discrete circuit function and a reasonable choice is a simple logic

gate. For example, a high gain difference amplifier might be judged as having twice the circuit complexity of the gate and so is assigned  $2u_c$ , whereas an  $n$ -digit binary counter might be assigned  $2nu_c$  (taking a single flip flop as  $2u_c$ ). Only the equipment which is absolutely essential to the basic operation of the encoder is considered; power supplies, serializers, output buffers, sample and hold circuits, line drivers etc. are ignored, except where they are vital to the encoding principle. Clock generation equipment is required by virtually all encoding systems to control the sequence of operations but otherwise it is not considered vital to the encoding principle. Therefore, for simplicity, any clock generation equipment is not included in estimates of encoder complexity.

Encoding speed depends upon the number  $N$  of sequential operations required per sample period, that is, we must quantify the number of operations in the encoding path. Since some of these operations take longer than others it is helpful to define a unit of operation,  $u_o$ , which is the operation requiring the minimum time. The other operations in the encoding path can then be weighted in terms of the unit operation. Again it is reasonable to take the basic gating operation as the unit operation since other operations invariably take longer than the propagation delay of a logic gate.

To enable a comparison to be made between encoding techniques it is necessary to stipulate certain weightings and to use them throughout. This is a broad but not unreasonable assumption. Within a particular technology it is reasonable to assume that a flip-flop has about twice the propagation delay of a simple gate whether the gate delay be  $1ns$  (fast ECL) or  $10ns$  (standard TTL). Further, a level comparator could be assumed to have about twice the delay of a gate within a particular technology; a fast tunnel-diode and transistor comparator could be used in conjunction with fast ECL (section 3.3.3) whereas a different encoder might use standard TTL and a



TABLE 2.1

## SPEED AND COMPLEXITY WEIGHTING OF CIRCUIT OPERATIONS

| Operation                                          | Symbol | Units of Complexity | Unit Operations | Note |
|----------------------------------------------------|--------|---------------------|-----------------|------|
|                                                    |        | uc                  | uo              |      |
| gating (single gate)                               | g      | 1                   | 1               |      |
| storage (single bistable)                          | f      | 2                   | 2               | 1    |
| fast sample and hold                               | h      | 2                   | not applicable  |      |
| voltage comparison                                 | c      | 2                   | 2               | 2    |
| full wave rectification <sup>21</sup>              | r      | 4                   | 2               |      |
| k-digit decoding (quantizing)                      | q      | k/2                 | 5               | 3    |
| k-digit binary counting<br>(k bistables)           | b      | 2k                  | see text        |      |
| encoding logic (to k-binary digits <sup>25</sup> ) | e      | 2 <sup>k</sup>      | 2               |      |
| Gray to binary translation<br>(k-digits)           | t      | 3k                  | not applicable  |      |
| subtraction (difference amplifier)                 | d      | 2                   | 5               | 4    |

## NOTES

1. Compare D-flip flop type 7474 ( $\overline{t}_{pd} \approx 17ns$ ) with NOR gate type 7427 ( $\overline{t}_{pd} \approx 8.5ns$ ). For a different technology, compare D-flip flop type MC1668 ( $\overline{t}_{pd} \approx 1.7ns$ ) with NOR gate type MC1662 ( $\overline{t}_{pd} \approx 1.0ns$ ). For either technology the flip flops are about twice as complex as the corresponding logic gate, where 'complexity' is taken as the numerical sum of transistors and resistors.
2. In this case the relevant delay is the usual propagation delay (which is considerably shorter than the output settling time). Two cases can be cited:
  - (a) an IC high speed voltage comparator type Aml06 having  $\overline{t}_{pd} \approx 20ns$  (10mV overdrive). This is not a 'state of the art' comparator and could be considered of comparable technology to standard TTL.
  - (b) a state of the art comparator, section 3.3.3,  $t_{pd} \approx 2ns$ . A corresponding state of the art logic gate is the MC1662.

In both cases the comparator propagation delay is about a factor 2 higher than the delay of the corresponding logic gate.
3. The decoder output should settle to well within 1q before subsequent coding operations can take place. Measurements (section 3.3.4) showed that the settling time of an ultra-high-speed decoder is about 5 times the delay of an ultra-high-speed gate.
4. The difference amplifiers handle large transient analog changes at their input and the amplifier output must settle to well within 1q before subsequent coding operations can take place. Settling times of IC wideband differential amplifiers are in the range 20ns (Am733) to 80ns (Am715) and 40ns is typical. The circuit delay is therefore taken to be about 5 times that of a logic gate (7427) of comparable technology.

conventional operational amplifier comparator.

The significant point is that the weighting is only expected to change significantly if different types of technology are mixed e.g. a conventional operational amplifier comparator and fast ECL and this is unlikely to occur if the complete encoder is to be integrated. The assumed weighting for the various circuit operations referred to in this chapter are given in Table 2.1.

## 2.1 PARALLEL OR SIMULTANEOUS VIDEO ENCODERS

Parallel encoders are extremely fast and versatile. For an  $n$ -digit binary code there are  $(2^n)!$  possible codes the encoder could deliver and only minimal circuit speeds are required since there are few sequential encoding operations per sample period. GOODALL<sup>12</sup> used the technique as early as 1951 to achieve 5-digit video encoding. He used a 'coding tube' consisting of a code plate placed between an electron beam (deflected by the analog signal) and a series of collector plates. A 'line' beam was used so that all  $n$ -digits were output simultaneously. The plate represented a unit distance code (the Gray code) to minimise the effect of errors in beam alignment. However, to apply the same technique to  $n$ -digit video encoding using solid-state devices would require  $2^n - 1$  level comparators and considerable encoding logic. Also, the encoding speed is reduced somewhat due to the finite logic propagation delay.

The number of logic gates required to encode  $2^n - 1$  comparator outputs into binary number code for studio applications increases approximately exponentially with the number of digits as indicated in Table 2.1. Typically the logic for each binary digit consists of a 2-rank system of NAND gates<sup>25</sup> so that 'e' in Table 2.1 can be assigned 2uo. Therefore, for a



solid-state parallel encoder delivering an n-digit binary number code a reasonable estimate of the equipment required is, from Table 2.1

$$E = e + (2^n - 1)c \approx 3.2^n \text{ uc} \quad (2.1)$$

For 8-digits this corresponds to 768uc or the complexity equivalent to about 768 basic logic gates! The encoding speed can be estimated by considering the number, N, of sequential operations per sample period. In this case we have only two basic operations (level comparison and encoding) and so

$$N = C + e = 4 \text{ uc} \quad (2.2)$$

To illustrate the practical significance of this, assume that the time allowed for coding in one sample period is 60ns; this is a typical figure for video encoders after allowing for the sample and hold acquisition time (see section 3.1). It follows that 15ns can be allotted to each unit operation and a simple logic gate can have 15ns propagation delay and each comparator can have 30ns delay. These two values are reasonably compatible in that they could probably be realised by a single technology (in this case standard TTL technology would seem to be most applicable). The encoder logic speed requirements are therefore quite modest for video encoding applications. Conversely of course, the use of high speed logic and a fast analog comparator would enable the sampling rate to be increased significantly, perhaps to several hundred MHz.

## 2.2 HYBRID VIDEO ENCODERS

TEESDALE and WESTON<sup>23</sup> avoided the high complexity of the truly parallel encoder by using a ternary based binary code devised by NEU<sup>55</sup>. More explicitly, 3 levels can be represented by 3 pairs of binary digits and this can be extended to cover  $3^k$  levels with 2k digits as indicated in Fig. 2.1.

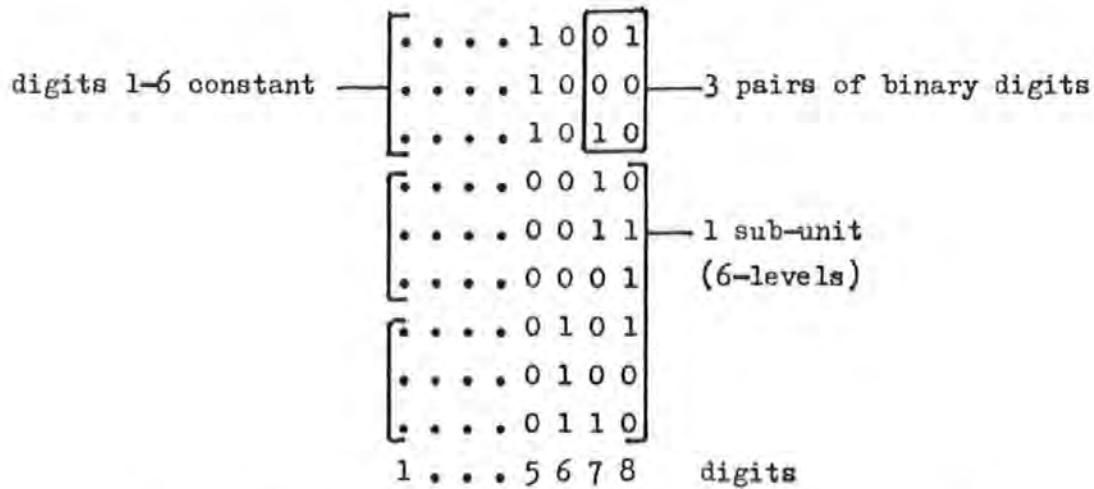


Fig. 2.1: The 8-digit code raster used by TEESDALE and WESTON  
(NEU's 'C' code)

The digit pair sequence repeats after 6 levels so the code raster can be divided into 6-level 'subunits'. The TEESDALE and WESTON video encoder first coarsely split the quantization range into 14 subunits and each subunit encoded a further 6 levels giving a total of 81 levels (with 3 redundant levels). This sequence of operations involved cascaded level comparators followed by a simple gating operation so the number of sequential operations per sample period is essentially

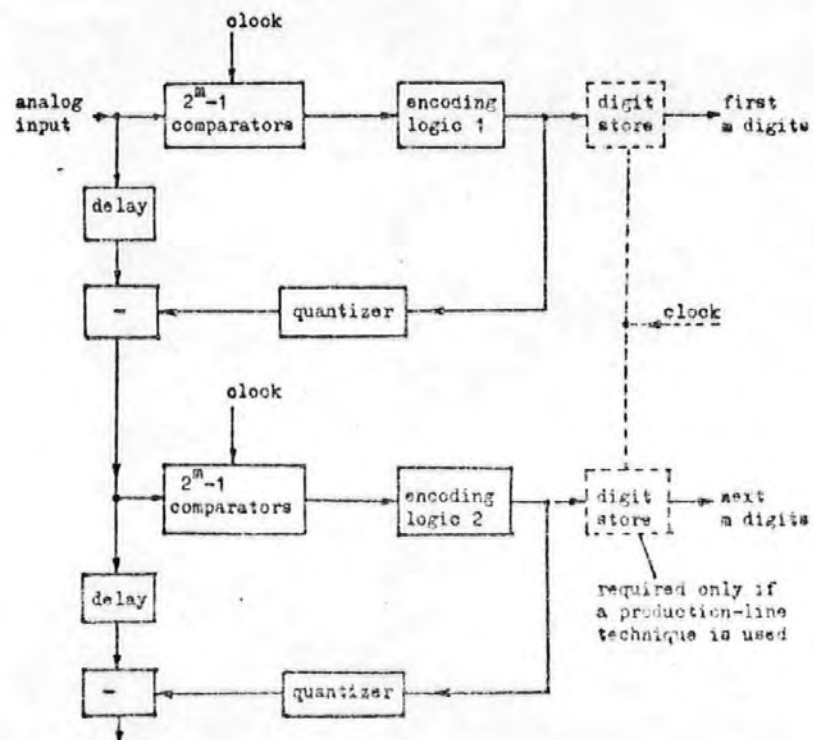
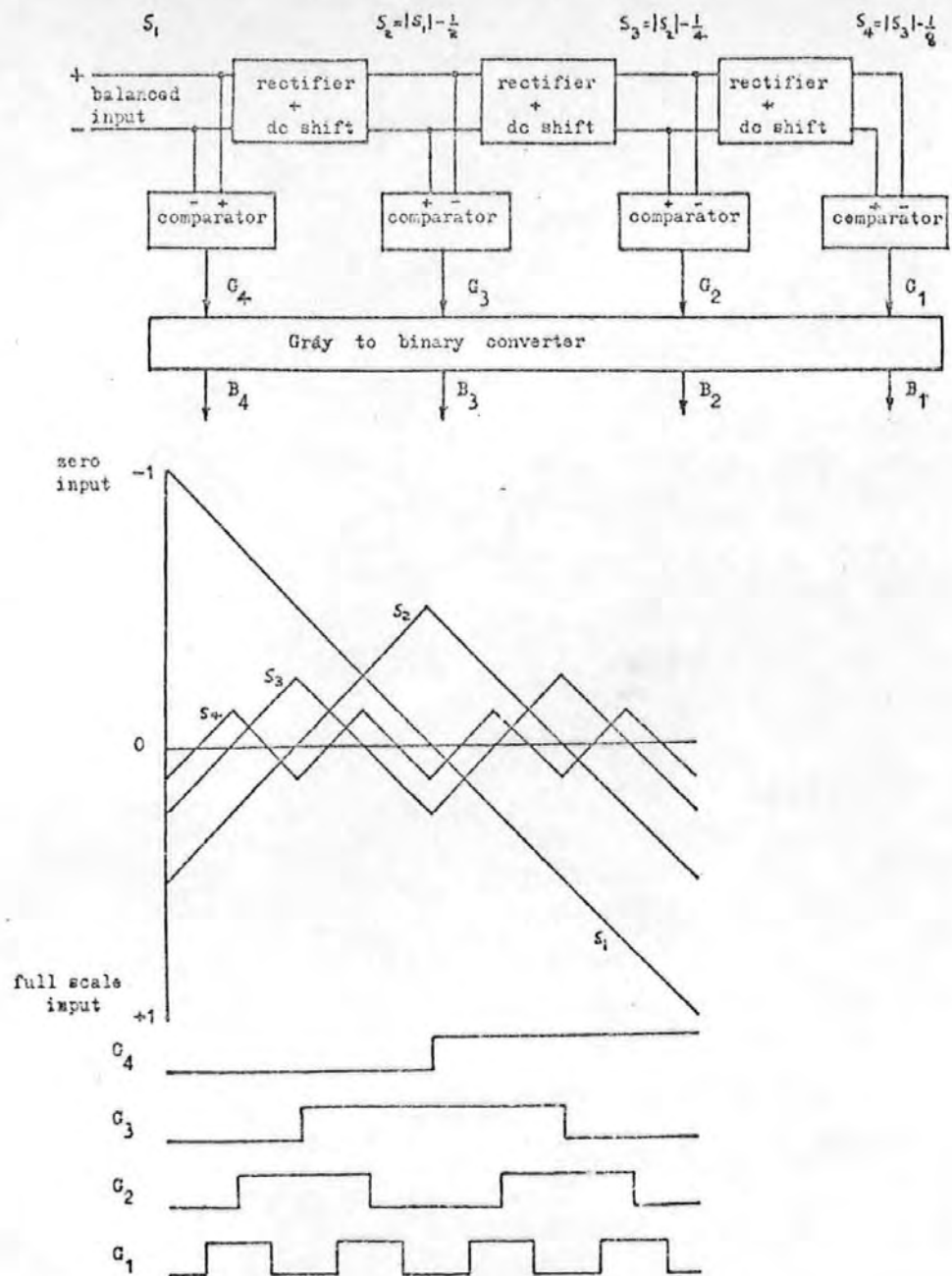
$$N = 2c + g = 5 \text{ uc} \quad (2.3)$$

Hence, for video encoding the logic speeds are again quite modest although, due to the cascaded comparators the technique is probably better classified as a fast hybrid encoder rather than a parallel encoder. TEESDALE and WESTON's 8-digit 81 level encoder used 28 comparators and 3 AND gates for every 2 comparators so in general the complexity can be written as

$$E = [3^{(\frac{n}{2}-1)} + 1][c + 3g/2] \quad (2.4)$$

The basic equipment required to encode 81 levels into NEU's 'C' code is then only 98uc and this is a considerable reduction when compared with a

Fig. 2.2: Folding encoder (EDSON and HENNING<sup>21</sup>)



parallel encoder having about the same resolution. Also, encoding errors resulting from an indecisive threshold are restricted to 1 LSD since NEU's 'C' code is a unit distance code. However, it must be remembered that for studio applications code conversion would be required thereby increasing the complexity considerably above 98uc.

The 'folding' encoder<sup>56</sup> is a particularly elegant solution to the problem of video encoding since, in principle at least, it offers the speed of a parallel encoder whilst having the complexity of a sequential or serial encoder. This is obviously an oversimplification and in practice the encoder is somewhat slower than the parallel encoder or the TEESDALE and WESTON encoder and it is somewhat more complex than a sequential encoder, especially if the output code is to be the binary number code. Not surprisingly it has been termed a parallel encoder<sup>51</sup> and a cascaded (sequential) encoder<sup>26</sup> but it would seem to fit best into the above classification as a hybrid encoder. The principle is illustrated in Fig. 2.2. Full wave rectification of the input signal together with a suitable dc shift gives a 'folded' characteristic from which it can be shown that the output is in Gray code. Therefore, for studio applications the basic equipment must include Gray to binary conversion logic. The Boolean expression for the  $(n-1)^{th}$  binary digit is

$$B_{n-1} = (G_{n-1} \cdot \overline{B_n}) + (\overline{G_{n-1}} \cdot B_n)$$

where  $B_n$  is a more significant digit than  $B_{n-1}$ . Clearly, as soon as  $G_{n-1}$  is generated  $B_{n-1}$  can be generated so that code conversion should not affect the encoding speed since it can proceed in parallel with the generation of each Gray digit. Assuming complementary Gray and binary outputs are available the complexity of an  $n$ -digit converter is

$$E = 3ng = 3n \text{ uc}$$

Despite the apparent simplicity of the folding encoder, implementation is difficult and it was not until WALDHAUER<sup>57</sup> described a near ideal rectifier circuit that the encoder could be used for video encoding. WALDHAUER placed rectifiers in the feedback path of a high gain operational amplifier so that the rectifiers in Fig. 2.2 are in fact quite complex for a video encoder. Each amplifier comprises an lf and hf section in parallel. The hf section comprises a 4-stage wideband amplifier and the delay through the amplifier is assumed to be approximately twice the delay of a corresponding logic gate, for a particular technology. Each rectifier actually comprises 2 such amplifiers in a balanced arrangement and the rectifier is assigned 4uc in Table 2.1. Thus we can express the equipment for a folding encoder delivering binary number code as

$$E = n(c + r + 3g) - r = 9n - 4 \text{ uc} \quad (2.5)$$

Assuming that all n-digits per sample are derived in one sample period and that code conversion proceeds as encoding proceeds, the number of sequential operations per sample period is

$$N = C + (n-1)r = 2n \text{ uc} \quad (2.6)$$

where 'c' here represents the last analog comparator. To compare the folding encoder with TEESDALE and WESTON's encoder we neglect the code conversion logic and select a value of n to give about the same number of quantizing levels. For the folding encoder this gives

$$E \approx 35 \text{ uc}$$

Comparing this with eqn. (2.4), and eqn. (2.6) with eqn. (2.3) we can conclude that TEESDALE and WESTON's encoder is roughly 3 times as complex as



the folding encoder although it is probably somewhat faster. Nevertheless, the folding encoder is still extremely fast and well suited for video encoding as demonstrated by EDSON and HENNING<sup>21</sup> in 1965. This appears to be the first report of a solid-state encoder capable of handling colour television (NTSC) signals. The encoder sampled at a 12MHz rate and it had a theoretical 9-digit resolution although the actual resolution was nearer to 8-digits due to instrumental imperfections.

A 'straight' hybrid encoder could be defined as a series-parallel encoder that derives  $m$ -digits at a time in  $n/m$  cascaded stages and all  $n$  digits are derived in one sample period. In Fig. 2.3 the last  $m$  digits would be derived at the end of the sample period and all  $n$ -digits could then be read out into a buffer register (which is not included in the basic equipment). Referring to Fig. 2.3 the equipment and operating speed can be given as

$$E = \frac{n}{m} \left[ (2^m - 1)c + e \right] + \left[ \frac{n}{m} - 1 \right] [d + q] \quad (2.7)$$

$$N = \frac{n}{m} [c + e] + q + d \quad (2.8)$$

In practice the quantizer 'q' and subtractor 'd' can be combined into a single wideband operational amplifier circuit as for example in a BBC 8-digit hybrid video encoder (DEVEREUX<sup>25</sup>). However, as TIESDALE and WESTON point out, this amplifier is subject to large step inputs for successive samples of large hf signals and the amplifier output settling time could be excessive. The BBC encoder did in fact suffer from this problem and the effect was to decrease the signal to quantizing noise ratio. From the data given by DEVEREUX this problem can be characterised by assigning  $5\mu\text{s}$  to represent the delay of the circuit. Also, the complexity of the difference amplifier can be represented by

$$E = \frac{n}{4} + 2 \quad \mu\text{s}$$



Using these values and also Table 2.1 we obtain for the straight hybrid encoder

$$E = \frac{n}{m} \left[ 2(2^m - 1) + 2^{\frac{n}{2}} \right] + \left[ \frac{n}{m} - 1 \right] \left[ \frac{n}{4} + 2 \right] \text{ uc} \quad (2.9)$$

$$N = 4 \frac{n}{m} + 5 \text{ uc} \quad (2.10)$$

where N represents the number of sequential operations required in one sample period (i.e. to completely encode one sample). For an 8-digit straight hybrid encoder with  $m = 4$  these equations reduce to

$$E = 96 \text{ uc} , \quad N = 13 \text{ uc}$$

Comparing these results with eqns. (2.5) and (2.6) we see that the straight hybrid encoder has about the same speed as a folding encoder delivering the same code and having the same resolution. However, the straight hybrid is significantly more complex and these calculations illustrate the relative sophistication of the folding encoder. To illustrate the practical significance of these calculations, assume that the actual encoding time is 60ns as before. This means that logic gates must have less than 5ns propagation delay and a comparator must accurately resolve an analog level within approximately 10ns. Whilst this is not unreasonable, these requirements can be relaxed by using a 'production-line' technique, a technique which can be applied to hybrid encoders and to some sequential encoders.

A production line encoder (sometimes referred to as a 'propagation' encoder<sup>59</sup>) can be defined as one in which the first stage starts operating on a new sample while previous samples are still undergoing conversion in later stages. The time required to convert a sample can then be spread over several sample periods thereby easing circuit speed requirements and providing increased settling time. In fact, DEVEREUX's encoder took over 3 sample

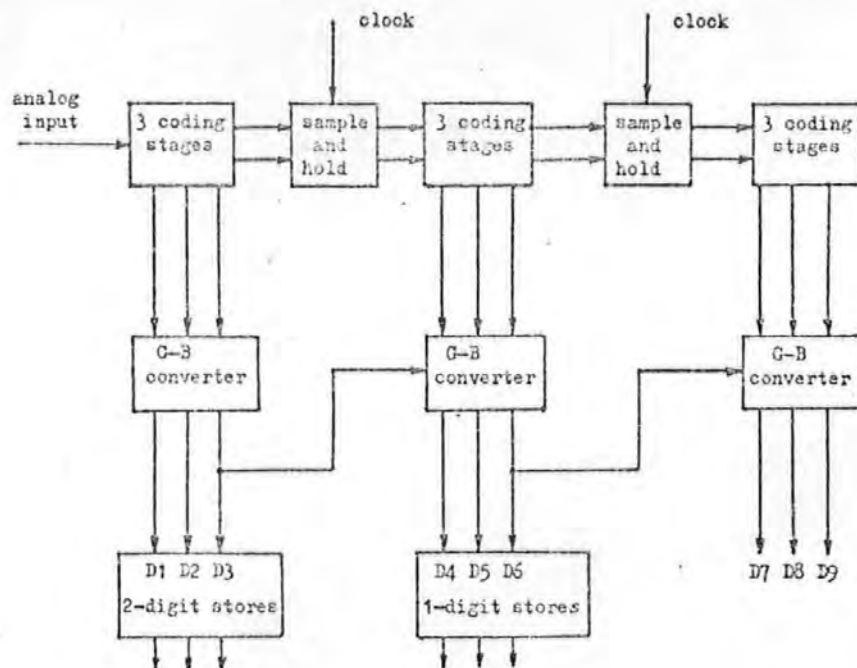


Fig.2.4 :hybrid encoder using folding and propagation techniques  
(PEARCE and MAYS<sup>59</sup>)

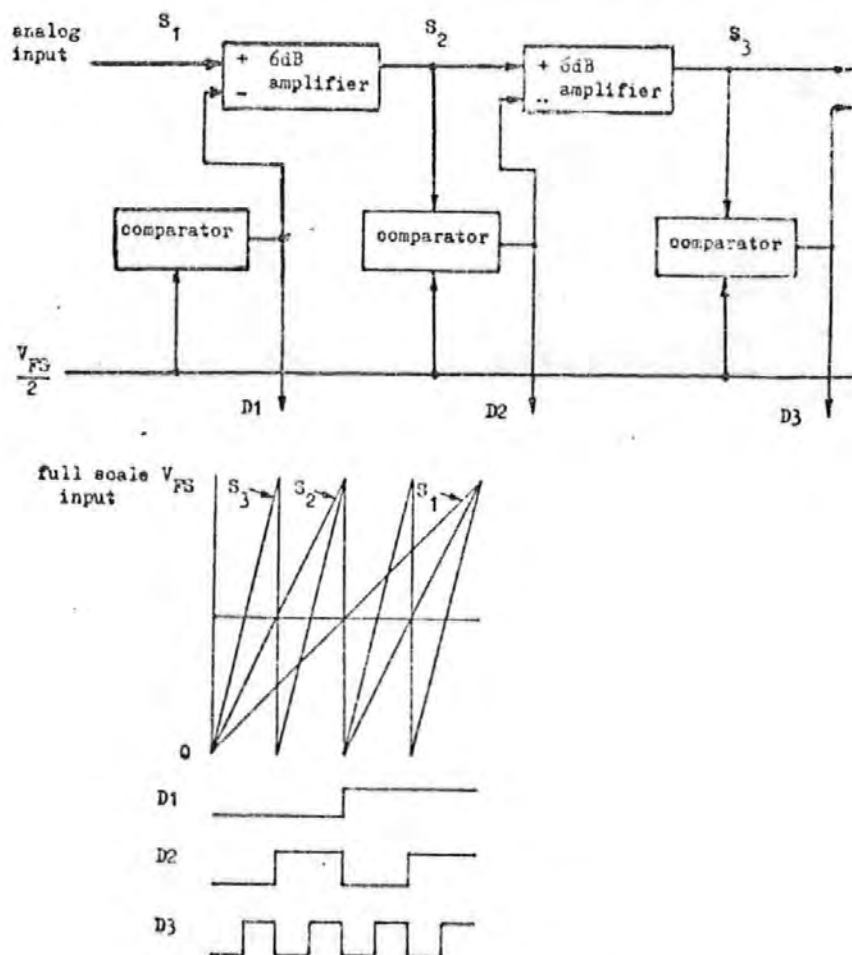


Fig.2.5 :non-programmed sequential encoder (BROWN<sup>22</sup>)

periods to encode one sample and the timing scheme was such that the operations of quantization, subtraction and level comparison had to be achieved within about one sample period. That is,

$$N = (q + d) + c = 7 \text{ } \mu\text{s} \quad (2.11)$$

In this case the production line technique appears to double the encoding speed, approximately. However, this advantage must be paid for as an essential feature of any production line encoder is information storage. Referring to Fig. 2.3 it is apparent that the  $m$  binary digits from encoding logic 1 must be stored to prevent them from being overwritten before they are read out with the remaining  $n-m$  digits. (In a straight hybrid encoder the digits could simply remain in logic 1 until all digits had been resolved and then all digits could be read out simultaneously at the end of the sample period.) The extra equipment required to store  $m$  binary digits is simply

$$E = mf = 2m \text{ } \mu\text{s}$$

The output register into which all digits are read simultaneously at the end of the encoding period is not included in this calculation to make it compatible with previous calculations. The complexity of DEVEREUX's encoder now becomes, from eqn. (2.9)

$$E = 104 \text{ } \mu\text{s} \quad (n=8, m=4)$$

PEARCE and MAYS<sup>59</sup> have implemented a similar hybrid encoder. Their basic system comprises three, 3-digit folding encoders cascaded to realise a 9-digit encoder, Fig. 2.4. The residue from each group of stages is sampled and held for the coding of the next MSD's and for an  $n$ -digit encoder generating  $m$  digits per stage the storage required is

$$E = m f \sum_{i=1}^{n/m} \left( \frac{n}{m} - i \right)$$

In addition, Gray to binary conversion is required if the encoder is intended for studio applications so the basic equipment required for PEARCE and MAY's encoder is

$$\begin{aligned}
 E &= \frac{n}{m} \left[ mC + (m-1)r \right] + \left( \frac{n}{m} - 1 \right) h + 3ng + mf \sum_{i=1}^{n/m} \left( \frac{n}{m} - i \right) \quad (2.12) \\
 &= 9n - 2\frac{n}{m} - 2 + 2m \sum_{i=1}^{n/m} \left( \frac{n}{m} - i \right) \quad \text{uc} \\
 &= 91 \quad \text{uc} \quad (n=9, m=3)
 \end{aligned}$$

In comparison, the equipment required for EDSON and HENNING's 9-digit folding encoder, including Gray to binary conversion, is 77uc.

The encoder is extremely fast. Assuming for example that 3 digits are resolved in one sample period ( $m = 3$ ) then the maximum number of sequential operations per sample period is

$$N = C + (m-1)r = 6 \text{ uc} \quad (2.13)$$

Thus, a relatively few operations could span the complete sample period (less the acquisition time) and the circuit speed requirements are quite modest.

### 2.3 SEQUENTIAL VIDEO ENCODERS

Sequential encoding is inherently simpler than hybrid encoding although the technique is restricted to codes which can be generated in sequence i.e. digit  $a_j$  of a code character  $a_1 \dots a_n$  has to be completely defined by preceding digits  $a_1 \dots a_{j-1}$  and independent of the following digits  $a_{j+1} \dots a_n$ . Fortunately for video applications this requirement is satisfied by the binary number code since, following CATTERMOLÉ<sup>51</sup>, digit

$a_j$  can then be expressed in terms of the analog input  $x$  as

$$a_j = \text{int} \left[ \frac{1}{2^{n-j}} \left( x - \sum_{i=1}^{j-1} a_i 2^{n-i} \right) \right]$$

- assuming uniform quantizing and  $0 < x < 2^n$ . Not surprisingly several attempts have been made to implement sequential video encoders; BROWN<sup>22</sup> implemented a 'non-programmed' sequential encoder in 1962 and JOHANNESSEN<sup>26</sup> implemented a 'programmed' sequential encoder in 1970.

### 2.3.0 NON-PROGRAMMED ENCODER

The non-programmed encoder is sometimes referred to as the cascaded, serial, or open loop successive approximation encoder (since the binary output successively approximates to the corresponding analog input). It is the limiting case of the hybrid encoder ( $m = 1$ ) and so comprises  $n$  cascaded stages, Fig. 2.5. As shown in the figure, it is usual in this type of encoder to amplify the residue from each stage by 6dB (so that a common reference  $V_{FS}/2$  can be used) and to combine the 6dB amplifier and subtraction node. The design of these difference amplifiers can be critical since, like most binary number encoders the sequential encoder generates large transients for certain changes in code character. Consider a ramp input for Fig. 2.5. As  $s_1$  increases slightly above  $V_{FS}/2$ ,  $D_1$  is set to  $V_{FS}/2$  and residue  $s_2$  is rapidly returned to zero whereas, in contrast, the residue  $s_2$  in Fig. 2.2 is 'folded over' and changes only relatively slowly. Clearly the settling time of the rectifier stages in the folding encoder should be significantly lower than the settling time of the difference amplifier in the sequential encoder and this is represented accordingly in Table 2.1. We can now estimate the complexity and speed of the non-programmed sequential encoder

$$E = nC + (n-1)d = 4n-2 \quad uc \quad (2.14)$$

$$N = nC + (n-1)d = 7n-5 \quad vo \quad (2.15)$$

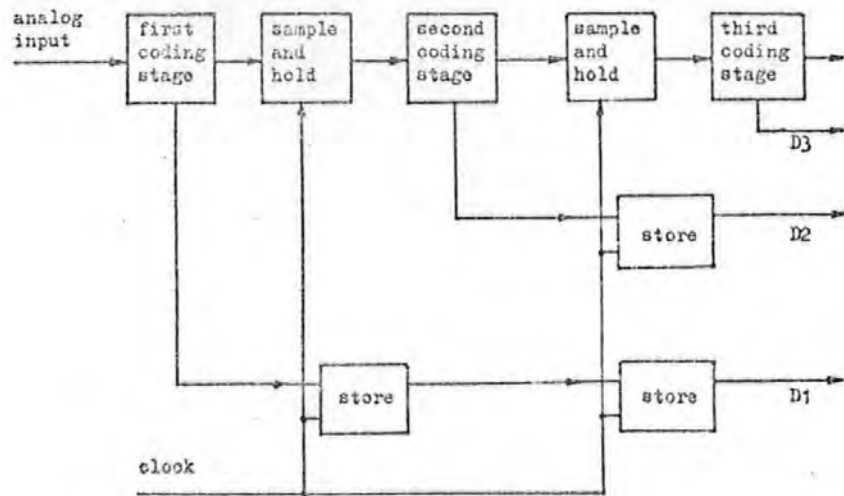


Fig.2.6 :non-programmed sequential encoder with extended production line technique(suggested by PEARCE and KAY<sup>29</sup> )

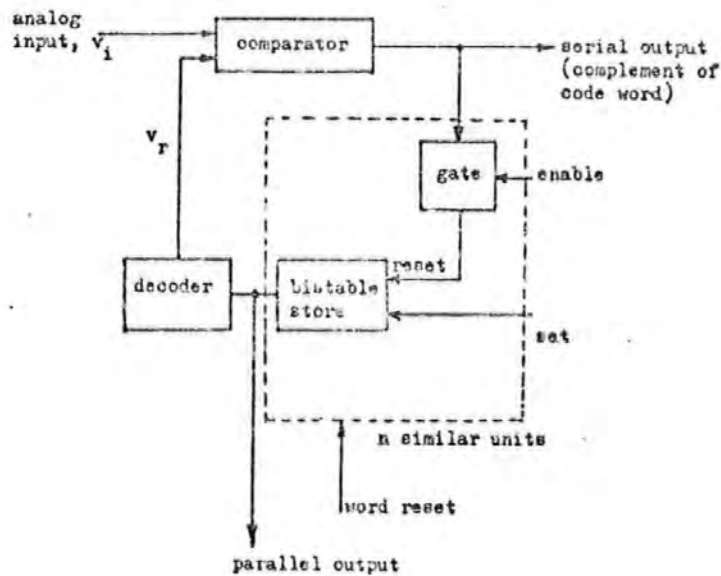


Fig.2.7 :programmed sequential encoder (JOHANNESEN<sup>26</sup>)

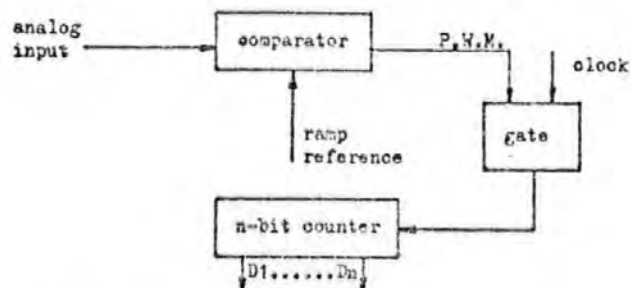


Fig.2.8 elementary Pulse Width Modulator



For 8-digit encoding  $E = 30u_0$  and  $N = 5u_0$  which suggests that the sequential encoder is significantly less complex than a folding encoder having the same resolution and delivering the same output code (eqn. 2.5). Primarily the higher complexity arises from the need for code conversion and, to a lesser extent, from the fact that each rectifier stage is probably about twice as complex as each difference amplifier in the sequential encoder.

However, the straight non-programmed sequential encoder as described here is much slower than the folding encoder, perhaps by a factor of 3 or more and to realise an 8-digit video encoder using this technique would require very high circuit speeds. Assuming all 8-digits are encoded in 60ns gives only 1.2ns/ $u_0$  and it is surprising that this technique was used to implement the first solid state video encoder (BROWN<sup>22</sup>).

The encoder shown in Fig. 2.5 requires  $n-1$  high speed differential amplifiers each with a delay of only  $5u_0$  or about 6ns. The amplifier speed requirements can be relaxed by employing a 2-step production-line technique; the first  $n/2$  digits could be generated by sequential coding and the residue could be stored in a sample and hold circuit after one sample period. The first  $n/2$  digits are then stored until the remaining digits are generated at the end of the second sample period. This gives

$$N = \frac{n}{2}(c+d) = 3.5n \quad u_0 \quad (2.16)$$

$$E = n(c+d + f/2) + h-d = 5n \quad u_0 \quad (2.17)$$

This procedure could be further extended until each digit takes one sample period to be resolved as suggested by PEARCE and MAYS<sup>59</sup>, Fig. 2.6. The speed of this encoder approaches that of the parallel encoder in that the only sequential operations per sample period are those of voltage comparison and subtraction i.e.

$$N = c+d = 7 \quad u_0 \quad (2.18)$$

From Fig. 2.6 it is clear that the total storage (excluding any buffer register) can be written as

$$E = f \cdot \sum_{i=1}^n (n-i)$$

and since each coding stage represents a comparator and difference amplifier the total equipment is

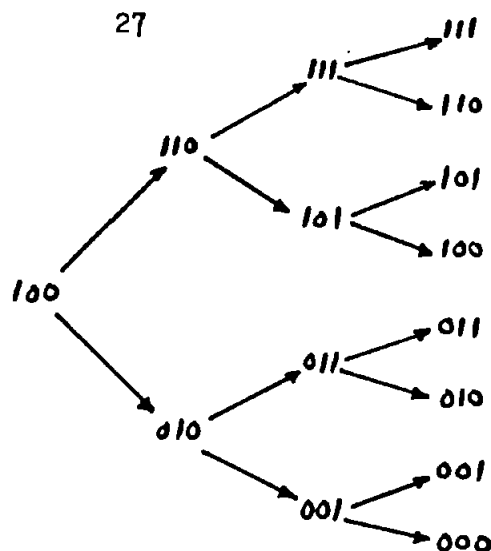
$$\begin{aligned} E &= nc + (n-1)(d+h) + f \cdot \sum_{i=1}^n (n-i) & (2.19) \\ &= 6n - 4 + 2 \sum_{i=1}^n (n-i) & uc \\ &= 122 \quad uc & (n=9) \end{aligned}$$

Referring to eqn. (2.12) it is clear that this encoder is inferior to a hybrid encoder having the same resolution and a similar conclusion was arrived at by PEARCE and MAYS.

### 2.3.1 PROGRAMMED ENCODER

The basic programmed encoder used by JOHANNESSEN<sup>26</sup> is shown in Fig. 2.7 and the name derives from the fact that the sequence of operations is 'programmed' by the timing system. Initially the MSD of the store is set to 1 and this is decoded to give  $V_r = V_{FS}/2$ . Supposing  $V_i < V_r$ , the comparator gives a reset pulse to correct the store and the next MSD is then set to 1 by the timing system to give  $V_r = V_{FS}/4$ , and so on. The process is illustrated below for a 3-digit word.

programmed  
sequential encoding  
process



The encoder speed depends upon the propagation delay around the loop and therefore upon the number and type of loop operations. The number of sequential unit operations per sample period is given by

$$N = n(f + g + c + q) = 10n \quad \text{uo} \quad (2.20)$$

Comparing eqn. (2.15) with eqn. (2.20) provides quantitative support for the view of JOHANNESSEN and others<sup>59</sup> that the programmed encoder is probably slower than the non-programmed encoder. Although JOHANNESSEN intended his encoder for television he did not implement a sample and hold circuit and so he could not encode video signals. However, allowance was made for the acquisition time of a sample and hold circuit since for a 12.3MHZ sampling rate the actual encoding time was 63ns. For 8-digit encoding this corresponds to only 0.8ns/uo and subnanosecond logic is mandatory. JOHANNESSEN used hot carrier diodes, SRD's, uhf transistors and a tunnel diode comparator in simple and miniaturised circuitry. Nevertheless, his implementation was for only 7-digits and only 6-digit resolution is claimed for the practical encoder.

Neglecting any clock generation equipment as in previous estimates the complexity can be expressed as

$$E = c + q + n(f + g) = 3.5n + 2 \quad \text{uc} \quad (2.21)$$

This indicates that the programmed encoder has about the same complexity as the non-programmed encoder and again provides quantitative support for JOHANNESSEN's view that the programmed encoder is considerably simpler than the folding encoder (eqn. (2.5)).

## 2.4 COUNTING ENCODERS

Counting is fundamental to the operation of many types of encoder and this generally results in encoders of extremely low if not minimal complexity. However, some of these encoders such as those of BOUTMY<sup>61</sup> and INGRAM<sup>62</sup> and that of McNEILLY<sup>63</sup> are based upon exponential rather than ramp waveforms and so give non-linear quantization which is not suitable for the application under consideration. Furthermore, the elementary counting encoders that use ramp waveforms, such as the voltage to frequency encoder, the pulse width modulator encoder<sup>64</sup> and the counter ramp encoder all scan the code raster a level at a time and so are prohibitively slow for video applications.

To illustrate, consider an elementary counter ramp encoder comprising AND gate, synchronous counter, decoder and comparator in a closed loop. Then

$$E = g + b + q + c = 2.5n + 3 \quad \mu c \quad (2.22)$$

$$N = (2^n - 1)(g + b + q + c) = 11(2^n - 1) \quad \mu c \quad (2.23)$$

(the delay through the counter is generally determined by a gate cascaded with a bistable and so the counter is assigned  $3\mu c$ ). Clearly the advantage of minimal complexity is offset by the unrealistic circuit speeds required, around  $0.02\text{ns}/\mu c$  for 8-digit video encoding. A counter ramp encoder using a 2-step production-line technique is more realistic. One possibility is to

derive the first  $n/2$  most significant digits during the first sample period and then this information is used to derive the remaining  $n/2$  digits during the second sample period; therefore several samples are processed simultaneously on a production line basis. This gives

$$N = \left( 2^{n/2} - 1 \right) u_0$$

and for 8-digit video encoding corresponds to about 0.35ns/ $u_0$  having allowed for the sample and hold time. This is about twice the circuit speed attempted by JOHANNESSEN and so is regarded as impractical even using a tunnel-diode comparator, E.C.L, a synchronous counter and a fast weighted current decoder.

#### 2.4.0 THE PULSE WIDTH MODULATOR

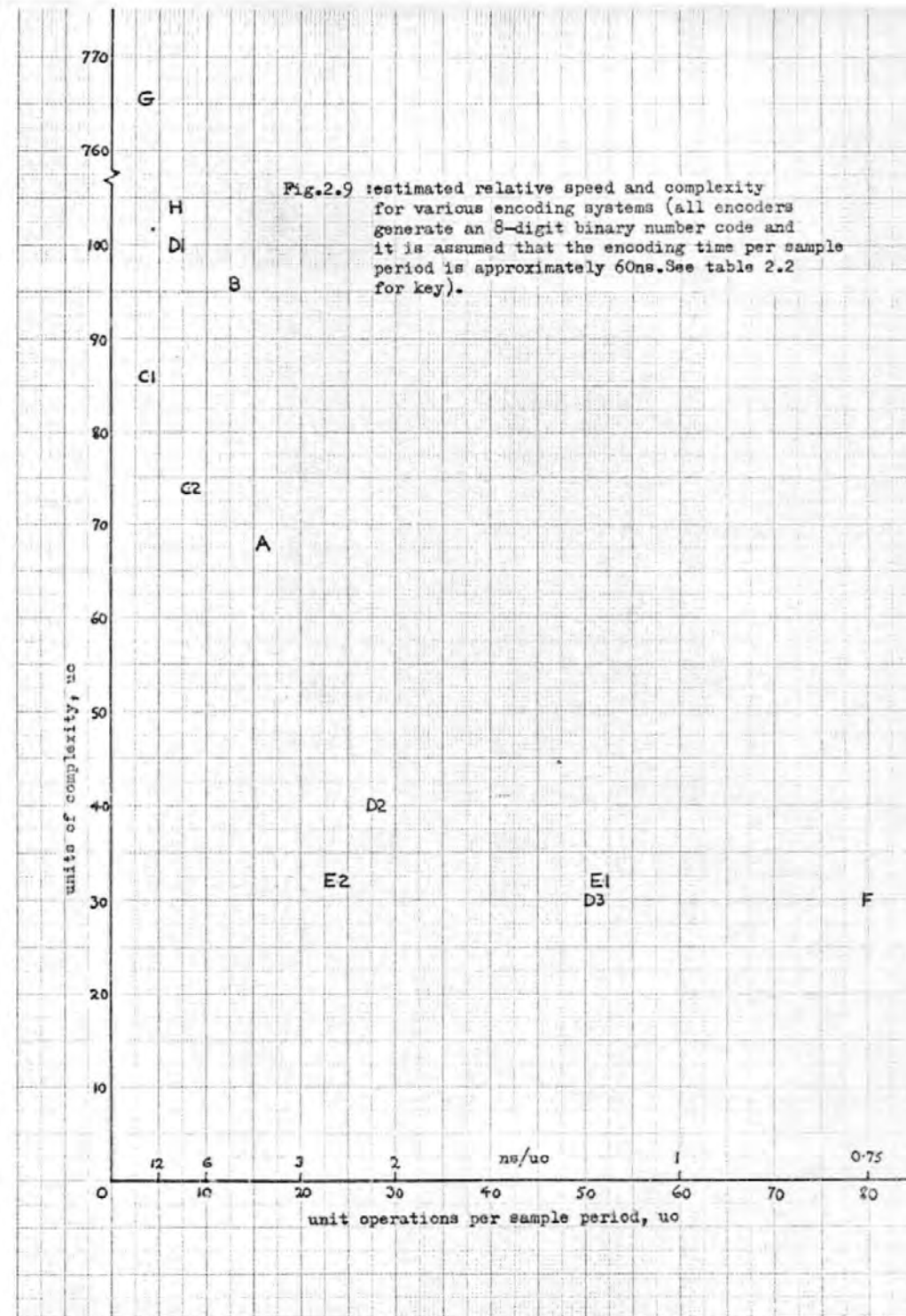
It is proposed in this thesis that a counting type video encoder can be realised by adopting an open loop system such as the elementary pulse width modulator (P.W.M.) encoder (Fig. 2.8) and by using a 2-step production-line technique.

Qualitatively the open loop system is more feasible than the counter ramp encoder because the count does not have to be decoded before the next level in the code raster is scanned. This has important practical implications since the counter specification can be relaxed and readily available high-speed asynchronous counters can be used. To assess the P.W.M. video encoder quantitatively the maximum possible number of sequential unit operations per sample period must be determined. This is mainly determined by the maximum possible number of counter bistable operations and is given by the sum of the distances 'd' between code characters over the complete code raster. Since a 2-step production-line technique is envisaged then the counter in each elementary P.W.M. encoder counts to only  $2^{n/2} - 1$ . Hence, a reasonable

TABLE 2.2

KEY TO FIG. 2.9

- A folding encoder with Gray to binary conversion (EDSON and HENNING<sup>21</sup>)
- B straight hybrid or series parallel encoder ( $m = 4$ )
- C1 hybrid folding encoder with Gray to binary conversion ( $m = 2$ ) (similar to PEARCE and MAYS<sup>59</sup>)
- C2 hybrid folding encoder with Gray to binary conversion ( $m = 4$ ) (similar to PEARCE and MAYS<sup>59</sup>)
- D1 non-programmed sequential encoder using extended production-line technique (suggested by PEARCE and MAYS<sup>59</sup>)
- D2 non-programmed sequential encoder using 2-step production-line technique
- D3 non-programmed sequential encoder (BROWN<sup>22</sup>)
- E1 pulse width modulator video encoder using 2-step production-line technique
- E2 modified pulse width modulator video encoder (discussed in chapter 7)
- F programmed sequential encoder (JOHANNESSEN<sup>26</sup>)
- G solid-state parallel encoder
- H hybrid encoder using production-line technique (DEVEREUX<sup>25</sup>)





estimate of  $N$  is

$$N = 2 \sum_{i=1}^{2^{n/2} - 1} (d_i) \quad u_0 \quad (2.24)$$

For 8-digit video encoding this gives  $N = 52u_0$  and corresponds to about  $1.1ns/u_0$ , allowing for the sample and hold time.

A P.W.M. video encoder using a 2-step production-line technique requires, in its simplest form, two elementary P.W.M. encoders, a store and decoder for the first  $n/2$  digits and a one-sample period delay. Neglecting the delay (which could be provided by a delay cable) the complexity can be written as

$$E = 2(c + g + b) + q + nf/2 = 6 + 13n/4 \quad uc \quad (2.25)$$

The complexity is therefore about the same as JOHANNESSEN's sequential encoder (eqn. (2.21)) for the same resolution.

## 2.5 SUMMARY

Fig. 2.9 summarizes the above analysis for video encoders generating an 8-digit binary number code. Clearly there is a region of uncertainty around each point and the graph is considered to represent the mean coordinates for each system since an attempt has been made to select the mean or typical weighting factors (Table 2.1). As an example of the expected spread in coordinates, increasing the delay of the voltage comparison operation by 50% (to  $3u_0$ ) causes between 0 and 15% increase in the horizontal coordinates. Such a change does not affect the broad conclusions set out below:

1. There is a useful trade-off between encoder complexity and circuit speed (following an approximately hyperbolic law) and the complexity of existing video encoders (H,C,A) could probably be reduced by a factor of 3 by

applying presently available high speed logic.

2. All video encoding techniques considered require relatively high speed logic (compared to MOS logic for example) ranging from about 15ns propagation delay per gate for system G to about 0.75ns delay per gate for system F. DEVEREUX's encoder (H) uses TTL having gate delays of typically 8ns whilst, in the form described, JOHANNESEN's encoder (F) requires subnanosecond logic and is probably still unsuitable for 8-digit video encoding.
3. Clearly system G is far too complex whilst the hybrid folding encoder of PEARCE and MAYS (system C) is perhaps only 80% as complex as DEVEREUX's encoder for the same circuit speed requirements. EDSON and HENNING's folding encoder is even less complex although it probably requires faster logic.
4. Systems E1, D2, and D3 appear, on this analysis, to be significantly less complex than existing video encoders whilst not requiring circuit speeds as high as those attempted by JOHANNESEN. However, even for system D2 the comparator propagation delay must be less than 4 or 5ns and no IC comparators having this specification were available at the commencement of this work. Therefore, since 8 discrete component comparators are required for systems D2 and D3 these systems were rejected in favour of system E1 (which requires only 2 comparators). System E1 is also more digital in nature and this is considered an advantage.

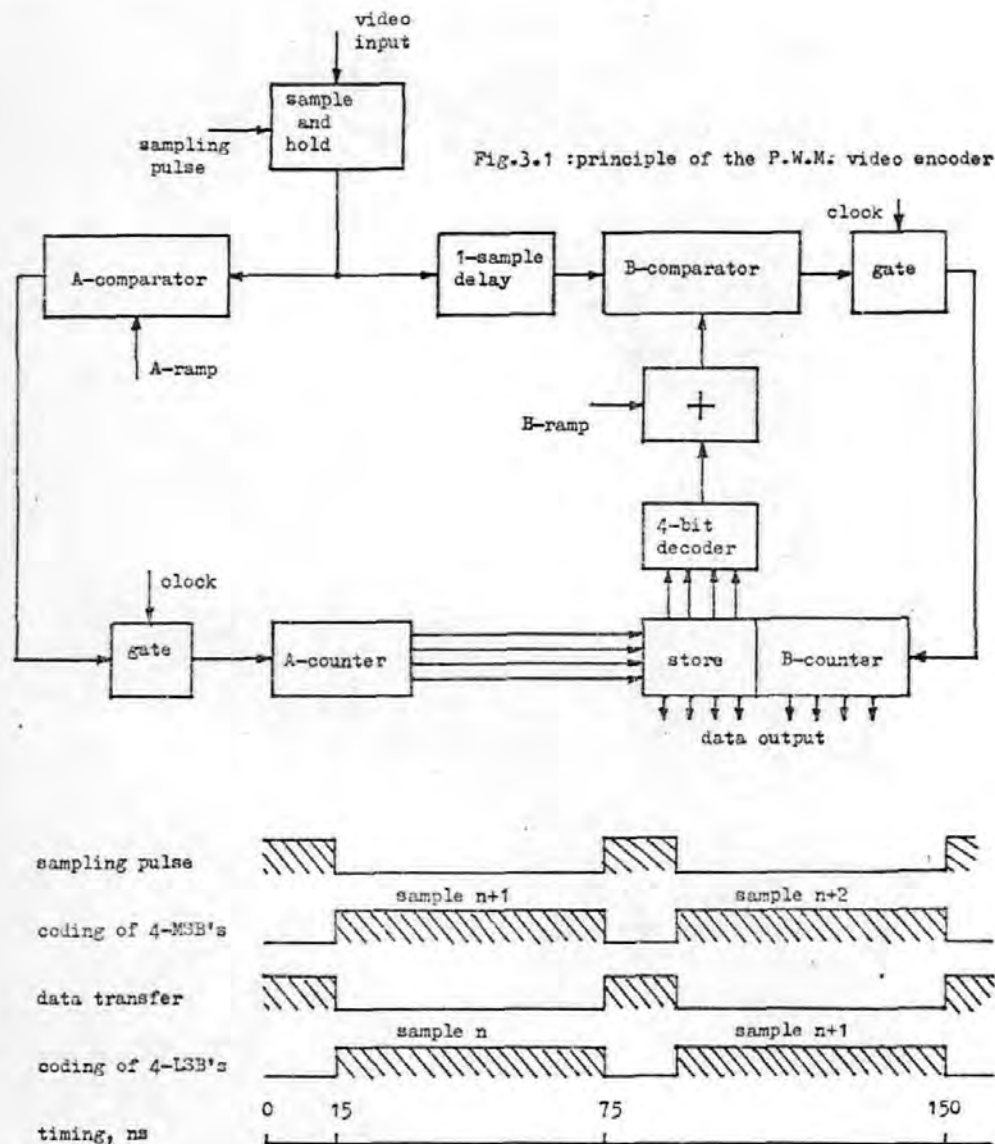
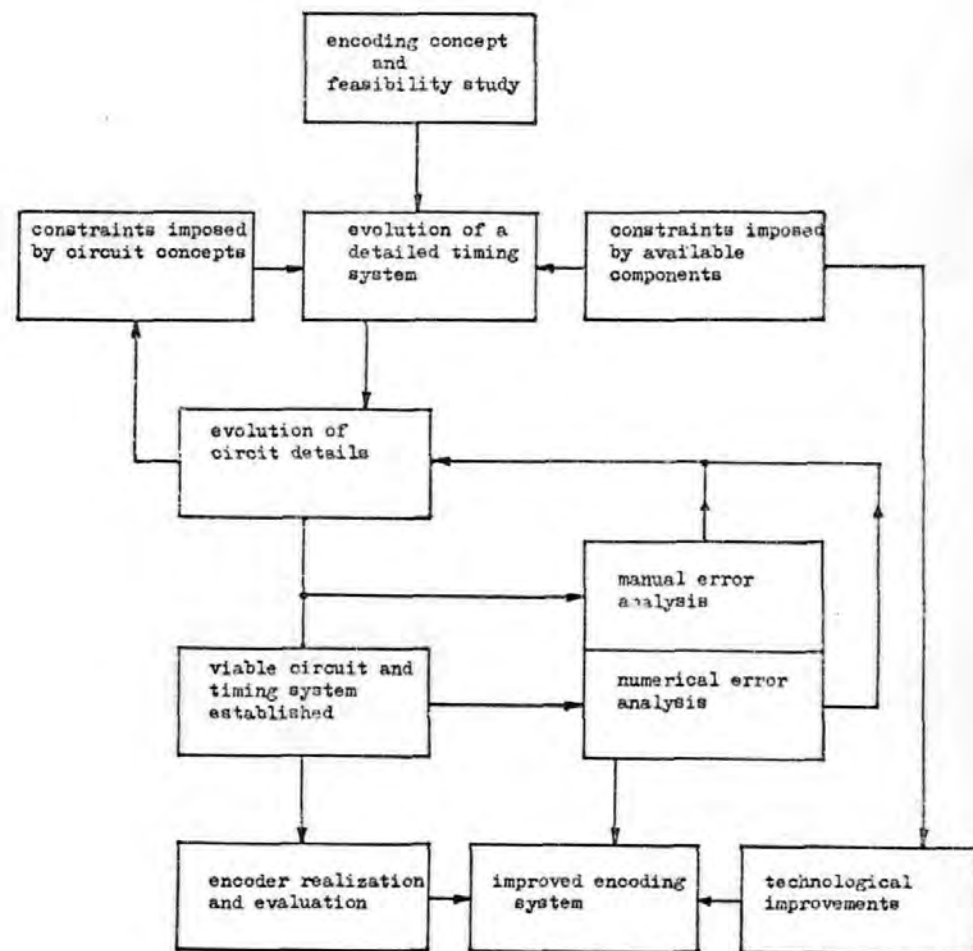


Fig.3.2 :encoder design philosophy



### CHAPTER 3: THE PULSE-WIDTH MODULATOR VIDEO ENCODER

#### 3.0 ENCODING PRINCIPLE AND DESIGN PHILOSOPHY

It was shown in section 2.4 that the pulse-width modulator could probably be incorporated into a 2-step encoding system for video signals and that this approach offered one of the simplest video encoding schemes consistent with state of the art circuit techniques. The principle of such a system is illustrated in Fig. 3.1; the 4 MSB's of sample  $n+1$  are derived during the same period as the 4 LSB's of sample  $n$  and the acquisition time of the sample and hold gate is then used as a data transfer period during which time the following sequential operations take place

- (a) data corresponding to sample  $n$  are readout
- (b) the 4 MSB's corresponding to sample  $n+1$  are transferred to store
- (c) the new data in store are decoded to provide a reference level for the coding of the 4 LSB's of sample  $n+1$
- (d) the A and B counters and A and B comparators are reset.

The encoder cycle is repeated by coding the 4 MSB's of sample  $n+2$  simultaneously with the 4 LSB's of sample  $n+1$ . The conversion rate is typically  $13 \cdot 3 \cdot 10^6$  samples per second, which is extremely high for pulse width modulators, and the conversion delay is typically 150ns.

A reasonable summary of the design philosophy is shown in Fig. 3.2. A detailed timing system was evolved before any major circuit design commenced although clearly, the timing had to be related to the capabilities of modern high-speed components and to the circuit concepts used. The circuit details could then evolve and minor changes were made to the timing system as dictated by the circuit. The whole iterative process involved much experimental work.

An error consciousness was maintained throughout the design and generally attempts were made to keep voltage errors below 1 quantum ( $q$ ) - this is an intuitive figure since it is virtually impossible to assess the effect of an error at this stage. Ideally of course we could express the codeo output  $V_o$  in terms of the input  $V_i$  and circuit parameters  $x_i$ , i.e.

$$V_o = f(x_1, x_2, \dots, x_i, V_i) \quad (3.1)$$

and the effect of single or multiple error could be deduced from the total differential  $dV_o$ . Clearly this analytical approach is intractable and the above intuitive approach had to suffice until a viable and complete circuit design had been established. At this point a numerical solution to eqn. (3.1) is feasible (chapters 5 and 6). Finally, technological improvements would hopefully enable much of the encoder to be realised in integrated circuit form and this, together with experimental and computer results, could lead to an improved encoding system.

### 3.1 TIMING SYSTEM

With reference to Fig. 3.1 an estimate of the clock frequency required for an  $n$ -digit PWM video encoder can be written as

$$f_c = \frac{2^{n/2} - 1}{t_s - t_a} \quad (3.2)$$

where  $t_s$  and  $t_a$  correspond to the sample period and the sample and hold acquisition time respectively. Assuming a sampling frequency of exactly 3 times subcarrier frequency (approximately 13.3MHz) then  $t_s \approx 75\text{ns}$ . For this sampling frequency, acquisition times as large as 25ns have been used for video encoding<sup>25</sup> and using these values eqn. (3.2) gives  $f_c \approx 300\text{MHz}$ . This is not unreasonable since the fastest IC bistable available at the time of design had a maximum toggle frequency of 325MHz and this bistable formed the

basis for a fast IC asynchronous 4-bit counter and a fast IC bi-quinary counter. However, a somewhat lower clock frequency was selected since it was considered that the above acquisition time could be reduced significantly. Also, the pulse width modulator principle dictates that, for a constant analog input, a strict time relationship should be maintained between the comparator output pulse and the clock pulses to the counter. In other words the 13.3MHz ramp reference waveform to each comparator must be phase locked to the clock and this is best achieved by frequency division from a v.h.f. clock generator; using the above mentioned IC's a suitable division ratio is 20. The clock frequency was therefore chosen as the 60<sup>th</sup> harmonic of subcarrier frequency or about 266MHz and a phase-lock loop was incorporated in order to lock the clock generator to colour subcarrier.

The coding interval spans 15 clock periods so that  $t_a$  and the data transfer time must be 5 clock periods or about 18.8ns. In fact,  $t_a$  is made somewhat less than this to allow sampling gate switching transients to settle and a 15ns acquisition time was chosen.

Studies of nanosecond pulse generation techniques using step recovery diodes (S.R.D.) showed that it is not too difficult to define pulse timing and pulse duration to better than 1ns. This fact together with the availability of high speed logic (ECL) capable of handling a 266MHz clock rate meant that the critical timing system outlined in Fig. 3.1 was probably feasible providing a high-speed analog comparator could be realised. The comparator is in fact one of the major circuit problems and the comparator requirements are briefly considered below. Firstly, the comparator propagation delay should be less than one clock period (nominally 3.76ns) implying at the outset that the comparator should be wideband and relatively simple. In this respect the work of SCHINDLER<sup>41</sup> and JOHANNESSEN<sup>26</sup> indicated that the comparator might be realised using a wideband differential amplifier working in conjunction



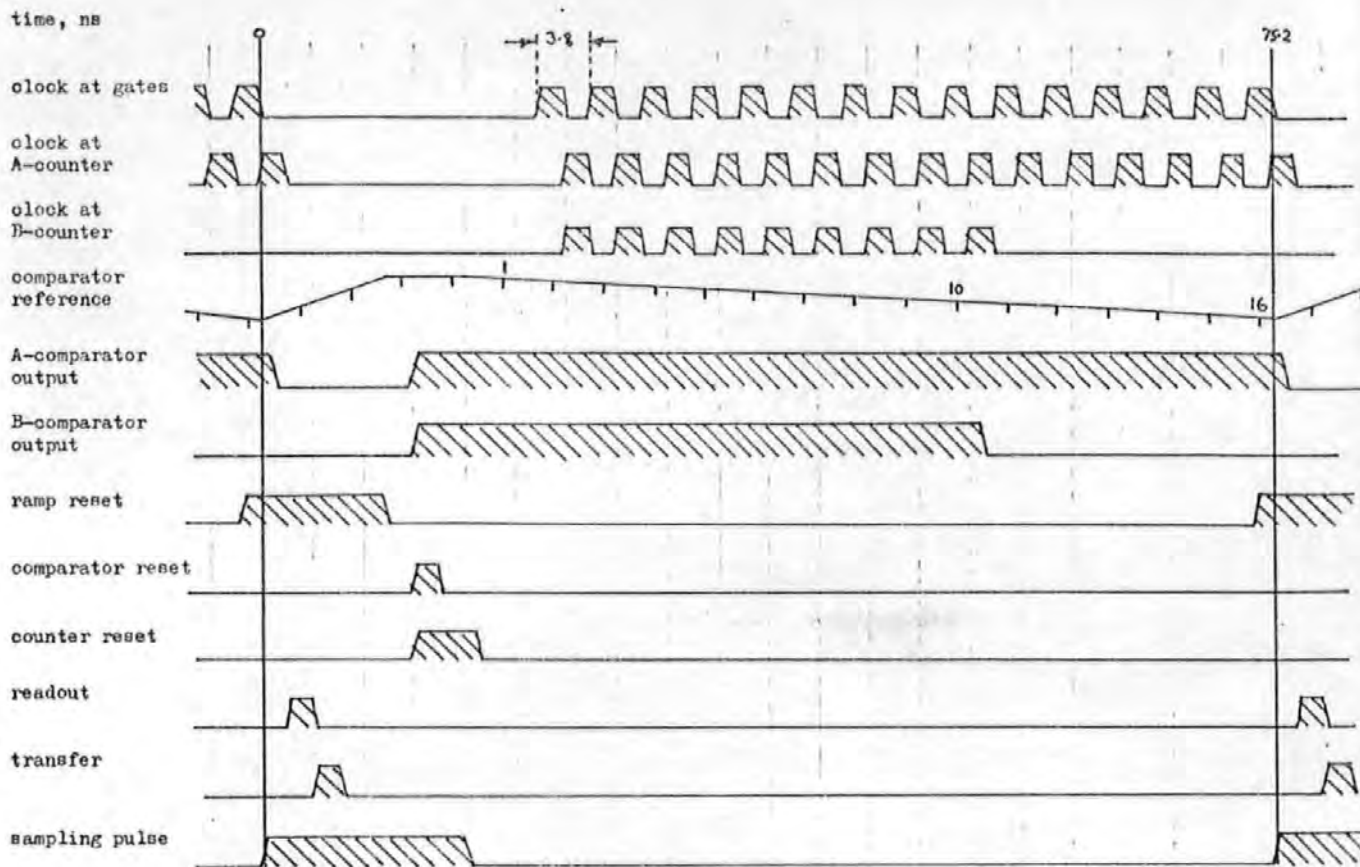


Fig.3.3 : timing system (comparator triggering corresponds to a constant comparator input of +3.08V and transmission line delays are neglected).

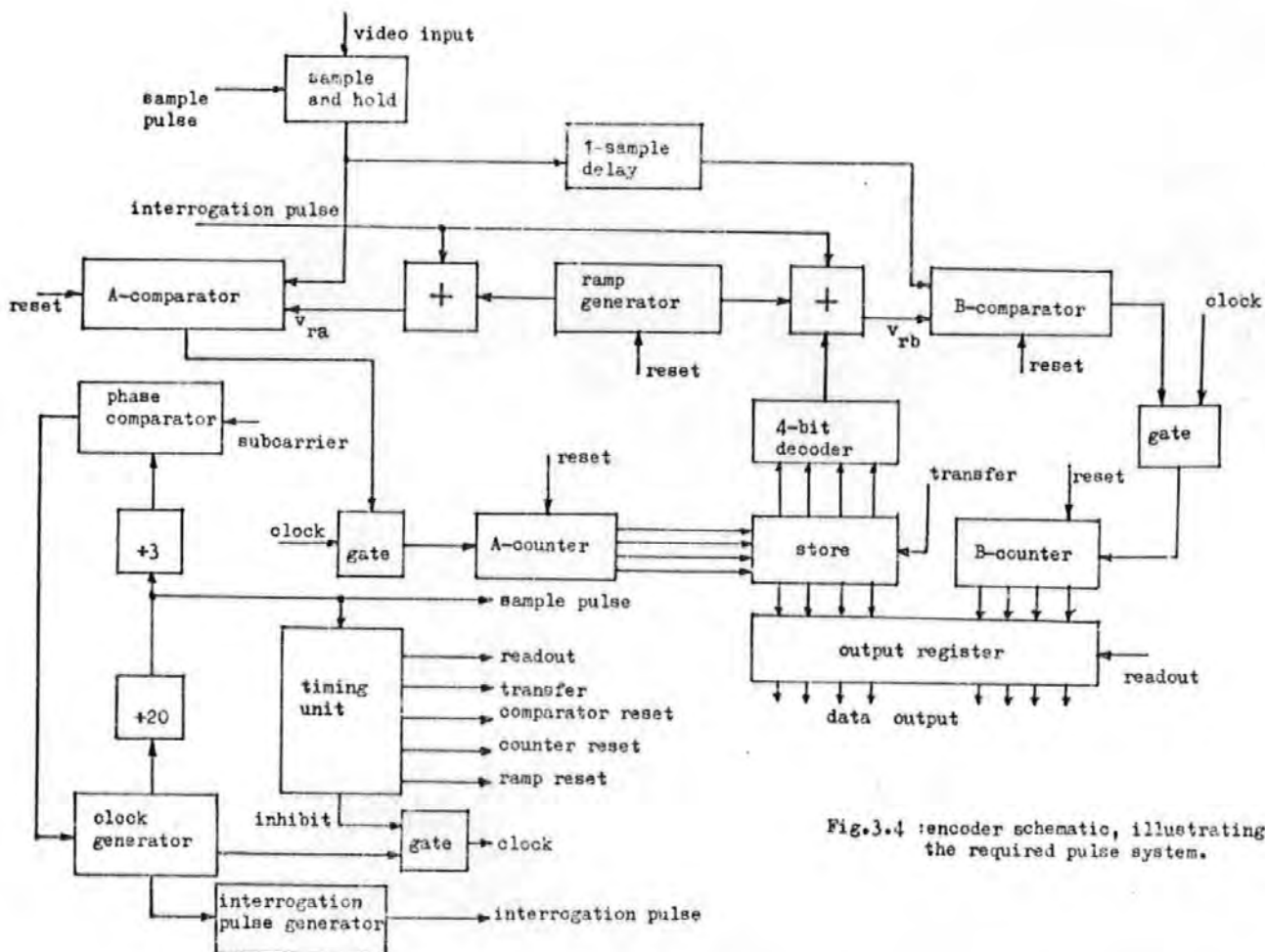


Fig.3.4 : encoder schematic, illustrating the required pulse system.

with a tunnel diode monostable or bistable. Secondly, the comparator output transition should not span more than one clock period and ideally the transition time should be significantly less than this to ensure that the corresponding gate can discriminate between two adjacent clock pulses. Thirdly, in the conventional pulse-width modulator the comparator output pulse width is continuously variable. This means that a comparator transition could occur simultaneously with the leading edge of a clock pulse at the gate and since the clock waveform is almost sinusoidal the gate operation could be ambiguous (due to noise or pulse jitter). Greater noise immunity could be achieved by further reducing the transition time although the effect of both noise and pulse jitter could be minimised if the transition always occurs between two clock pulses i.e. at a clock 0. To achieve this condition it is necessary to lock the comparator triggering to the clock and this can be done by adding interrogation pulses (at clock frequency) to each ramp reference signal. A consequence of this of course is that the comparator pulse width is quantized.

The foregoing ideas can now be formulated into a detailed timing system as shown in Figs. 3.3 and 3.4. The rise and fall times are idealised but the propagation delays through the various circuit elements are estimates from calculation or from device data e.g. it was estimated that the delay of a tunnel-diode comparator should be significantly less than one clock period and a half clock period delay is assumed in Fig. 3.3. The most critical timing occurs at readout and transfer; the state of the B-counter is sampled by the readout pulse as soon as possible after a 1111 count (the worst case) and allowing for the counter bistable delay and a small margin for timing error it follows that this pulse should occur at approximately  $t = +3\text{ns}$  w.r.t. the rising edge of the sampling pulse. The transfer pulse is advanced as far as possible in order to give maximum decoder settling time and so it occurs only several nanoseconds after the readout pulse. Considering the reset pulses, the

comparator reset must occur after the ramp has been reset to avoid premature comparator triggering and the counter reset should not be less than about 4.5ns h.a.d. to ensure correct resetting. Apart from these requirements the timing of the reset pulses is not very critical since the clock pulses are inhibited during the data transfer period. A further reason for inhibiting the clock pulses is to avoid coding error i.e. it is possible that the 16<sup>th</sup> interrogation pulse will just fail to trigger the comparator due to noise or an analog voltage error. The effect is most likely to occur for the B-comparator in which case, if a 16<sup>th</sup> clock pulse was present it could reset or partially reset the B-counter before readout was completed.

Each counter is therefore stopped, examined, and reset although as CATTERMOLE<sup>51</sup> points out this is not an essential procedure for the P.W.M. encoder. In principle the counters can be left running (so that no reset pulse is required) providing the state of each counter is rapidly sampled at the time of a comparator transition. However, this system cannot be applied if a sample and hold gate is used or if the maximum counter propagation delay is longer than one clock period (the latter criterion is violated in the proposed encoder, particularly for a 0111 to 1000 transition).

So far it has been assumed that the clock is locked to subcarrier frequency but this is not mandatory for 8-bit encoding, especially if dither is used. Any idea of how far  $f_c$  can deviate from the locked value  $f_{co}$  (266MHZ) can be obtained as follows. Assume that a ramp, generated from a constant current source  $I$  and capacitor  $C$ , is applied to a comparator and that the other comparator input is  $v_i$ . The number of gated clock pulses in a simple pulse-width modulator is then

$$N = \left(\frac{C}{I}\right) f_c v_i$$

For a fixed full scale input a specific code word must correspond to a specific  $v_1$  and  $I$  must be adjusted to compensate for variations in  $f_o$ . If the full scale input is allowed to vary then there seems no real compulsion to vary  $I$  and in either case there seems no limit on  $f_o$  variations. However, limits are imposed if we stipulate that there must always be a complete code raster or 15 counts per sample period. Assuming a fixed sample period then this period should correspond to between 14.5 and 15.5 clock periods i.e.

$$\frac{14.5}{15} < \frac{f_c}{f_{co}} < \frac{15.5}{15}$$

$$257 < f_c < 275 \quad \text{MHz}$$

In the proposed system the sample period is related to  $f_o$  by a factor 20 so the number of pulses per sample period tends to be constant and the above limits are relaxed. Allowing for the fixed inhibit pulse duration ( $5/f_{co}$ ) then the time for  $N$  clock pulses is  $20/f_o - 5/f_{co}$  and

$$\frac{14.5}{f_c} < \left( \frac{20}{f_c} - \frac{5}{f_{co}} \right) < \frac{15.5}{f_c}$$

$$239 < f_c < 293 \quad \text{MHz}$$

Summarizing, it seems probable that considerable variation in  $f_o$  can be tolerated, especially since the relative timing and duration of the readout, transfer and reset pulses is determined by the circuit and therefore should be invariant with  $f_o$ . Strictly though, the ramp amplitudes should be adjusted to compensate for variations in  $f_o$  if the encoder is to have a constant full-scale input.

### 3.2 CODING EXAMPLE

The sampled and held video at each comparator is designed to be

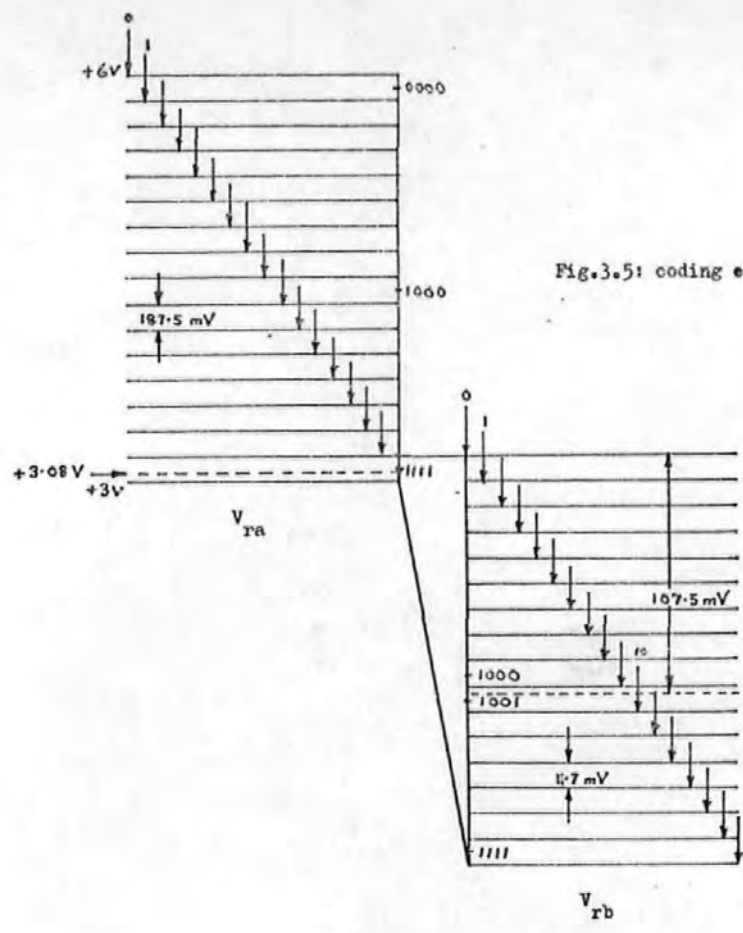


Fig.3.5: coding example

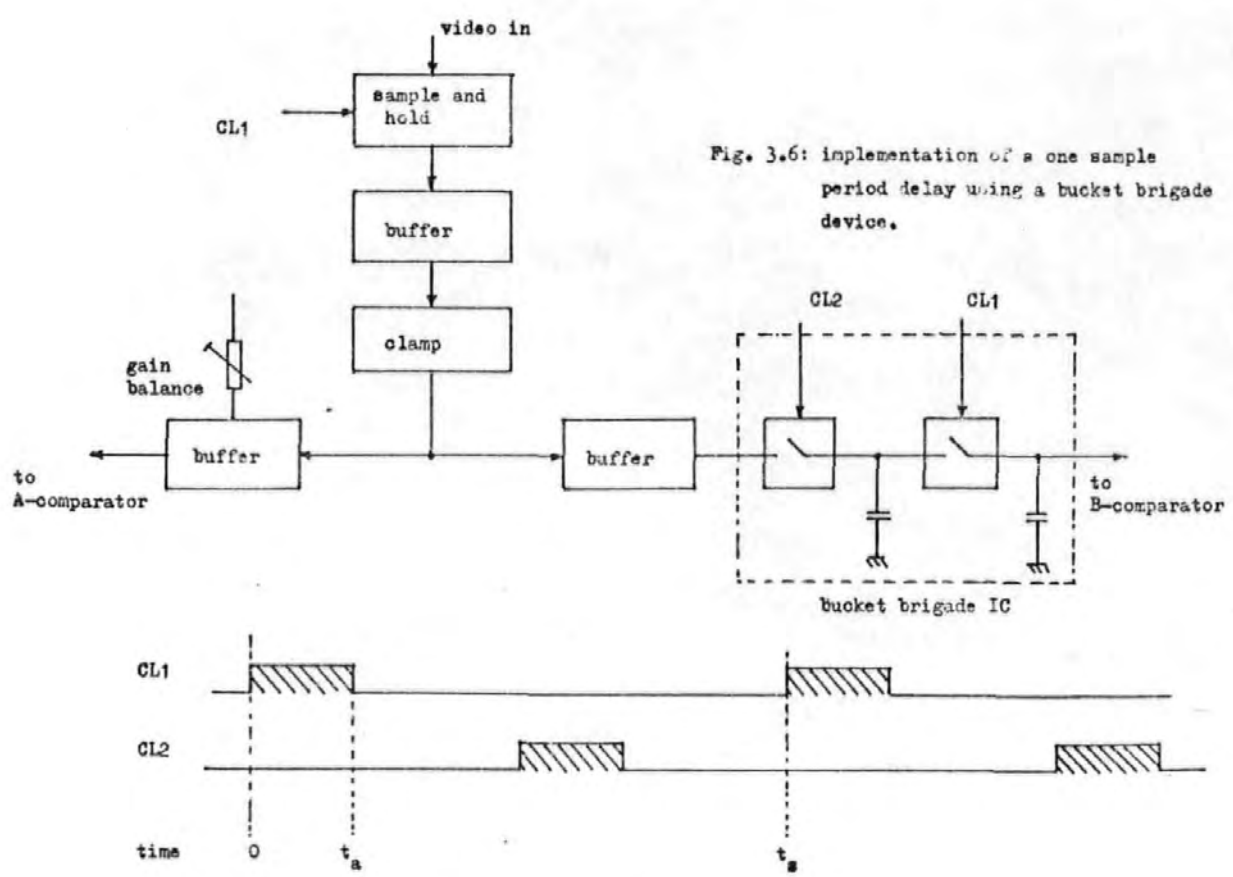


Fig. 3.6: implementation of a one sample period delay using a bucket brigade device.

Fig.3.7:8-bit PWM video encoder schematic

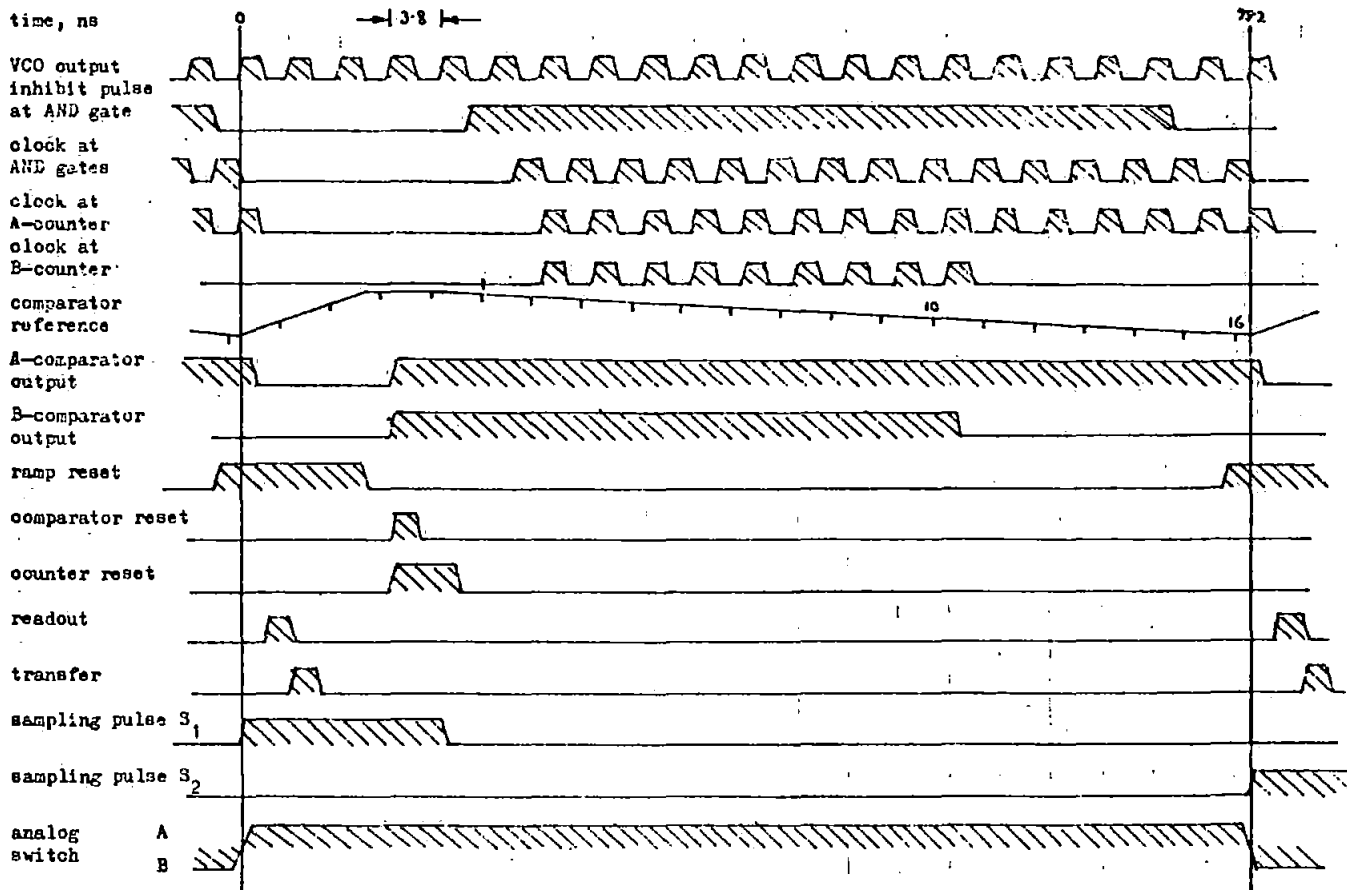
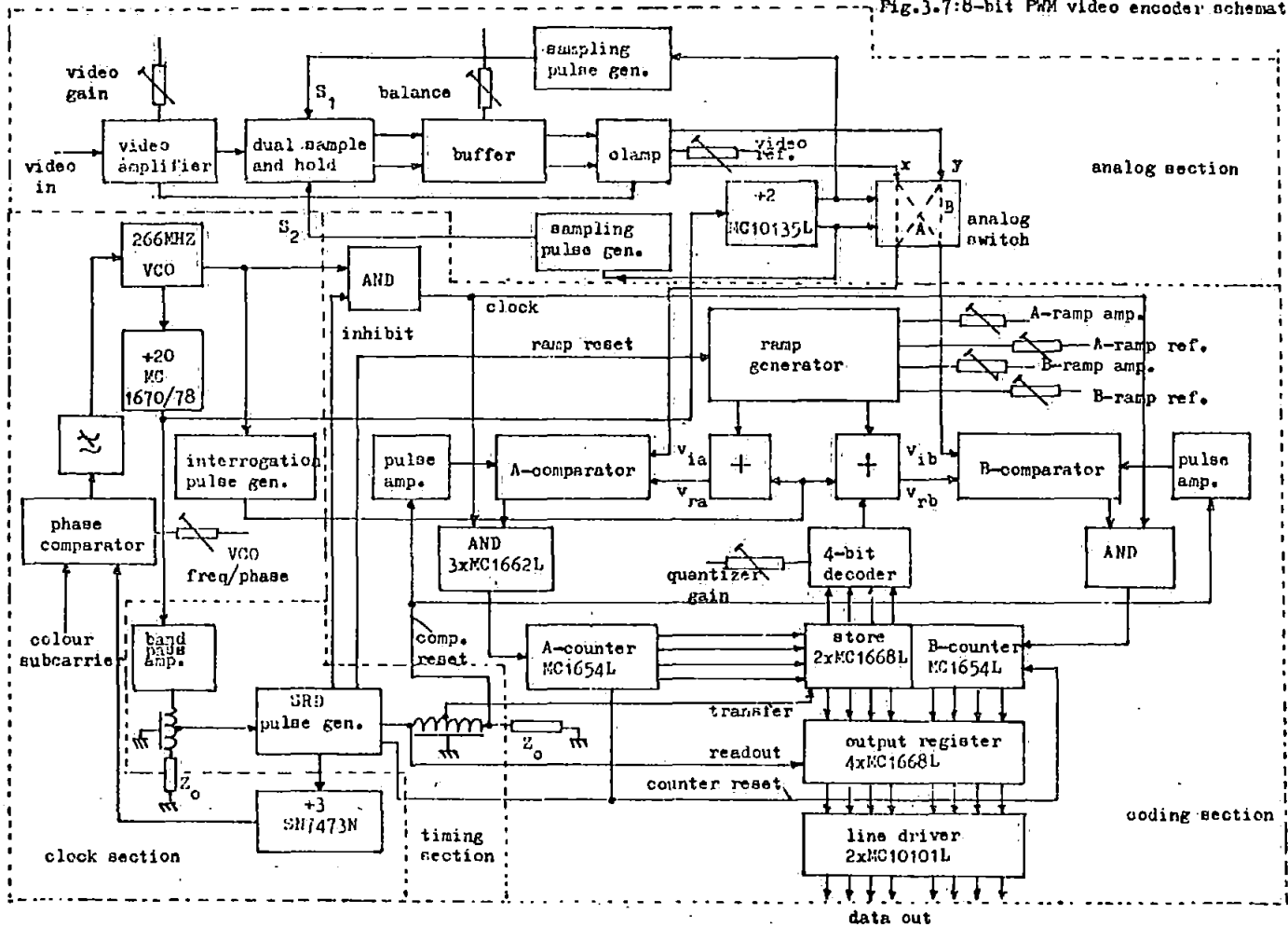


Fig.3.8: timing for encoder in fig.3.7 (comparator triggering corresponds to a constant comparator input of +3.05V and transmission line delays are neglected).

negative going (synos positive) within the range +3V to +6V and this means that the quantum interval,  $q$ , is 11.7mV (a compromise between the noise problems associated with a small quantum interval and the power dissipation problems associated with a large quantum interval). It follows that a 3V ramp is required for coding the 4 MSB's and a 3/16V ramp is required for the LSB's and Fig. 3.5 shows the reference levels defined by linearly adding the interrogation pulses to each ramp. To illustrate the coding principle we assume that bright picture elements are being sampled, each corresponding to +3.08V at the comparator inputs. Referring to Fig. 3.3 it will be seen that the A-comparator does not trigger until the 16<sup>th</sup> interrogation pulse so that all 15 clock pulses are counted. A few nanoseconds later the count 1111 is stored and the contents of the store are decoded to provide a reference level  $V_{rb}$  for coding the 4 LSB's. For an  $n$ -bit, 2-step encoder the generalised form of  $V_{rb}$  is

$$V_{rb}(x) = V_0 - V_{fs} \left[ \sum_{i=1}^{n/2} \left( \frac{a_i}{2^i} \right) - \frac{x}{2^n} \right] \quad (3.3)$$

where  $n$  is an even integer,  $V_0$  represents an adjustable dc level and  $V_{fs}$  represents the quantizing range. Coefficients  $a_i$  are either 1 or 0 depending upon the 4 MSB's and  $x$  is an integer in the range 0 to 16. In the example, the +3.08V sample gives the full-scale decoder output such that  $V_{rb}(0)$  is +3.1875V as shown in Fig. 3.5. This leaves 107.5mV to be coded, corresponding to 9.18q or 1001, so the B-comparator triggers on the 10<sup>th</sup> interrogation pulse and only 9 clock pulses are gated to the B-counter. The samples are finally readout as 11111001.

### 3.3 CIRCUIT DESIGN ASPECTS

A schematic of the prototype encoding system is shown in Fig. 3.7 and for discussion purposes it is convenient to divide it into analog, clock,



timing and coding sections.

### 3.3.0 ANALOG SECTION

This section must incorporate a linear amplifier, a sample and hold circuit, a line frequency clamp and a 1 sample period delay and preferably all these functions should be such that they could be put into IC form. In this respect the delay would seem best realized by some form of electronic analog delay such as a bucket brigade or charge coupled device as illustrated in Fig. 3.6 but unfortunately, at the time of design these devices were limited by poor charge transfer efficiency for clock frequencies above a few MHz<sup>80</sup> and so some other delay mechanism had to be sought. A high  $Z_0$  delay cable could be used (typically the delay is 140ns/m for  $Z_0 = 950\Omega$ ) but this is bulky and also has the disadvantages that cable attenuation tends to increase with  $Z_0$  and if the sampling frequency were changed it would be necessary to change the delay cable. An alternative approach to the problem is illustrated in Fig. 3.7 and clearly this has the possibility of being integrated. The delay is achieved by using a dual sample and hold gate and a fast analog switch and by making a small modification to the timing system as shown in Fig. 3.8. Essentially, the charge on one sample gate is held over for a second sample period so that it can be switched rapidly to the B-comparator for the encoding of the 4 LSB's. The total hold time is therefore  $2t_s - t_a$ .

One of the fundamental problems in the encoding of wideband signals is that the encoder output code,  $D(nt_s)$  corresponding to a sample at  $t = nt_s$  could differ considerably from the code corresponding to the actual input voltage sample  $v_i(nt_s)$ . Mathematically

$$D(nt_s) \longleftrightarrow v_i(nt_s) + e$$

where 'e' is an error voltage. Sample and hold errors are one of the main reasons

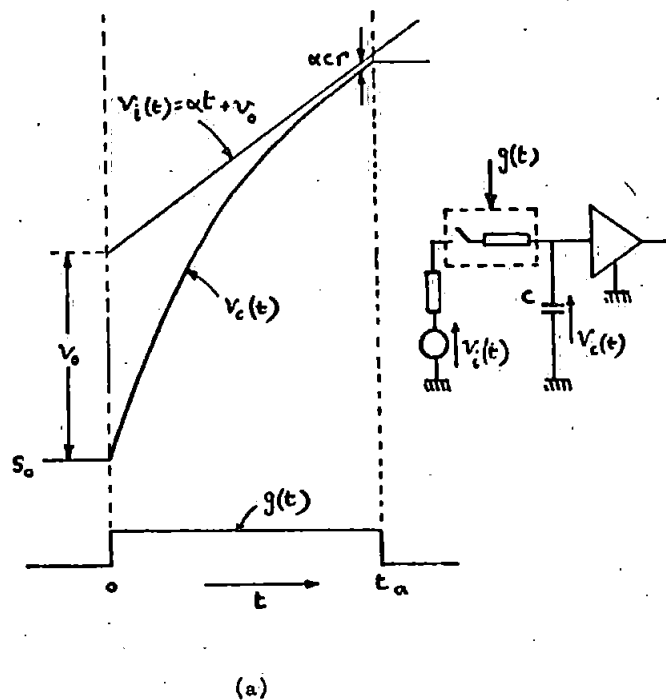


Fig. 3.9 :sampling waveforms

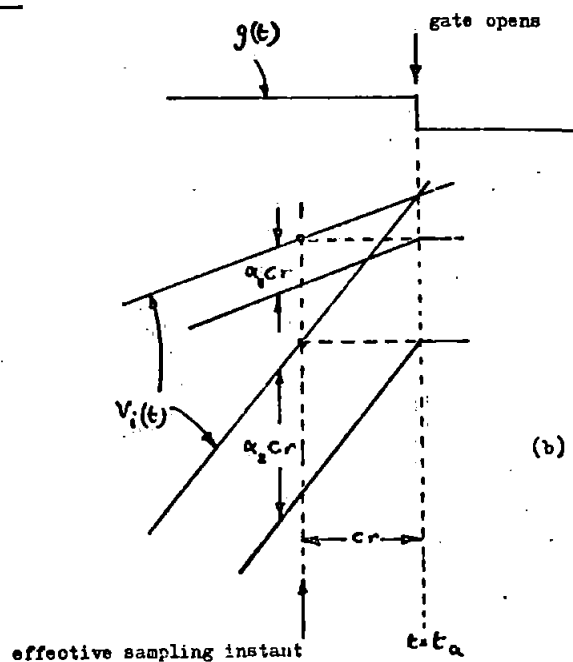
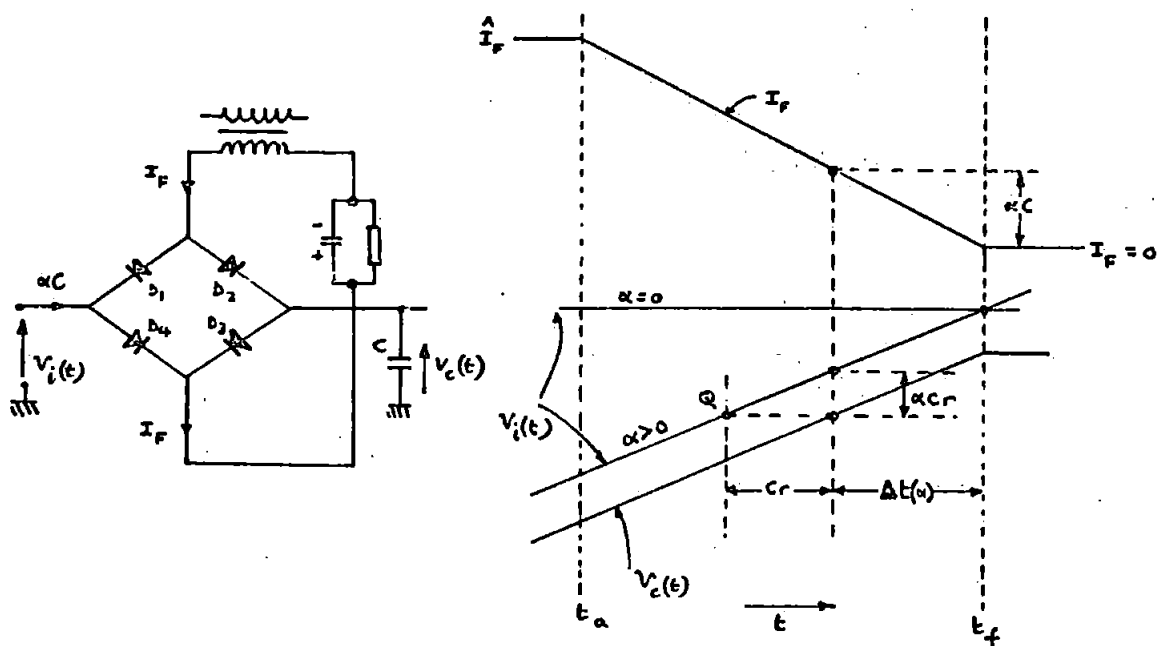


Fig. 3.10: illustrating uncertainty in the sampling instant



causing this discrepancy and some design aspects of this problem are considered below.

Each sample gate is conventional; it uses a Shottky diode matched quad driven from a balanced pulse transformer in order to minimise charge transfer from the drive pulse to the hold capacitor  $C$ , and a MOSFET buffer amplifier is used to minimise charge leakage during the hold period. The major leakage will then be due to the sampling gate leakage current  $I_g$  (typically 100nA) and if the capacitor voltage is to be held constant to within  $q/10$  over the hold period then

$$C > 10 q I_g (2t_s - t_a)$$

Taking  $q = 11.7\text{mV}$  gives  $C > 11.5\text{pF}$  approximately. An upper bound to  $C$  can be obtained by considering the sampling waveforms in Fig. 3.9(a). Here the following simplifying assumptions have been made:

1. the analog input  $v_i(t)$  increases linearly with time over the acquisition period.
2. the effects of any parasitic series inductance and any leakage paths are negligible.
3. the gate switching is ideal i.e. the gate turns on and off instantaneously.

It follows that

$$v_c(t) = v_i(t) - (v_0 - \alpha cr) e^{-t/cr} - \alpha cr + s_0 \quad (0 \leq t \leq t_a) \quad (3.4)$$

where  $s_0$  is the previous sample amplitude,  $r$  is the total series resistance, and  $\alpha$  is the slew-rate of  $v_i(t)$  for  $0 \leq t \leq t_a$ . It is reasonable to require that

$$(v_0 - \alpha cr) e^{-t/cr} < q/2 \quad (\text{the maximum quantizing error})$$

$$\therefore C < \frac{t_a}{6.9r} \quad \text{approximately}$$

Using typical values ( $t_a = 15\text{ns}$ ,  $r = 20\Omega$ ) gives  $C < 109\text{pF}$ . It is interesting to note that the steady-state error  $\alpha cr$  is not important since it corresponds to a

fixed perturbation  $c_r$  in the sampling instant as shown in Fig. 3.9(b). What is detrimental is a random perturbation in the sample instant ( $t = t_a$ ) due to sample pulse jitter or due to a finite slew rate in the gate drive current and the total uncertainty in the sample instant is termed the aperture time. We will assume pulse jitter to be negligible and calculate the required slew rate for satisfactory broadcast performance. Referring to Fig. 3.10, the following assumptions have been made:

1. the analog input is linear over the small time interval considered (a few nanoseconds) and the gate drive current decreases linearly with time.
2. the circuit has reached steady state such that the charging current is  $\alpha c$  at  $t = t_a$ .
3. the diodes have an ideal forward characteristic and turn off immediately the forward current drops to zero (i.e. negligible charge storage).

For a constant input signal ( $\alpha = 0$ ) the diodes cut-off at  $t = t_f$  but if  $\alpha$  is finite the effective sampling point is  $Q$  since diodes  $D_1$  and  $D_3$  cut off when  $I_F = \alpha C$  (the gate is assumed to open at this point although this is only strictly true if it is driven from a high impedance source). The time uncertainty or aperture time is

$$\Delta t(\alpha) = \alpha c (t_f - t_a) / \hat{I}_F \quad (3.5)$$

and the aperture error (i.e. the voltage error arising from the finite rate of change of both  $I_F$  and the analog input) is

$$e_a = \alpha^2 c (t_f - t_a) / \hat{I}_F \quad (3.6)$$

Assuming  $e_a$  has a uniform p.d.f. in the range 0 to  $\hat{e}_a$

$$\begin{aligned}
 \overline{e_a^2} &= \int_0^{\hat{e}_a} p(e_a) e_a^2 d(e_a) \\
 &= \hat{e}_a^2/3 \\
 &= \frac{1}{3} \left[ \frac{\hat{\alpha}^2 C}{\hat{I}_F} (t_f - t_a) \right]^2
 \end{aligned}$$

A reasonable criterion is that the r.m.s. aperture error should be less than the r.m.s. quantizing error i.e.

$$\frac{\hat{\alpha}^2 C (t_f - t_a)}{\sqrt{3} \hat{I}_F} < \frac{V_{FS}}{2^n \sqrt{12}}$$

Taking  $\hat{\alpha} = V_{FS} \pi f_m$  where  $f_m$  is the maximum video frequency gives a lower bound for the current slew-rate  $S$

$$S > 2^{n+1} V_{FS} (\pi f_m)^2 C \quad (3.7)$$

and letting  $V_{FS} = 3V$ ,  $C = 50pF$ ,  $f_m = 5.5MHz$  and  $n = 8$  gives a minimum slew-rate of  $2.3 \cdot 10^7 A/s$ . If, for example,  $t_f - t_a = 2ns$  then  $\hat{I}_F > 46mA$  and the corresponding aperture time is 225ps (eqn. (3.5)). This shows that a relatively high drive current is required to minimise aperture error and a similar conclusion has been reached by PEARCE and MAYS<sup>59</sup>.

Each sampling pulse generator (Fig. 3.7) was designed to generate current pulses of this order and each pulse is of 15ns duration with rise and fall times of a few nanoseconds. Also, the two sampling pulses must occur alternately at intervals of one sample period and any error in the relative timing of these pulses must be of the order of 1ns, or less (see chapter 6). These requirements can be met by the S.R.D. pulse shaping network shown in

Fig. 3.11. This type of network is analysed in section 3.3.2 for the generation of the inhibit pulse and a qualitative description suffices here. The falling edge of the square wave at  $T_{82}$  collector depletes  $D_1$  of stored charge and  $D_1$

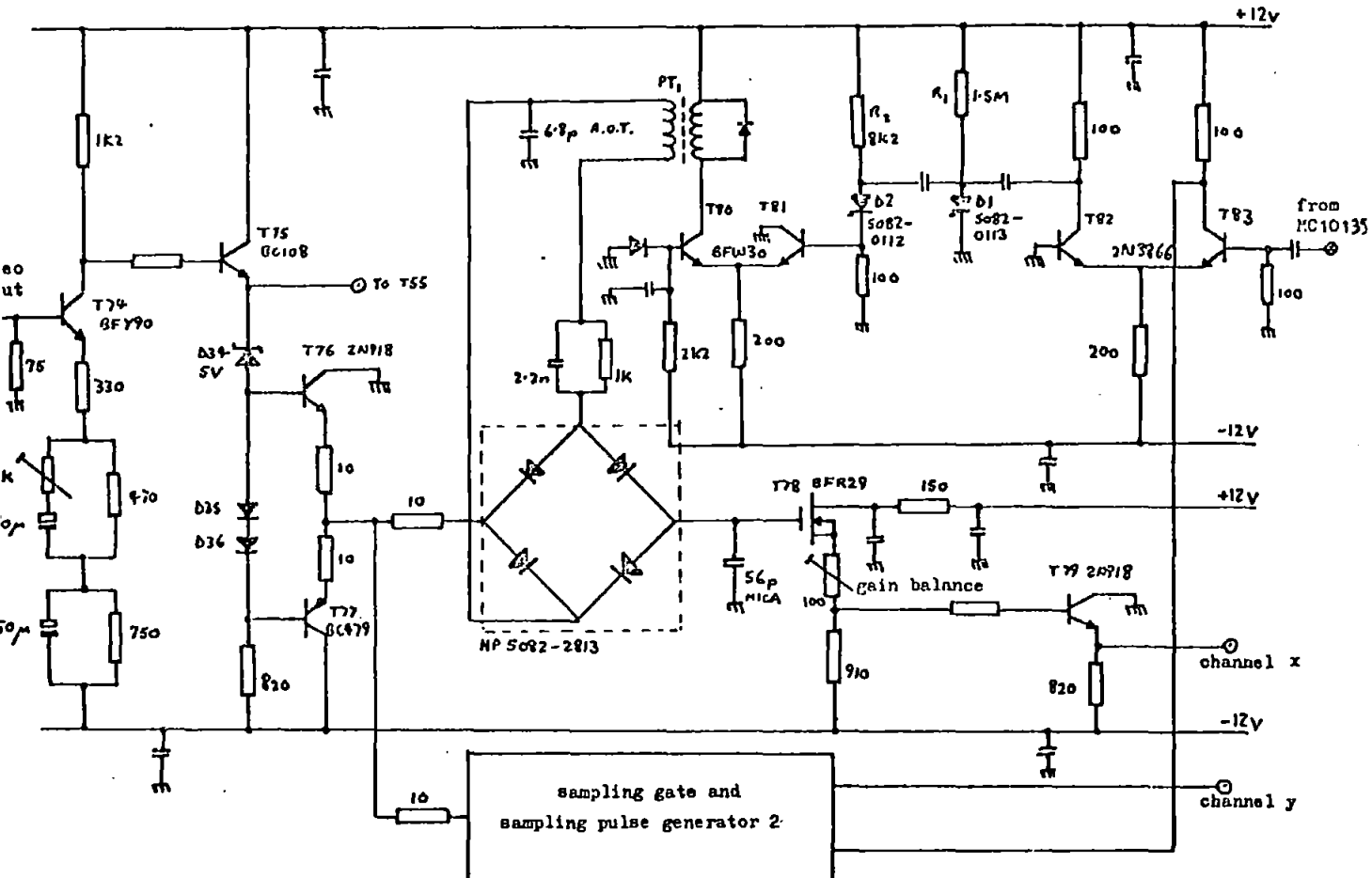


Fig. 3.11: video amplifier and sampling circuits

'steps' off giving a rapid negative transition at  $T_{81}$  base. After a delay determined by the stored charge in  $D_2$ , a positive transition occurs as  $D_2$  'steps' off and  $T_{81}$  base potential rises to approximately 0V. Both diodes are turned on again by the rising edge of the square wave at  $T_{82}$  collector. The timing and duration of the negative pulse at  $T_{81}$  base is therefore determined by resistors  $R_1$ ,  $R_2$  respectively. Fig. 3.12 shows the waveform at  $T_{81}$  base; the pulse rise and fall times are about 600ps and the positive 0.5V step (graticule centre) is due to the rising edge of the square wave at  $T_{82}$

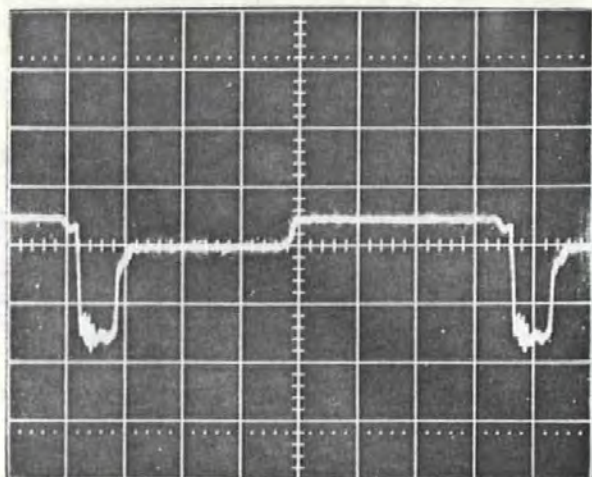


Fig. 3.12: sampling waveform at T81 base. Scales: 20ns/div, 1V/div

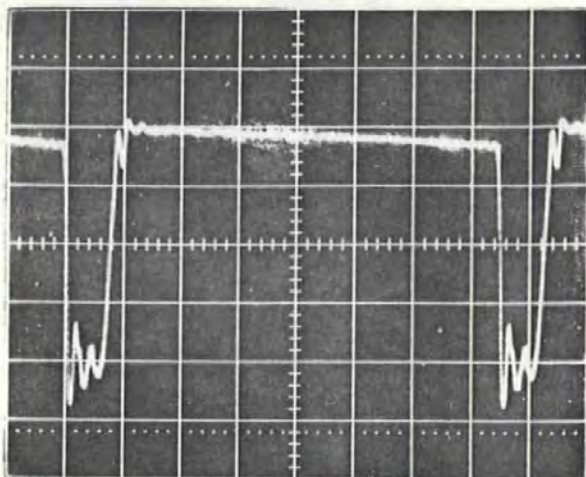
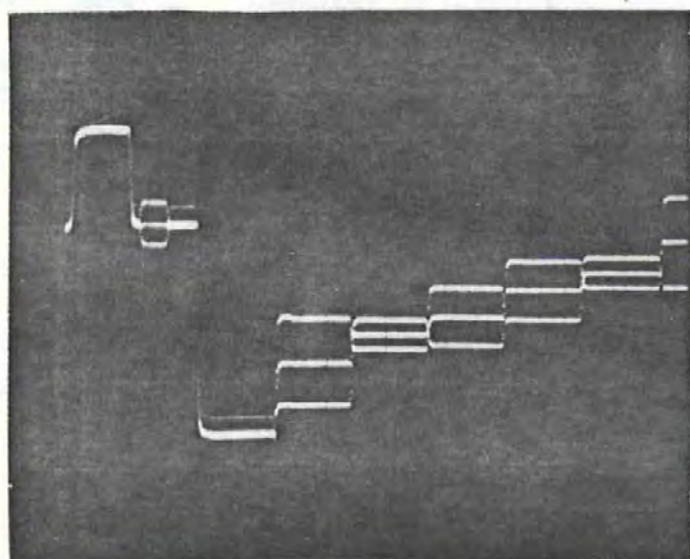
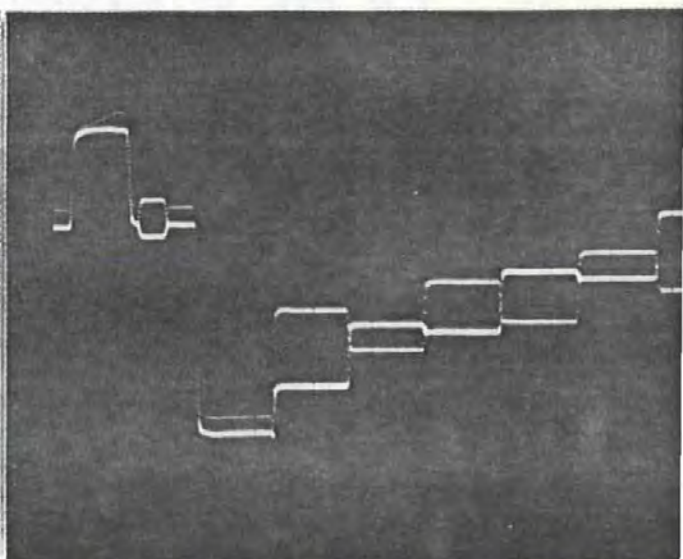


Fig. 3.13: sampling pulses measured across 100Ω across PT1 secondary. Scales 20ns/div, 1V/div



0° sampling phase



90° sampling phase



Fig. 3.14: sampled and held EBU colour bars (U-chrominance components only)



Fig. 3.15: clamp and analog switch

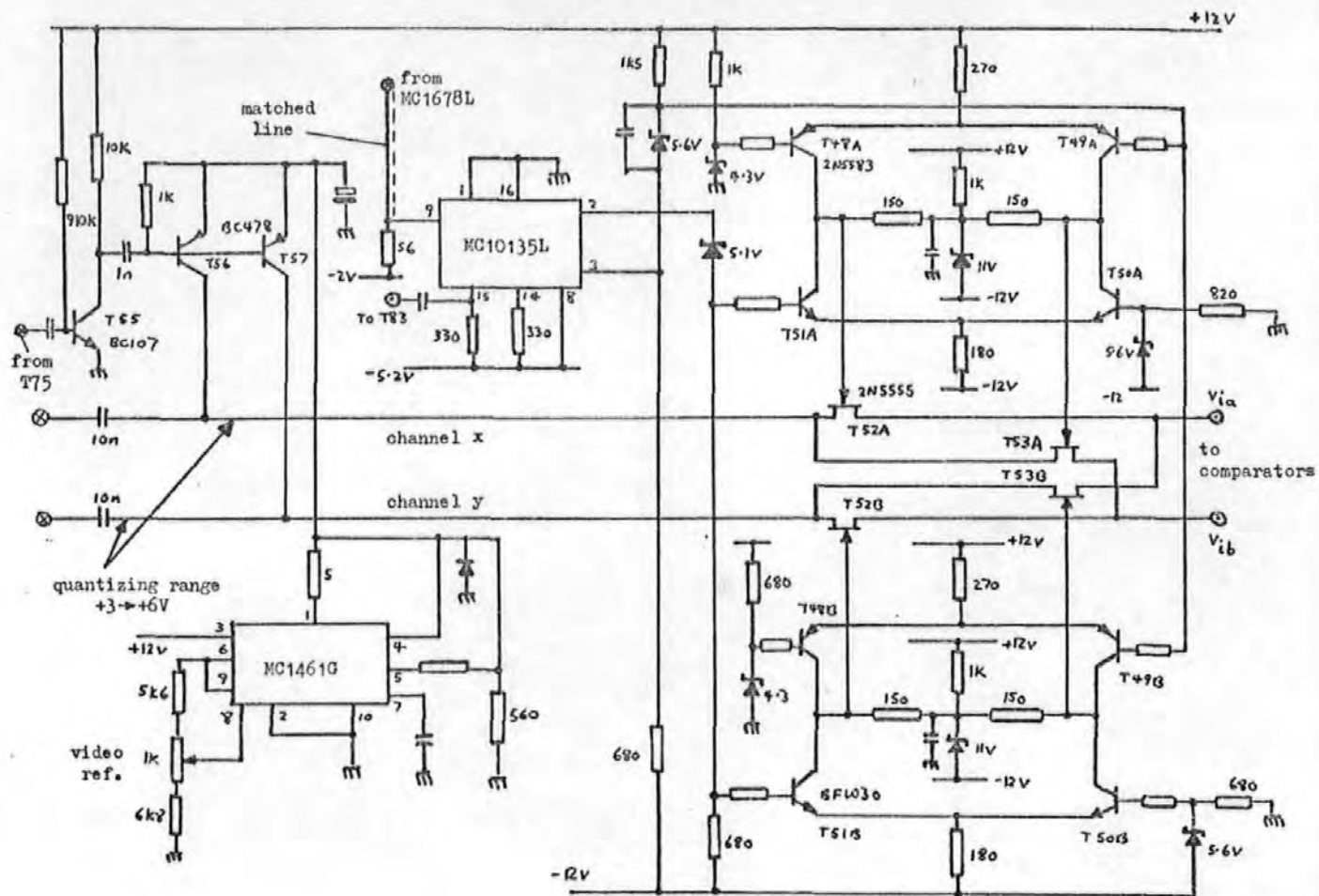
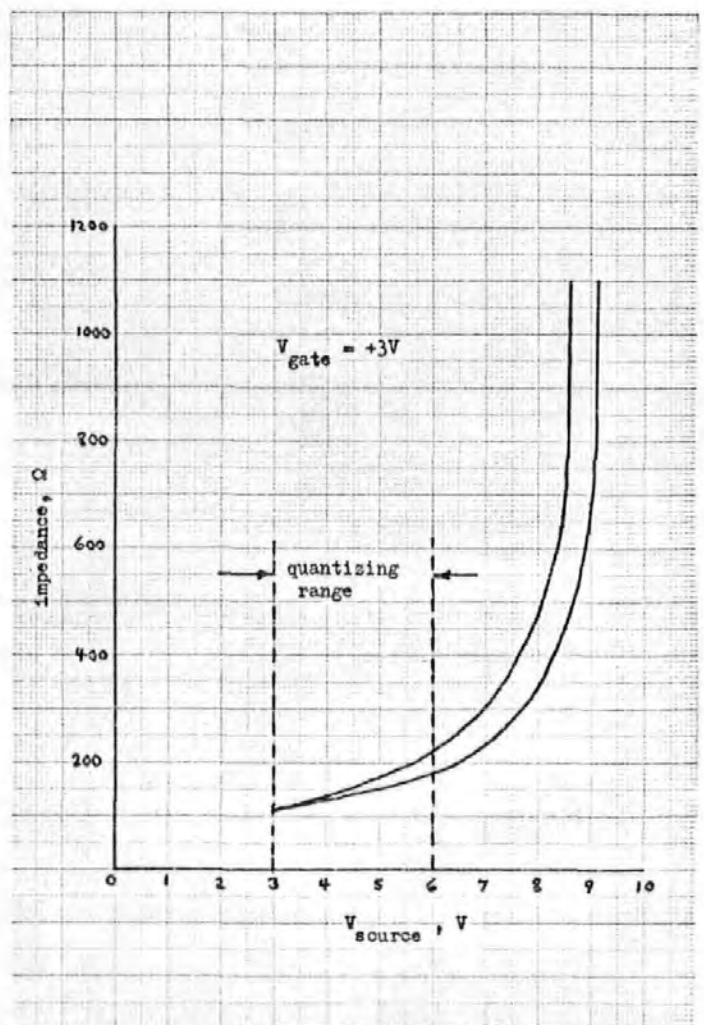


Fig. 3.16: measured low frequency drain-source impedance for two n-channel depletion mode JFET devices.



collector. The corresponding sampling pulses at half sampling frequency and measured across a  $100\Omega$  load at PT1 secondary are shown in Fig. 3.13.

The performance of the sample and hold circuit is illustrated in Fig. 3.14; this shows a sampled and held EBU colour bar waveform at T79 emitter. To simplify the display a fixed phase chrominance and burst signal is shown, that is, the V-chrominance component is inhibited at the bar-generator to avoid displaying up to 6 horizontal lines per colour bar. Sampling is locked to subcarrier and under these conditions the oscillator frequency control (fig. 3.7) enables the sampling phase to be varied as illustrated in the figure. Detailed examination of these waveforms revealed a 20mV tilt on some parts of the held chrominance signal. This was attributed to unbalance in the sampling pulse drive since the tilt could be more than halved by inserting a small balancing capacitor in the drive circuit (Fig. 3.11).

Referring to Fig. 3.15, the sampled and held video is clamped such that sync level corresponds to the top of the quantizing range (+6V) and the clamp capacitor is chosen as 10nF so that for  $< 2\%$  line tilt the leakage current must be  $< 10\mu\text{A}$ . The clamped signal is then switched and switching must occur between the 16<sup>th</sup> and 1<sup>st</sup> interrogation pulses - a period of only 18ns and during which time all switching transients should have decayed to within one quantum amplitude. An integrated switch meeting this specification was not available so that a fast JFET switch was designed. This type of switch was chosen in preference to a bipolar switch since it is easier to isolate the switch control signal from the analog signal and also because a FET has zero offset voltage. The switching speed depends upon the charge/discharge rate of the JFET gate capacitances so that a device having low input, output and reverse transfer capacitance was selected. The switching time is also reduced by driving the gate directly from a relatively low source impedance (in contrast to resistor or capacitor gate drive<sup>37</sup>) although this does have the disadvantage

in that the switch impedance varies over the quantizing range as shown in Fig. 3.16. However, since the switch current has to be  $< 10\mu\text{A}$  the effect of the switch impedance variation is  $< q/10$  and direct gate drive is acceptable. Fig. 3.16 also shows that the gate drive swing must be  $> 7\text{V}$  to ensure FET cut-off and this means that the transistor gate drive circuits have to switch currents as high as  $30\text{mA}$ . These current switches are emitter coupled for optimum switching speed although the low logic swing ( $0.8\text{V}$ ) made it necessary to carefully select the zener diodes and in general the circuit was critical to set up.

The dynamic performance of the switch is illustrated in Fig. 3.17. This is quite a severe test since it presupposes that time adjacent samples are different by  $2/3$  of the quantizing range whereas for most of the time, even for chrominance signals, the level difference will be considerably less than this and the switching time is correspondingly reduced.

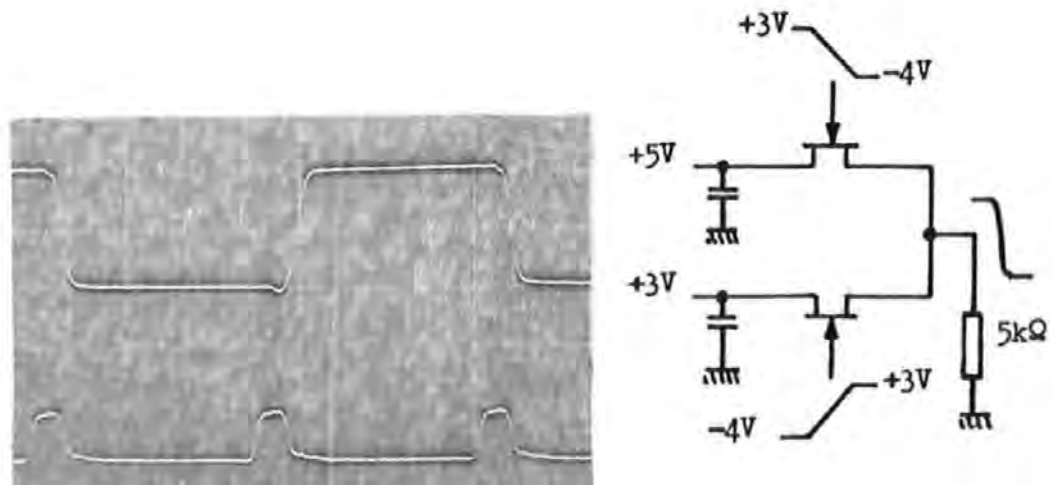


Fig. 3.17: Analog switch dynamic performance: upper trace, switching between  $+3\text{V}$  and  $+5\text{V}$  levels, lower trace, clock to bistable driver.  
scales:  $1\text{V/div}$ ,  $20\text{ns/div}$

### 3.3.1 CLOCK SECTION

The VCO should deliver 266MHZ clock pulses at the standard ECL levels and it should be electronically tunable for use in a phase lock loop. Amongst the possibilities explored was a h.f. emitter-coupled oscillator (MC1648) and a GaAs tunnel-diode oscillator. The I.C. was designed for just such an application but upon test it failed to work above 220MHZ. The tunnel-diode oscillator has the advantage of simplicity, but it is relatively difficult to tune it electronically. The only possibility of tuning it with a 'varicap' is to vary the rise and fall times by varying the effective diode capacitance  $C_j$ , e.g.

$$t_r \approx C_j (V_F - V_P) / I_P$$

$$t_f \approx C_j (V_V - V_P) / I_V$$

where  $V_F$  is the forward voltage corresponding to  $I_P$  and  $V_V$  is the valley voltage corresponding to  $I_V$ . Clearly this is not very satisfactory since the time spent in the relatively constant voltage regions is independent of  $C_j$ . A grounded-base Colpitts oscillator was finally chosen since it is relatively easy to tune, and it has a larger output swing. Referring to Fig. 3.18, the oscillator switches an emitter coupled pair to give the correct logic swing and the correct logic levels to the frequency divider. The D-flipflop has a maximum toggle frequency of 350MHZ and the  $\div 10$  counter is a high-speed 4-bit counter with internal feedback to give a bi-quinary function; the output of this counter is the nominal 13.3MHZ sampling frequency.

Fig. 3.18 also shows the interrogation impulse generator; T17 drives a S.R.D. impulse generator which is used to switch current mode switches T41, T42 and T43, T44. A useful estimate of the duration of the negative impulse across the load  $R_L$  is

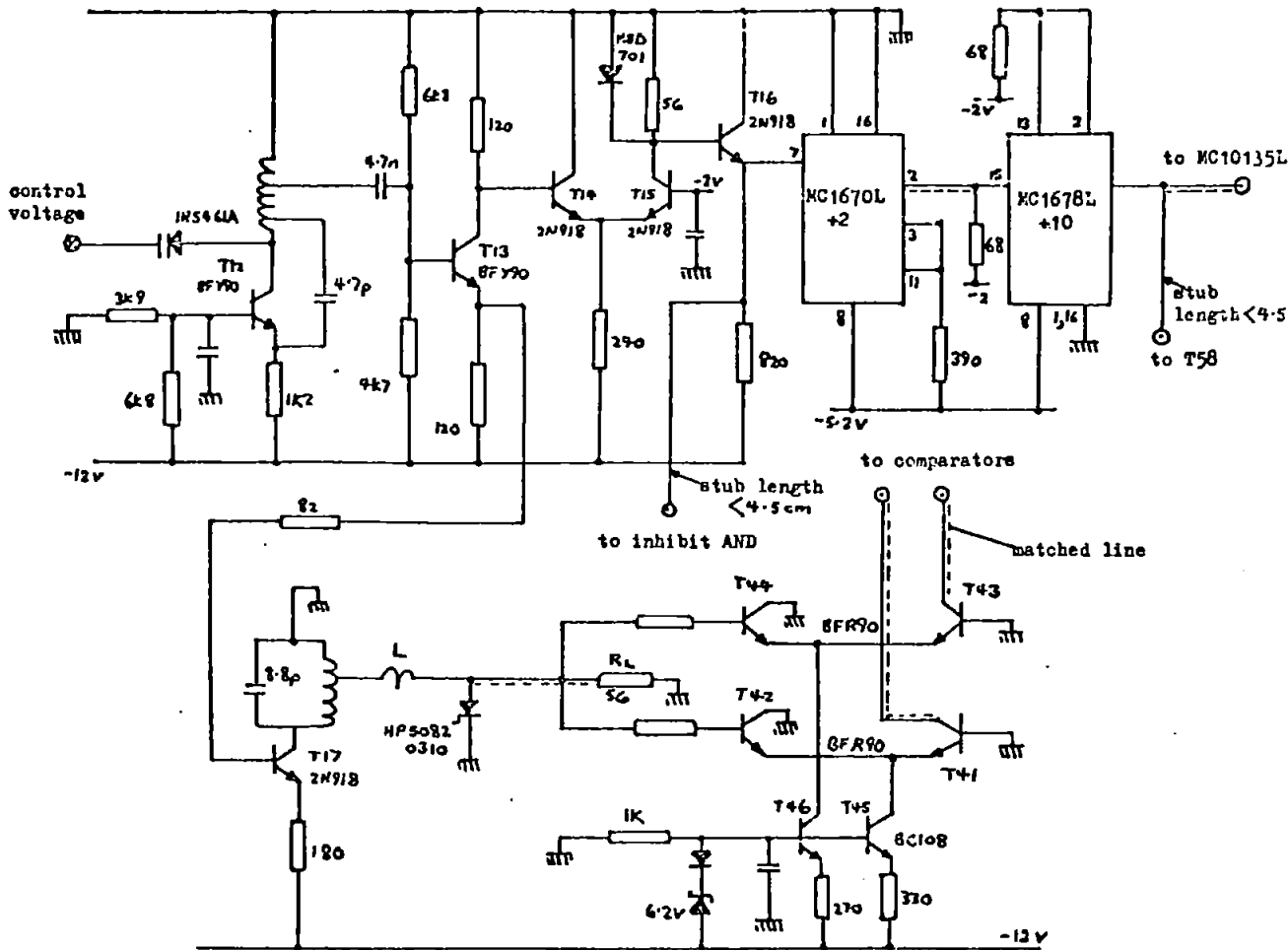


Fig. 3.18: VCO, impulse generator and frequency divider

$$t_p = \pi \left( \frac{L C_{VR}}{1 - h^2} \right)^{1/2}$$

where

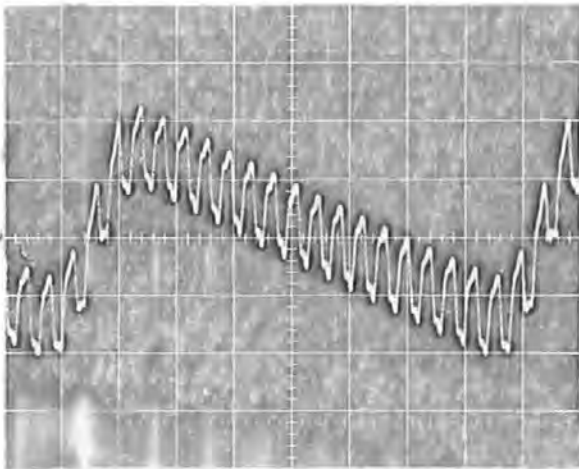
$$h = \frac{1}{2R_L} \left( \frac{L}{C_{VR}} \right)^{1/2}$$

where  $C_{VR}$  is the diode depletion capacitance and  $h$  is the damping factor.  $C_{VR}$  is typically 3pF and the impulse duration should be of the order of ns so that  $L \approx 18nH$ . The rise time  $t_r$  of the interrogation pulses at each comparator is a function of the collector time constant  $R_L C_L$  across which the pulses are developed but it also depends upon the impulse rise-time  $t_{r1}$ , the transistor parameters and the switched current,  $I_0$ . The latter factors are seldom considered but they have a significant bearing upon the rise time in

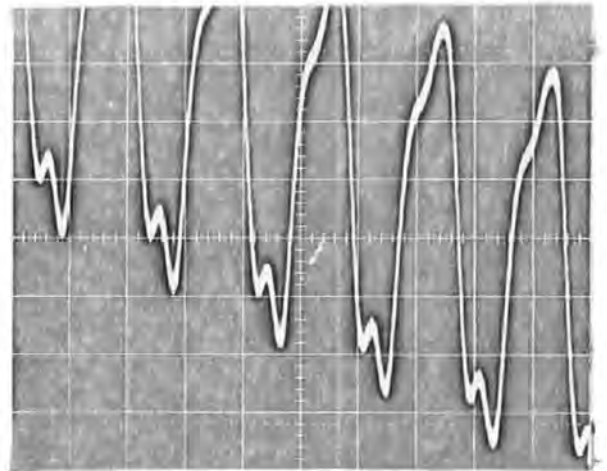
this application. An approximate expression combining all these factors is derived in appendix 1 as

$$t_r = \left[ t_{ri}^2 + \left( \frac{1.6 r I_o}{\omega_T v_i} \right)^2 + (2.2 C_L R_L)^2 \right]^{1/2} \quad (3.8)$$

The time constant  $C_L R_L$  is fixed from current drive limitations and by inevitable parasitics but the switching transistors T41 — T44 can be chosen such that the second term is relatively small. For example, typical values are  $t_{ri} = 300\text{ps}$ ,  $R_L = 100\Omega$ ,  $C_L = 2\text{pF}$ ,  $v_i = 0.2\text{V}$ ,  $I_o = 20\text{mA}$  and  $r = 50\Omega$ , and taking  $f_T = 500\text{MHz}$  gives  $t_r = 2.6\text{ns}$ . In this case the active devices are severely limiting  $t_r$  and very significant improvement is obtained by using u.h.f. devices having  $f_T \approx 5\text{GHz}$ . For the above values  $t_r$  now reduces to  $590\text{ps}$  and this is typical of the measured rise-times as shown in Fig. 3.19.



1V/div, 10ns/div



0.2V/div, 2ns/div

Fig. 3.19: Comparator reference  $V_{ra}$  (Fig. 3.31) showing interrogation pulses on A-ramp.

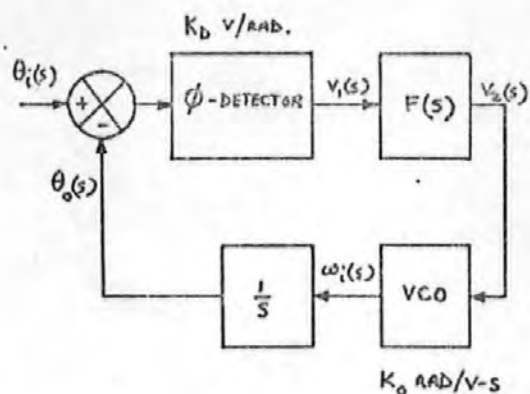


Fig. 3.20: linear model of the phase lock loop under locked conditions.

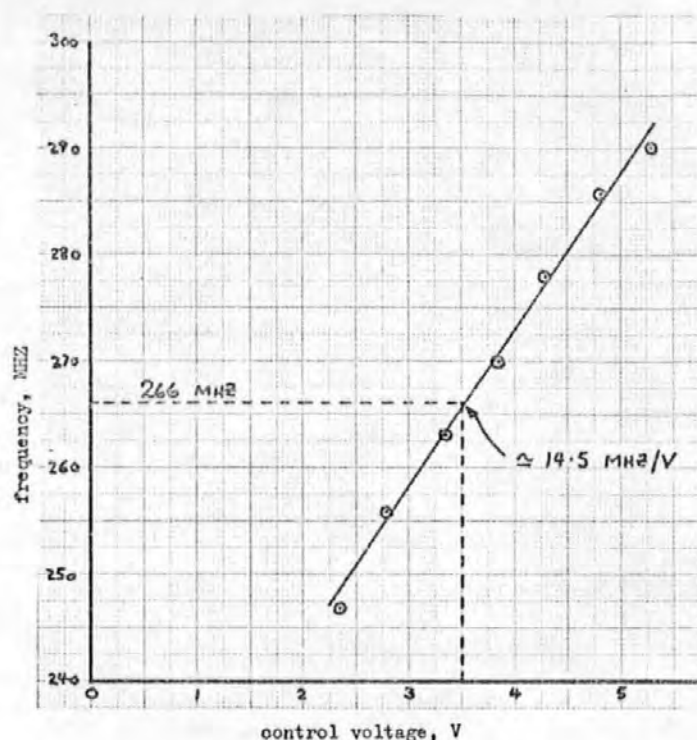


Fig. 3.21: VCO characteristic

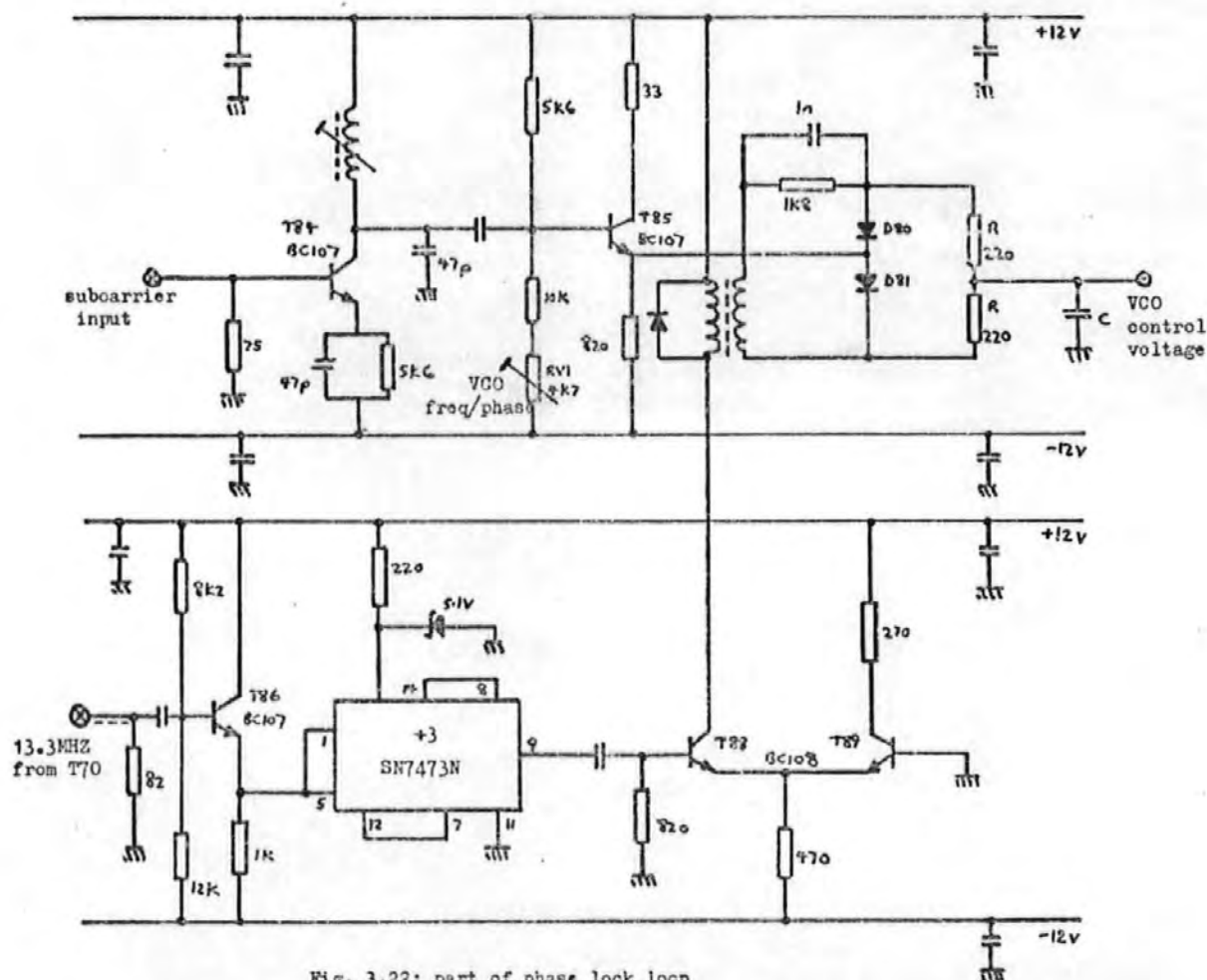


Fig. 3.22: part of phase lock loop



The phase lock loop can be analysed from Fig. 3.20. The model is considered linear in the sense that  $\theta_i - \theta_o$  is small and therefore the phase detector output can be assumed to be proportional to  $\theta_i - \theta_o$ . The loop input signal is colour subcarrier and the VCO is assumed to free-run near to subcarrier frequency. The actual VCO (the Colpitts oscillator) operates at the 60<sup>th</sup> harmonic of subcarrier frequency and this must be taken into account when calculating  $K_o$ . The closed loop transfer function is

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_D F(s)}{s + K_o K_D F(s)}$$

The filter  $F(s)$  affects the dynamic response of the loop, that is, loop stability, transient response to a step input, capture range, tracking and noise immunity. Of these parameters only loop stability and perhaps noise immunity are important in this application and a simple lag filter suffices. i.e.

$$F(s) = (1 + s\tau)^{-1}$$

giving 
$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where 
$$\omega_n = \left(\frac{K_o K_D}{\tau}\right)^{1/2}, \quad \zeta = \frac{\omega_n}{2K_o K_D}$$

The poles of  $H(s)$  show that the loop is unconditionally stable as required.

At this point it is helpful to find the loop gain  $K_o K_D$ . The oscillator frequency as a function of the control voltage is shown in Fig. 3.21; the oscillator free-runs at 266MHz for a nominal control voltage of +3.5V and the slope at this point gives

$$K_o \approx \frac{\pi}{2} \cdot 10^6 \text{ rad/V-s}$$

Under locked conditions the control voltage and therefore the sampling phase can be varied using RV1 in Fig. 3.22. In this case a static phase error

$\theta_i - \theta_o$  will be set up to provide the necessary control signal or in other words the phase detector sampling point moves up or down the subcarrier. If the sampled subcarrier has peak amplitude  $V_o$  then, for small errors, the control signal is approximately  $V_o(\theta_i - \theta_o)$ . Hence  $K_D = V_o \triangleq 1.5V/\text{rad}$  and  $K_O K_D \triangleq 2.4 \cdot 10^6 \text{ s}^{-1}$ .

It is conceivable that random noise could result in phase jitter in  $\theta_o$  (thereby increasing the aperture uncertainty time) and to minimise this effect the loop was designed for minimum noise bandwidth<sup>43</sup>. In this case, the damping factor  $\zeta$  is 0.5 so that

$$\tau = (K_O K_D)^{-1} = 4.2 \cdot 10^{-7} \text{ s}$$

Referring to Fig. 3.22 it is clear that  $\tau \triangleq RC/2$  assuming that  $R$  is significantly larger than the diode impedance. A reasonable value for  $R$  is  $220\Omega$  in which case  $C \triangleq 4\text{nF}$  and this is also an adequate value for decoupling the VCO.

The loop performed satisfactorily and pulled-in providing the oscillator frequency was within the range  $266 \pm 5\text{MHz}$ .

### 3.3.2 TIMING SECTION

This section of the encoder generates and provides timing adjustment for the following pulses

counter reset  
ramp reset  
inhibit  
readout  
transfer  
comparator reset

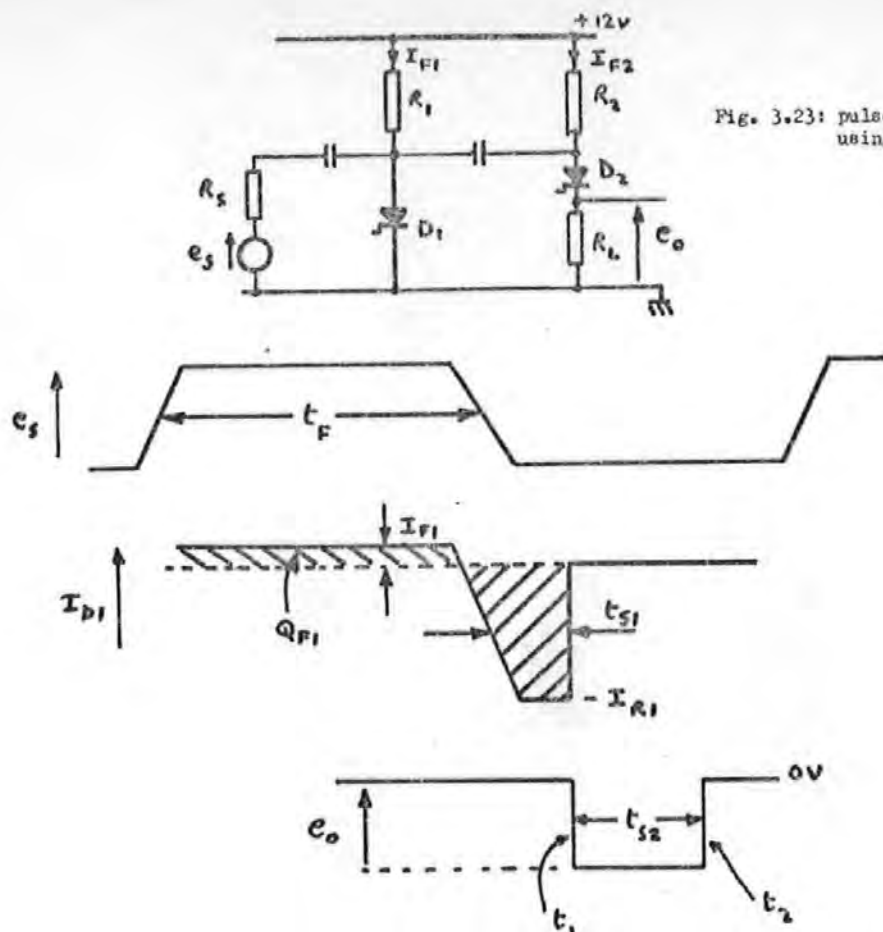


Fig. 3.23: pulse generation using two SRD's.

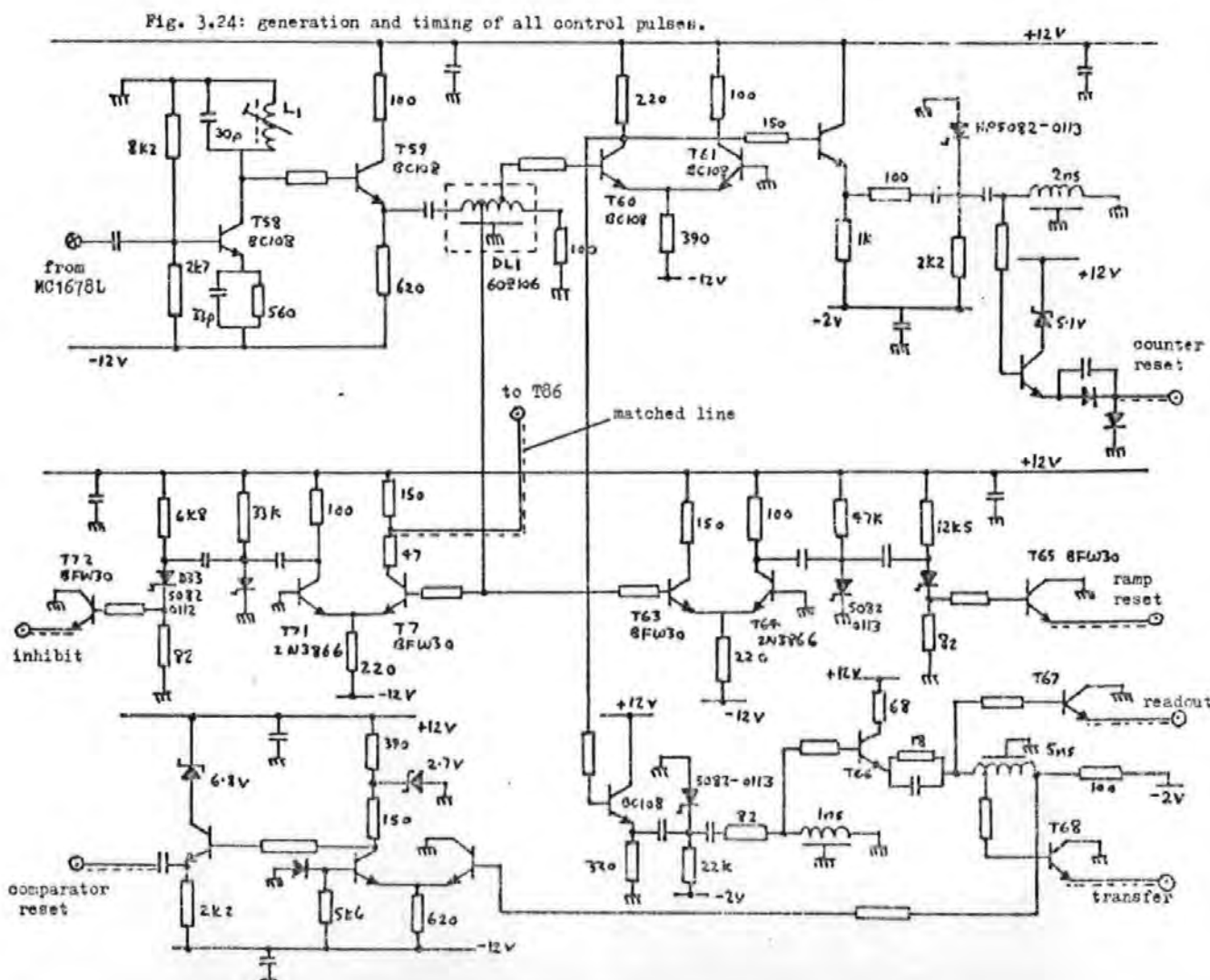


Fig. 3.24: generation and timing of all control pulses.

These pulses must be compatible with ECL and have a p.r.f. equal to the sampling frequency or about 13.3MHz. Also, from the timing system Fig. 3.8 it is apparent that the duration and timing of these pulses must be defined to within 1ns and that the rise and fall times must be about 1ns.

The S.R.D. is ideal for this application since it has a subnanosecond transition time and precision timing of this transition is achieved easily by varying the amount of stored charge. For example, consider the S.R.D. pulse generator shown in Fig. 3.23. If  $D_1$  has been forward conducting for a period  $t_F$  where  $t_F \gg \tau_i$  (the minority carrier lifetime) then the minority carrier stored charge is

$$Q_{F1} \simeq I_{F1} \tau_i$$

When the input signal  $e_s$  falls,  $D_1$  remains forward conducting until the stored charge is removed by reverse current  $I_{R1}$ . During this period  $D_2$  is ON and the output is held near OV since  $D_1$  is low impedance (about  $1\Omega$ ). When all the stored charge is removed  $D_1$  steps OFF and effectively  $I_{R1}$  is applied as a current step to the parallel combination  $R_p$  of the source  $R_s$  and load  $R_L$  such that  $e_o = I_{R1} R_p$ . Equating stored and removed charges

$$I_{F1} \tau_i \simeq I_{R1} t_{s1} \quad (t_F \gg \tau_i \gg t_{s1})$$

$$t_{s1} \simeq \frac{I_{F1} R_p \tau_i}{e_o} \quad (3.9)$$

From eqn. (3.9) it is clear that precision timing of the leading edge of the pulse relative to the input waveform can be achieved by simply varying  $I_{F1}$  via  $R_1$  but on the other hand jitter or longer term drift in the leading edge of the pulse will occur if  $I_{F1}$  is not stable e.g. if  $t_{s1} = 10\text{ns}$ , a 1% peak to peak variation in  $I_{F1}$  due to noise will give a 100ps jitter on the leading edge. Also, the transition time  $t_t$  tends to increase with stored charge (and

therefore with  $t_{s1}$ ) but the stored charge is always small in this application and the effect is negligible.

When  $D_1$  steps off the negative pulse applied to the output forces a reverse current through  $D_2$  and the storage time  $t_{s2}$  of this diode defines the pulse duration. Hence

$$\begin{aligned} Q_{F2} &\approx \frac{e_o t_{s2}}{R_L} & t_F \gg \tau_2 \gg t_{s2} \\ t_{s2} &\approx \frac{I_{F2} R_L \tau_2}{e_o} \end{aligned} \quad (3.10)$$

and precision control of the pulse duration can be achieved by varying  $R_2$ .

Exact calculation of  $R_1$  and  $R_2$  is impossible partly because only nominal values of  $\tau_1$  and  $\tau_2$  are available. It has also been assumed that each diode reaches its steady-state charge  $Q_F$  before the drive signal reverses the diode current, that is  $t_F \gg \tau$ . However, in this application the maximum possible value of  $t_F$  is about 50ns and  $\tau$  is typically 50 - 100ns so that steady-state is never attained. On this basis eqns. (3.9) and (3.10) should yield low values for  $I_{F1}$ ,  $I_{F2}$  or high values for  $R_1$  and  $R_2$ . On the other hand, the rising edge of the drive signal  $e_g$  provides a current pulse  $i(t)$  which aids the forward current  $I_{F1}$  and strictly, the charge continuity equation should be

$$\frac{dQ_{F1}}{dt} = I_{F1} + i(t) - \frac{Q_{F1}}{\tau_1}$$

Normally the charge arising from  $i(t)$  will decay to negligible proportions with time constant  $\tau_1$  but this is not so if  $t_F \approx \tau_1$ . In short, there is an effective forward current  $I(t_F)$  (where  $I(t_F) \rightarrow 0$  as  $t_F \rightarrow \infty$ ) such that

$$Q_{F1} = [I_{F1} + I(t_F)] [1 - e^{-t_F/\tau_1}] \tau_1 \quad (3.11)$$

Eqn. (3.11) provides a plausible explanation of the experimental fact that  $R_1$

can be very high or even omitted completely and the pulse generator will still function; in the sampling pulse generator Fig. 3.11 for example,  $R_1$  was raised to  $1.5\text{M}\Omega$  in order to achieve the required pulse advance.

For the network shown in Fig. 3.23 the output rise and fall times are given by

$$t_1 \simeq \left[ t_{t1}^2 + (2.2 R_P C_{VR1})^2 \right]^{1/2}$$

$$t_2 \simeq \left[ t_{t2}^2 + (2.2 (R_S + R_L) C_{VR2})^2 \right]^{1/2}$$

where  $t_t$  is the diode transition time and  $C_{VR}$  is the depletion capacitance. Taking  $R_S = R_L = 100\Omega$ ,  $t_{t1} < 250\text{ps}$  and  $C_{VR1} < 5\text{pF}$  gives  $t_1 < 600\text{ps}$ . A lower capacitance diode was selected for  $D_2$  such that  $t_{t2} < 175\text{ps}$  and  $C_{VR2} < 1.7\text{pF}$  giving  $t_2 < 800\text{ps}$ . This type of S.R.D. network is used for generating the ramp reset and inhibit pulses, Fig. 3.24; it is also used to generate the sampling pulses and Fig. 3.12 substantiates the above rise-time calculations.

For shorter duration pulses it is more economical to use a single S.R.D. driving into a shorted transmission line and several examples are shown in Fig. 3.24. In this case a positive going drive signal depletes the diode of stored charge and a positive voltage step is then sent down the line as in conventional delay-line pulse generation. The reflected wave is absorbed by the series resistance and, as before, the pulse delay can be adjusted by adjusting the diode forward current. Fig. 3.24 shows that two lines are required, a  $2\text{ns}$  line for the counter reset pulse and a  $1\text{ns}$  line for the remaining pulses. These are realised using microstrip transmission lines since they have wide bandwidth, well defined characteristic impedance and the delay is relatively easy to adjust. The characteristic impedance and delay of a microstrip line have to be defined in terms of an effective dielectric constant  $\epsilon_{re}$  since the dielectric is not homogeneous. KAUPP<sup>46</sup> gives a linear

approximation valid for most microstrip lines as

$$\epsilon_{re} = 0.475 \epsilon_r + 0.67$$

where  $\epsilon_r$  is the relative permittivity of the printed circuit board dielectric.

The line delay is therefore

$$T \approx 3.33 (0.475 \epsilon_r + 0.67)^{1/2} \text{ ns/m}$$

The characteristic impedance  $Z_0$  can be found by transforming from a wire-over ground line, and, using a transformation provided by SPRINGFIELD<sup>47</sup>, KAUPP gives

$$Z_0 \approx \frac{87}{[\epsilon_r + 1.41]^{1/2}} \cdot \ln \left[ \frac{5.98 h}{0.8 W + t} \right]$$

where  $W$  is the line width,  $t$  the line thickness and  $h$  is the dielectric thickness. The lines used had a low loss epoxy dielectric ( $\epsilon_r = 4.5$ ) and the following dimensions

$$t = 1.4 \text{ mil}$$

$$W = 50 \text{ mil approximately}$$

$$h = 62 \text{ mil}$$

The corresponding parameters are  $Z_0 = 78.5 \Omega$  and  $T = 5.6 \text{ ns/m}$  so that a 2ns pulse requires a line about 18cm long. These delay lines provide precision adjustment of the pulse duration whilst the relative timing of the readout, transfer and comparator reset pulses is achieved by a further delay line in the emitter of  $T_{66}$  (Fig. 3.24). This is a constant- $k$  line of delay  $t_d$  and  $Z_0 \approx 100 \Omega$ . The cut-off frequency of the line must be sufficiently high to avoid unacceptable degradation of the output rise-time  $t_r$  and to this end the number of sections required is<sup>48</sup>

$$m \approx 1.1 \left( \frac{t_d}{t_r} \right)^{1.5}$$



The delay of the line and the positioning of the taps obviously depends upon the circuit propagation delays. The comparator reset pulse need only be delayed about 5ns w.r.t. the readout pulse since there is significant propagation delay here due to the layout and further delay occurs in the reset pulse amplifier (Fig. 3.7). The line delay is therefore about 5ns and a delay of about 1ns/section gives an acceptable risetime.

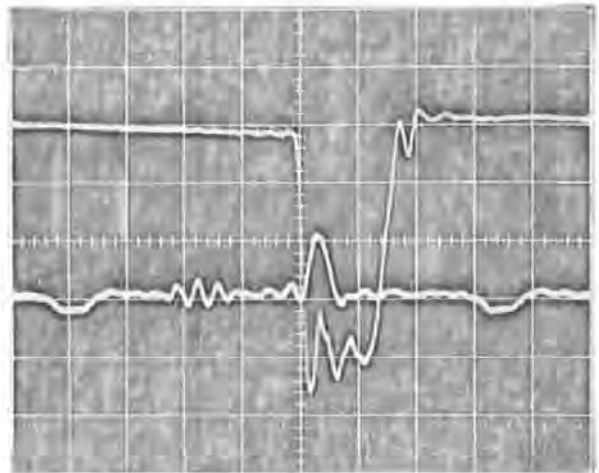
All these pulses must be correctly timed relative to the leading edge of the sampling pulse and to this end a coarse timing adjustment is provided by DL1, Fig. 3.24. The bandpass amplifier  $T_{58}$  selects the (nominal) 13.3MHz fundamental from the output of the MC1678L so that a commercial delay-line can be used; this is a 50ns lumped constant line with 5ns taps and an output risetime of 12ns. Obviously the delay also depends upon L1 since a bandpass amplifier off resonance has a finite phase shift. Therefore, a combination of L1 and DL1 provided a coarse timing adjustment and final adjustments were done in the S.R.D. circuits. Fig. 3.25 illustrates the precision timing that could be achieved by the above arrangement. The upper trace shows a sampling pulse measured across a 100 $\Omega$  load shunting the secondary of the pulse transformer and the lower trace shows the readout pulse at the output register. The figure should be compared with the theoretical timing system in Fig. 3.8.

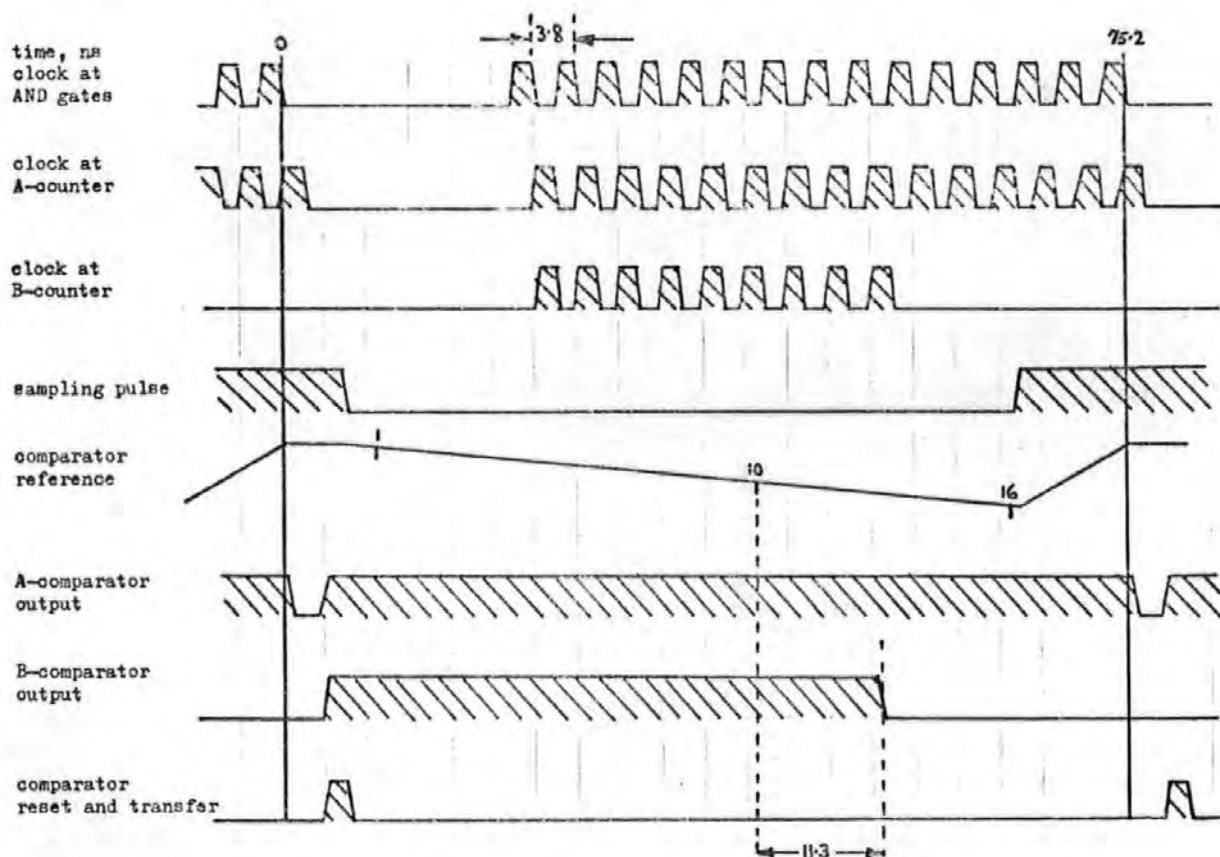
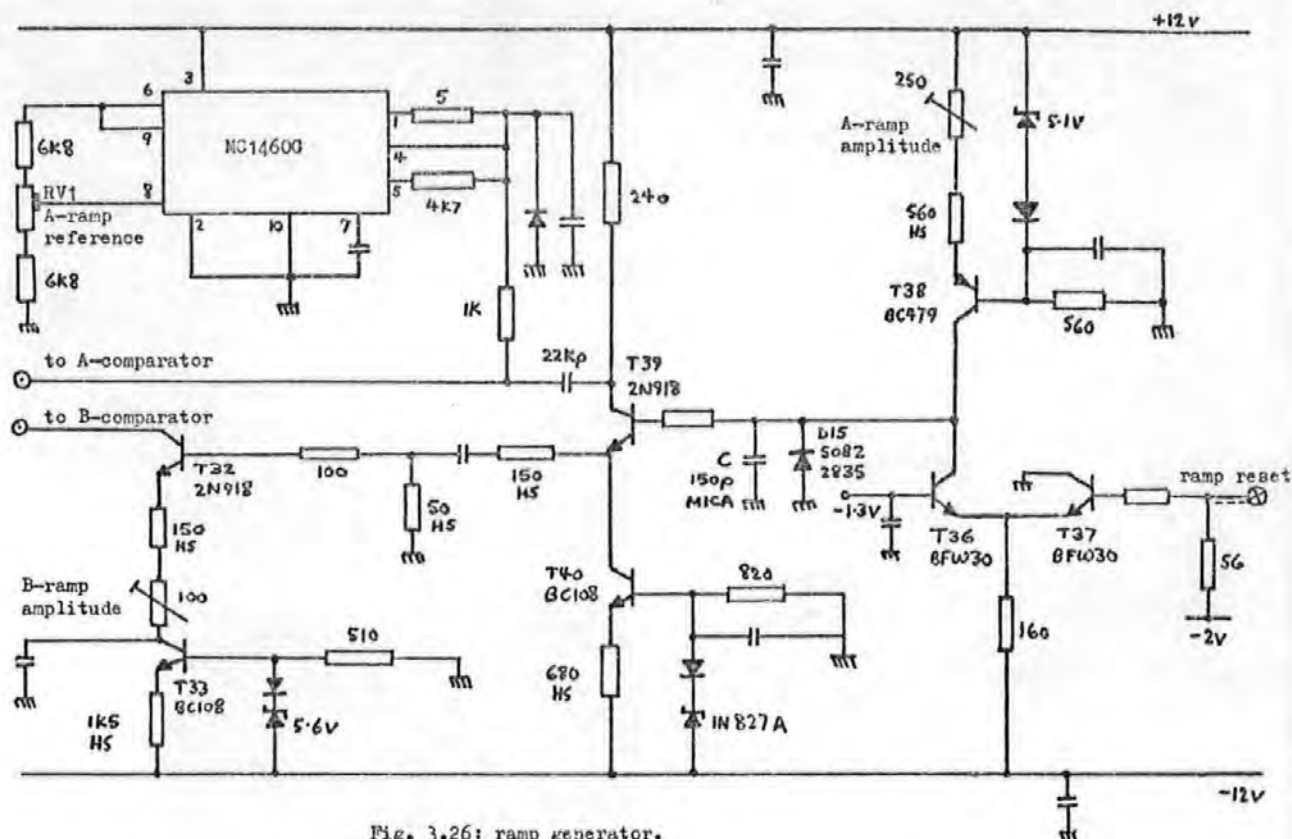
Fig. 3.25:

Upper trace: sampling pulse

Lower trace: readout pulse

Scales: 1V/div, 10ns/div





### 3.3.3 CODING SECTION

This section describes the elements of the PWM encoding loop, that is, the ramp generator, analog comparator and the gating, counting and storage elements. The problems involved in the design of the high-speed 4-bit decoder are considered in section 3.3.4.

The ramp generator must provide two, synchronous, 13.3MHz ramps, one of 3V amplitude and one of  $3/16$ V amplitude. The ramps must be highly linear and the amplitude and mean level of each ramp must be adjustable and stabilised against temperature variations. Expressing nonlinearity as the maximum deviation from a straight line drawn between two fixed end points, an intuitive value aimed for was  $\pm 1q$  (although, according to the numerical analysis in chapter 6 even this is probably too high). We can deduce from Fig. 3.8 that the linear period should extend from the 1<sup>st</sup> to the 15<sup>th</sup> interrogation pulse or for at least 53ns. Any nonlinearity after the 15<sup>th</sup> interrogation pulse could be tolerated since this simply means that the 16<sup>th</sup> interrogation pulse may fail to reset the comparator. If this occurs, the counter will still reach full-scale count and remain there until reset since the clock is inhibited during the data transfer period. As the sample period is about 75ns a linear period of at least 53ns means that the ramp must be reset within 22ns.

The circuit in Fig. 3.26 sufficed for the prototype encoder although slight ramp nonlinearity and slight damped ringing can be observed at the start of the ramp. These voltage errors are of the order of  $1q$  and probably arise from depletion capacitances (since they are voltage dependent) and from the high slew-rate of the capacitor discharge current respectively. The temperature stability of the circuit is also important and any drift in the ramp amplitude, for instance, will cause incorrect tracking of the ramp with the 4-bit decoder. Even for a modest temperature range of  $\pm 10^{\circ}\text{C}$  both  $C$  and

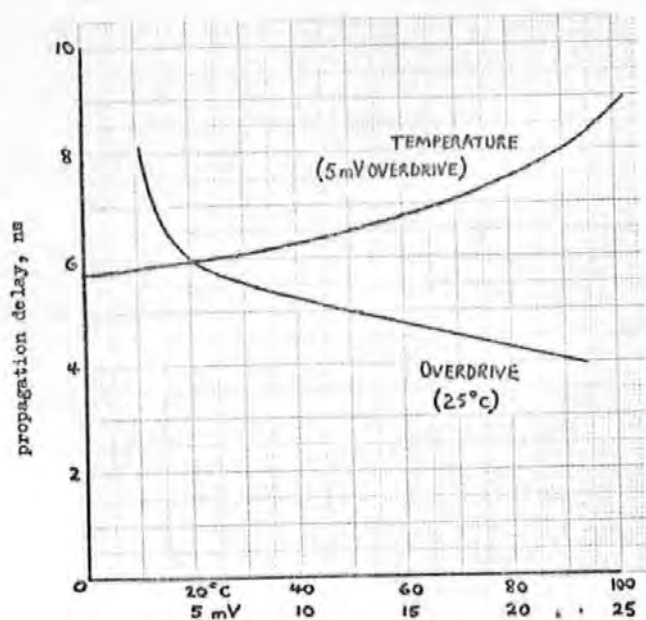


Fig. 3.28: variation in propagation delay for high speed comparator type Am685 (ADVANCED MICRO DEVICES INC.)

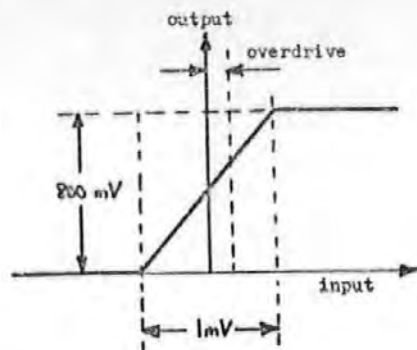


Fig. 3.29: required comparator transfer characteristic

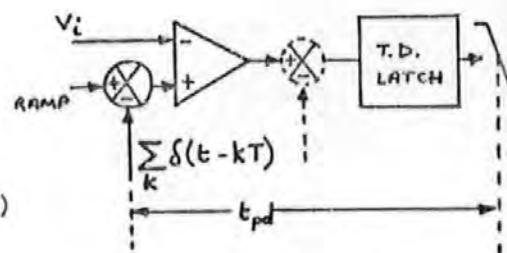


Fig. 3.30: ultra high speed comparator

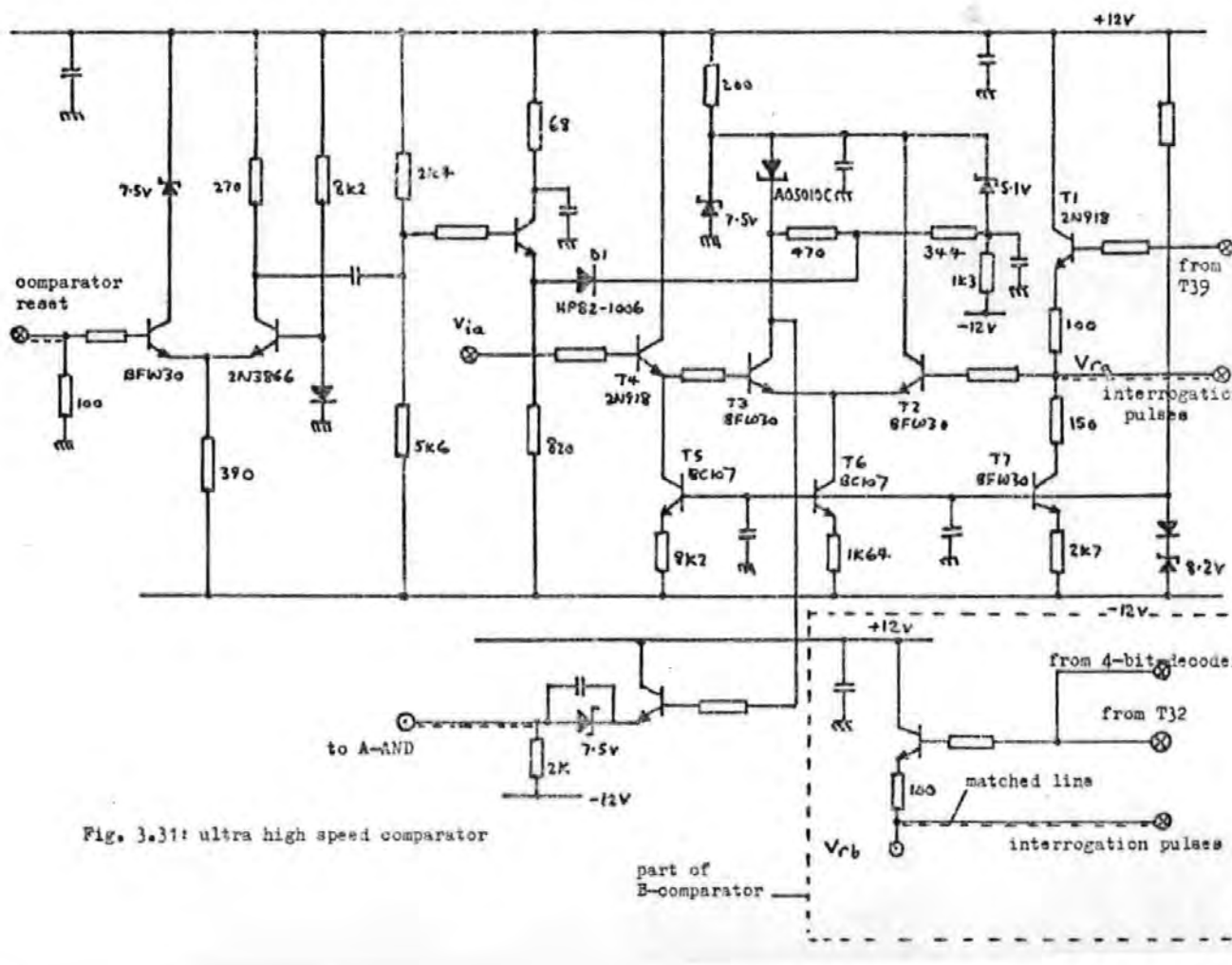


Fig. 3.31: ultra high speed comparator

$T_{38}$  emitter resistance should each have a temperature coefficient  $< 100 \text{ppm}/^{\circ}\text{C}$  to keep the ramp amplitude errors within  $\pm q/2$ .

The most difficult circuit design problems are associated with the analog comparators and this can be illustrated by taking two examples. In section 3.1 for example it was stated that for minimum ambiguity in AND gate operation the comparator transitions should occur very rapidly during a clock 0 and this implies a very high output slew-rate of approximately  $1\text{V/ns}$ . It was also stated that the comparator propagation delay should be less than the clock period and, at the time of design, both of these requirements were about an order better than the corresponding performance of any commercially available device! The reason why the propagation delay should be of this order is not difficult to see; suppose for example that we modified the timing system in Fig. 3.3 to accommodate a comparator propagation delay corresponding to 3 clock periods, approximately  $11.3\text{ns}$ . This can be done by advancing the comparator reference waveform and certain other timing waveforms by  $11.3\text{ns}$  as illustrated in Fig. 3.27 but unfortunately such a timing system is not satisfactory for several reasons. Firstly, it assumes that the comparator propagation delay is constant whereas it is likely to vary with temperature and with comparator overdrive (this is illustrated in Fig. 3.28 for an advanced monolithic comparator). Secondly, the data transfer period is now reduced by about 50% and the timing becomes too critical. Hence, to minimise the effects of temperature and overdrive variations and to give the maximum possible data transfer period (which even then is critical) it is necessary to minimise the nominal propagation delay. A delay less than one clock period is therefore a reasonable objective.

To achieve this delay means that the comparator circuit (usually a differential amplifier) must be relatively simple and wideband, but this is



in direct conflict with the gain (or resolution) requirements indicated in Fig. 3.29. In this application the comparator should be able to resolve voltage changes  $\ll 1q$ , say  $1mV$ , so that the small signal gain should be about 800 to achieve an output swing compatible with ECL. Furthermore, it is theoretically possible to obtain an ambiguous output if the input differential is very small (very small overdrive). The problems of low gain and output ambiguity can be solved if the differential amplifier is followed by a high-speed latch since this makes a definite decision as to the state of the differential amplifier and effectively increases the comparator gain. A latch is also essential if the comparator is to be strobed with interrogation pulses. The obvious choice is a strobed D-type flip-flop but then the comparator resolution will depend upon the duration of the strobe pulse and if the amplifier gain is low (10) and the duration of the pulse is about  $1ns$  it is unlikely that the overall resolution could be reduced to the order of  $1mV$ .

It was therefore decided to follow the work of SCHINDLER<sup>41</sup>, JOHANNESSEN<sup>26,60</sup> and others who have successfully realised ultra high-speed comparators using tunnel-diodes. SCHINDLER used a tunnel-diode monostable to trigger a tunnel-diode bistable and JOHANNESSEN used a tunnel-diode monostable formed by placing the diode in the emitter circuit of a differential pair. The arrangement finally adopted is shown in Fig. 3.30, this shows a simple wideband differential amplifier coupled to a tunnel-diode latch. The strobe pulses synchronise the comparator triggering to the clock such that the comparator output transition coincides with a clock zero as previously discussed. The strobe pulses could be added after the comparator as indicated but it was found easier to add the pulses at the comparator input; the pulses then provide discrete reference levels as illustrated in Fig. 3.5. The arrangement in Fig. 3.30 gives a very low propagation delay ( $t_{pd} \approx 2ns$ ), a

subnanosecond comparator output transition and a theoretically high comparator resolution. For example, suppose the tunnel-diode forming the latch is in its low voltage state but is taken to its peak point ( $I_p$ ,  $V_p$ ) by a strobe pulse. The diode requires negligible energy  $\Delta E$  to change from its low voltage state to its high voltage state, one estimate<sup>48</sup> gives  $\Delta E \approx 10^{-15} \text{ J}$ . The state change could be effected by increasing the strobe pulse amplitude at the diode by  $\Delta V$  such that

$$\Delta E \approx I_p \Delta V \Delta t$$

where  $\Delta t$  is the pulse duration. Taking  $\Delta t = 0.5 \text{ ns}$  and  $I_p = 10 \text{ mA}$  gives  $\Delta V \approx 0.2 \text{ mV}$  and the required change at the comparator input would be significantly lower than this due to the gain of the differential amplifier.

The circuit diagram for the A-comparator is shown in Fig. 3.31. Negative going interrogation pulses at  $T_2$  base apply progressively larger current pulses to the tunnel-diode and the comparator output goes low when  $I_p$  is exceeded. One criterion in the design was to ensure that the circuit remains stable even under large overdrive conditions ( $T_3$  hard ON). This is achieved in the final circuit as shown in Fig. 3.32; increasing overdrive takes the tunnel-diode out of its stable state Q towards state R so that the circuit is always stable.

The comparator resolution can be measured by replacing  $V_{ia}$  (Fig. 3.31) with a variable direct voltage supply and then observing the change in  $V_{ia}$  required to change the number of pulses at the output of the corresponding AND gate (Fig. 3.33, for example, shows the gate output for a full scale analog input,  $V_{ia} = +3\text{V}$ ). Although the theoretical resolution is  $\ll 1 \text{ mV}$ , in practice there was a measurable threshold 'blurr' and using a sampling oscilloscope the output appeared similar to a hysteresis loop as the comparator dithered between two stable states A and B over a  $V_{ia}$  range of

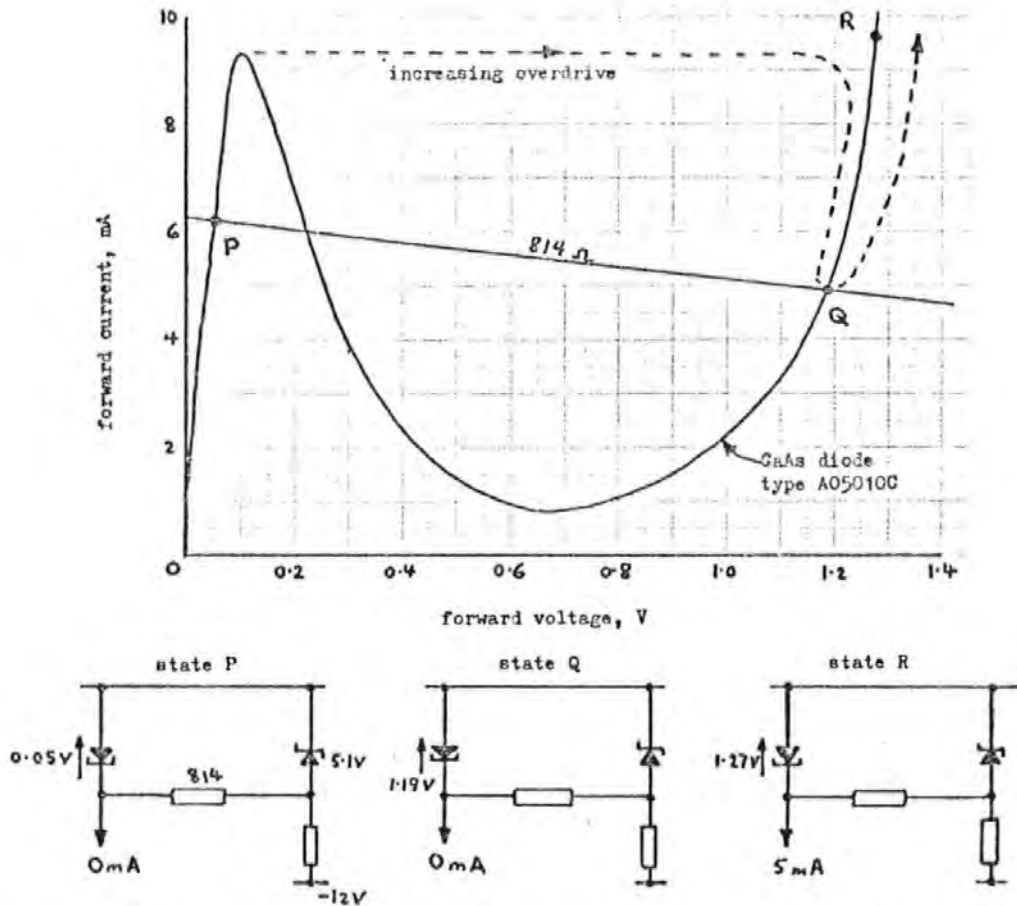


Fig. 3.32: effect of overdrive on tunnel-diode latch

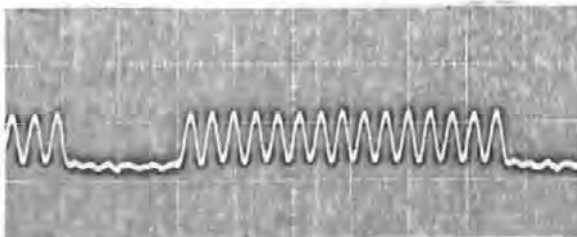


Fig. 3.33: AND-gate output for  $V_{ia} = +3V$ .

Scales: 1V/div, 10ns/div.

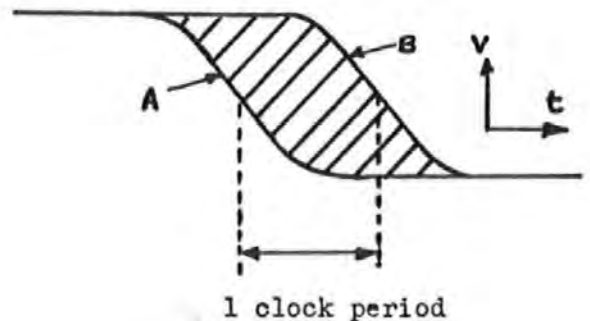


Fig. 3.34: comparator output at threshold showing a threshold blurr

several mV, see Fig. 3.34. It was concluded that circuit noise levels, which were of the order of 1mV rms, were probably responsible for this since a change in diode voltage of only 0.2mV is theoretically sufficient to trigger the diode when at its peak point  $(I_p, V_p)$ .



Fig. 3.35: threshold error over the quantizing range

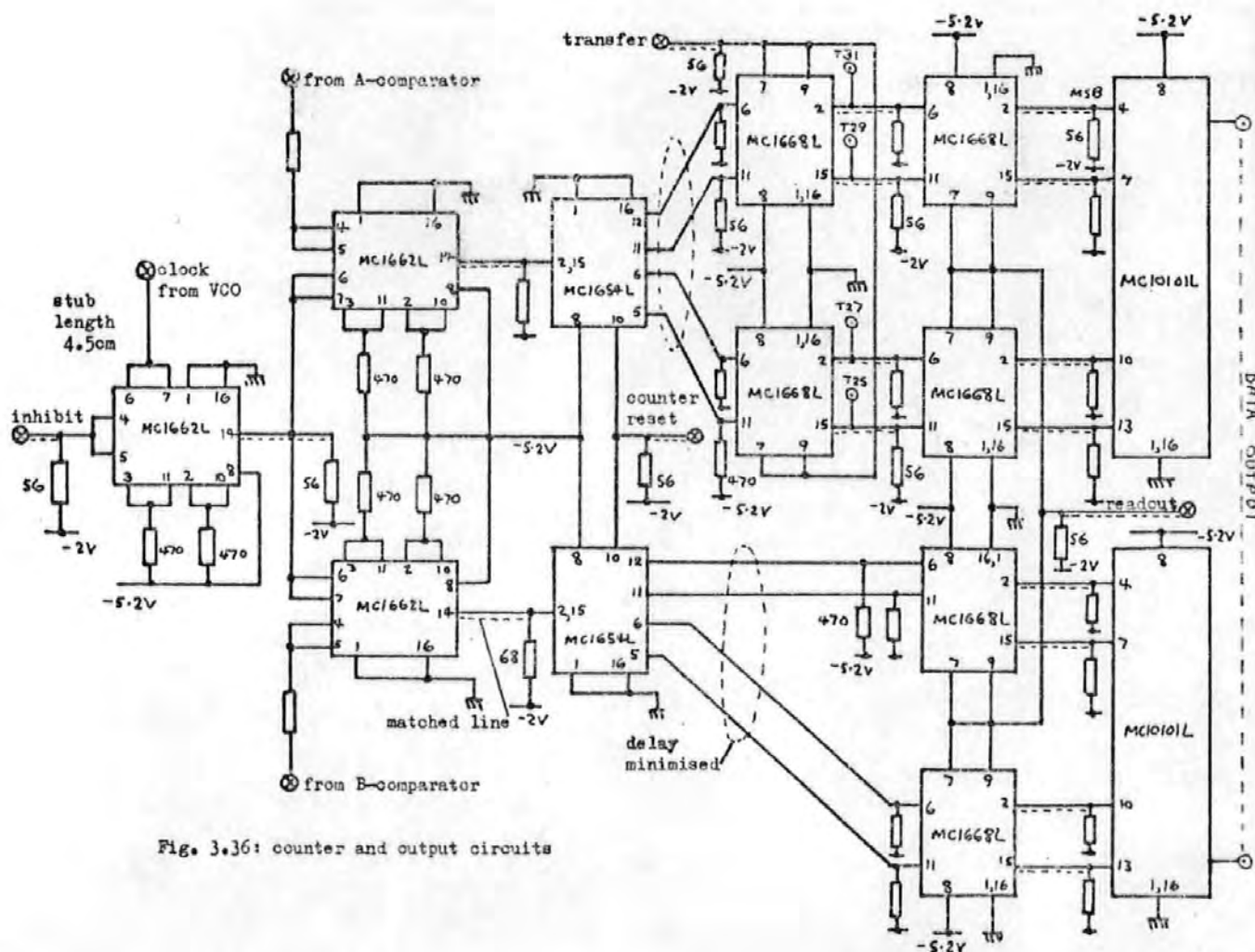
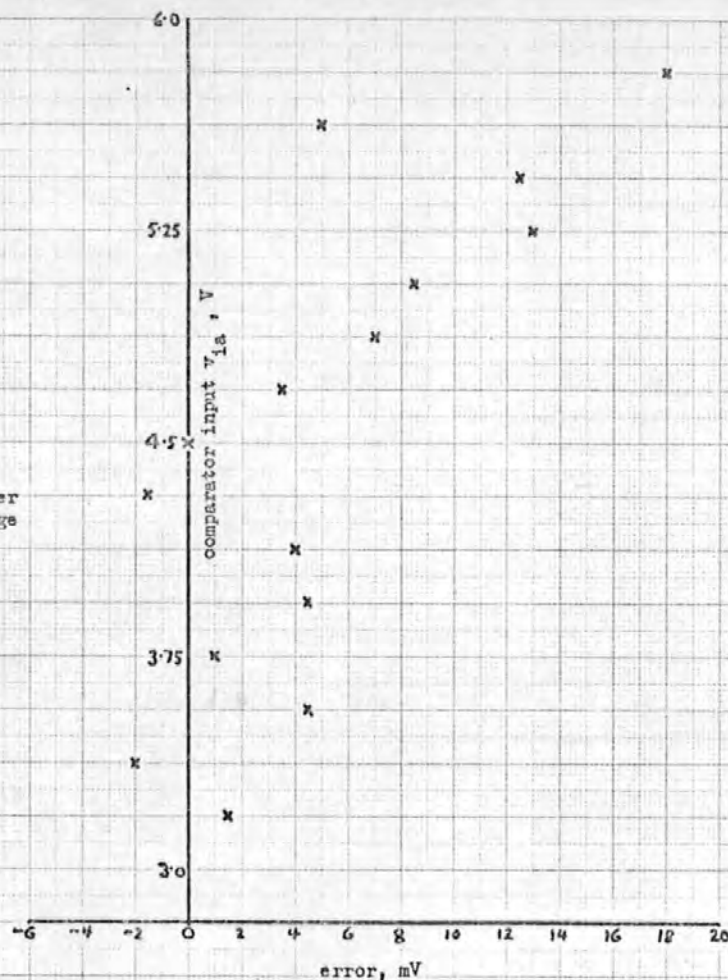


Fig. 3.36: counter and output circuits

Linearity measurements were made in a similar way; observations were made of the change in  $V_{ia}$  required to cause a change in the number of clock pulses at the AND gate output. Clearly the result also depends upon the ramp linearity so this is really a measure of overall coding linearity. The ideal threshold levels for the A-comparator are defined as

$$e(n) = 6 - 0.1875n \quad V \quad (n=1, \dots, 15)$$

so the A-RAMP AMPLITUDE was adjusted such that the mean analog change required to cause a change in AND gate output was 187.5mV. The A-RAMP REFERENCE was then set such that the AND gate output just changed from 8 to 7 clock pulses as  $V_{ia}$  was increased above +4.5V thus setting the threshold error at mid-scale to zero. The remaining thresholds were measured and the threshold error was plotted as a function of the analog input  $V_{ia}$ . The graph, Fig. 3.35, shows considerable spread although some of this is due to measurement uncertainty arising from finite comparator resolution. Also, if these measurements were made relatively slowly it was found that upon returning to mid-scale ( $V_{ia} = +4.5V$ ) a drift of about 10mV had occurred due to transistor  $V_{be}$  variations with temperature. Nevertheless, there is a tendency to a positive error for high  $V_{ia}$  and the behaviour for very small analog signals ( $V_{ia} \approx +6V$ ) tends to be particularly erratic. The results appear to reflect the slight non-linearity at the start of the ramp referred to earlier in this section although fortunately the worst threshold error occurs for synchronizing information and for the relatively rare occurrence of highly saturated low luminance colours.

To summarize, the comparator resolution appears to be limited by random noise but is considered to be adequate for experimental purposes since any ambiguity in the threshold is still significantly less than 1q. Also the coding linearity is accurate to within 1q over the analog range except for very

low level analog inputs.

The remaining elements in the coding section use MECL III IC's (1ns rise and fall time). Referring to Fig. 3.36, each AND gate comprises 3 NOR gates which are interconnected using 470 $\Omega$  pulldown resistors instead of the more usual 50 $\Omega$  line termination. This is permissible for electrically short interconnections (<4.5cm approximately) and has the advantage of reducing the NOR gate propagation delay by 20%. A similar approach can be used for the interconnections at each counter output so that the transfer and readout pulses can be advanced as much as possible. Consequently, each AND gate had a nominal propagation delay of only 2.0ns (approximately 1.9ns is assumed in the timing diagram) and on test functioned satisfactorily up to 300MHZ. The basis of the asynchronous counters, store and output register is a very high-speed D-flip-flop having a nominal propagation delay of 1.8ns and a maximum toggle frequency of 325MHZ. The complementary outputs of each flip-flop in the output register could be used to give a differential transmission capability although actual line drivers were used in the prototype encoder.

#### 3.3.4 4-BIT and 8-BIT VIDEO DECODERS

Although decoder design is well established special care has to be taken in the design of video decoders due to the very high circuit speeds involved. A fast response is particularly important for the 4-bit decoder and this is considered first.

Referring to the timing system in Fig. 3.8 it is seen that the Q outputs of the store are available at  $t \approx +5.6ns$  i.e. 1.8ns after the leading edge of the transfer pulse. Since the 4-bit decoder output should have settled before the first strobe pulse occurs (at  $t = +17.8ns$ ) it follows that the decoder settling time must be  $< 12.2ns$  and to allow some margin for timing

errors a 10ns settling time is a reasonable objective (although at the time of design this was less than half the settling time of the fastest commercially available device). This stringent specification is best achieved using a weighted current type decoder since propagation delays arising from the ladder networks used in more conventional decoders are eliminated. Other design requirements are,

1. ECL compatability since the decoder is driven directly from the store.
2. Full scale output and mean output should each be adjustable to within 1q to ensure acceptable alignment of the two coding scales (Fig. 3.5).
3. Minimal temperature drift.
4. Negative going output.

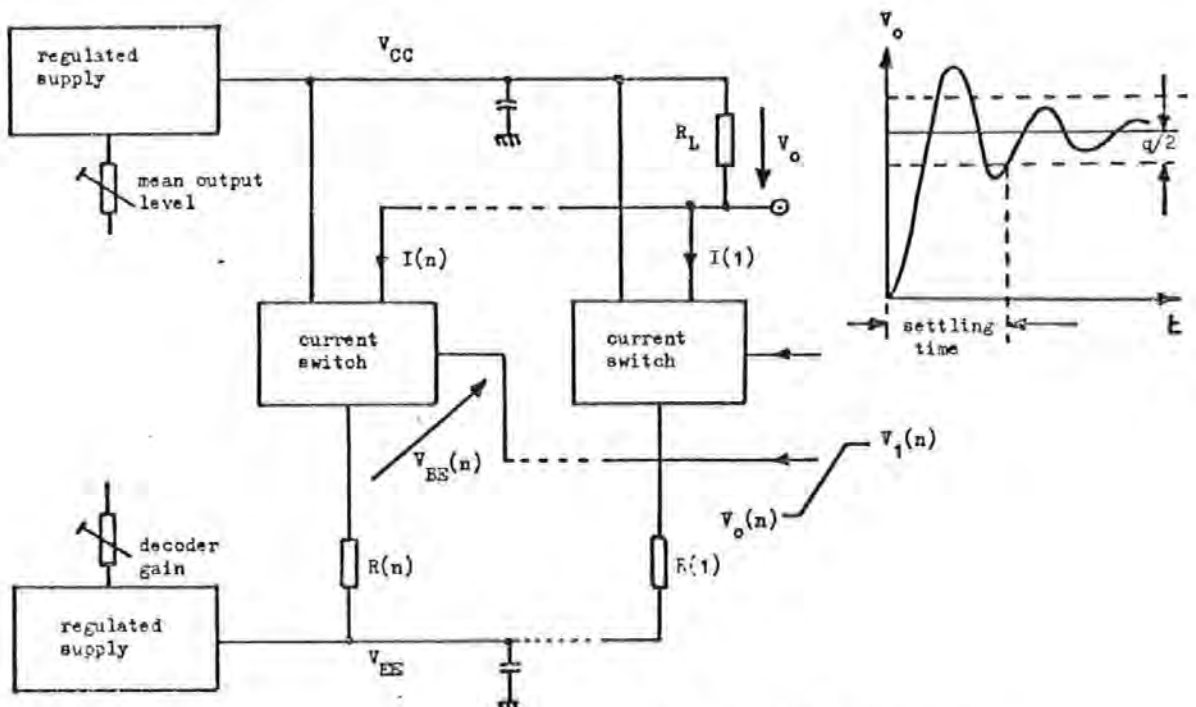


Fig. 3.37: high speed decoder

The basic arrangement is shown in Fig. 3.37. Binary weighted resistors  $R(n)$  provide weighted currents which are steered using emitter coupled switches and ideally the output voltage is given by

$$|V_o| = I(1) R_L \sum_{n=1}^4 \left( \frac{D_n}{2^{n-1}} \right) \quad D_n = 1 \text{ or } 0$$

In general, error occurs in  $V_o$  due to error in the binary weighting which in turn depends upon  $V_1(n)$ ,  $V_{BE}(n)$  and  $R(n)$ . The effect of error in  $V_1(n)$  and

$V_{BE}(n)$  can be reduced by making  $V_{EE}$  large and a suitable value is calculated below. If there is no current loss through the switches the  $n^{\text{th}}$  weighted current is

$$\overline{I}(n) = (\overline{V}_i(n) - \overline{V}_{BE}(n) - \overline{V}_{EE}) / \overline{R}(n)$$

where the bar denotes nominal (or undeviated) values. Hence,

$$dI(n) = (dV_i(n) - dV_{BE}(n) - dV_{EE} - \overline{I}(n)dR(n)) / \overline{R}(n)$$

so the fractional current error is approximately

$$\frac{\Delta I(n)}{\overline{I}(n)} = \frac{\Delta V_i(n) - \Delta V_{BE}(n) - \Delta V_{EE}}{\overline{V}_i(n) - \overline{V}_{BE}(n) - \overline{V}_{EE}} - \frac{\Delta R(n)}{\overline{R}(n)}$$

Assume that  $V_{EE}$  is large and stabilized so that

$$\left| \frac{\Delta I(n)}{\overline{I}(n)} \right|_{\max} = \pm \left( \frac{|\Delta V_i(n)| + |\Delta V_{BE}(n)|}{|V_{EE}|} + \left| \frac{\Delta R(n)}{\overline{R}(n)} \right| \right) = K(n)$$

The actual value of the  $n^{\text{th}}$  weighted current is then

$$I(n) = (1 + K(n)) \overline{I}(n) / 2^{n-1} \quad n=1, \dots, 4$$

It follows that equally spaced voltage reference levels will not be generated since  $K(n)$  is finite and the worst spacing error could occur at the centre of the 4-bit code raster. For a 0111 to 1000 change the maximum error,  $e$ , in the decoder output change occurs when  $K(1)$  is of opposite sign to  $K(2)$ ,  $K(3)$  and  $K(4)$  i.e.

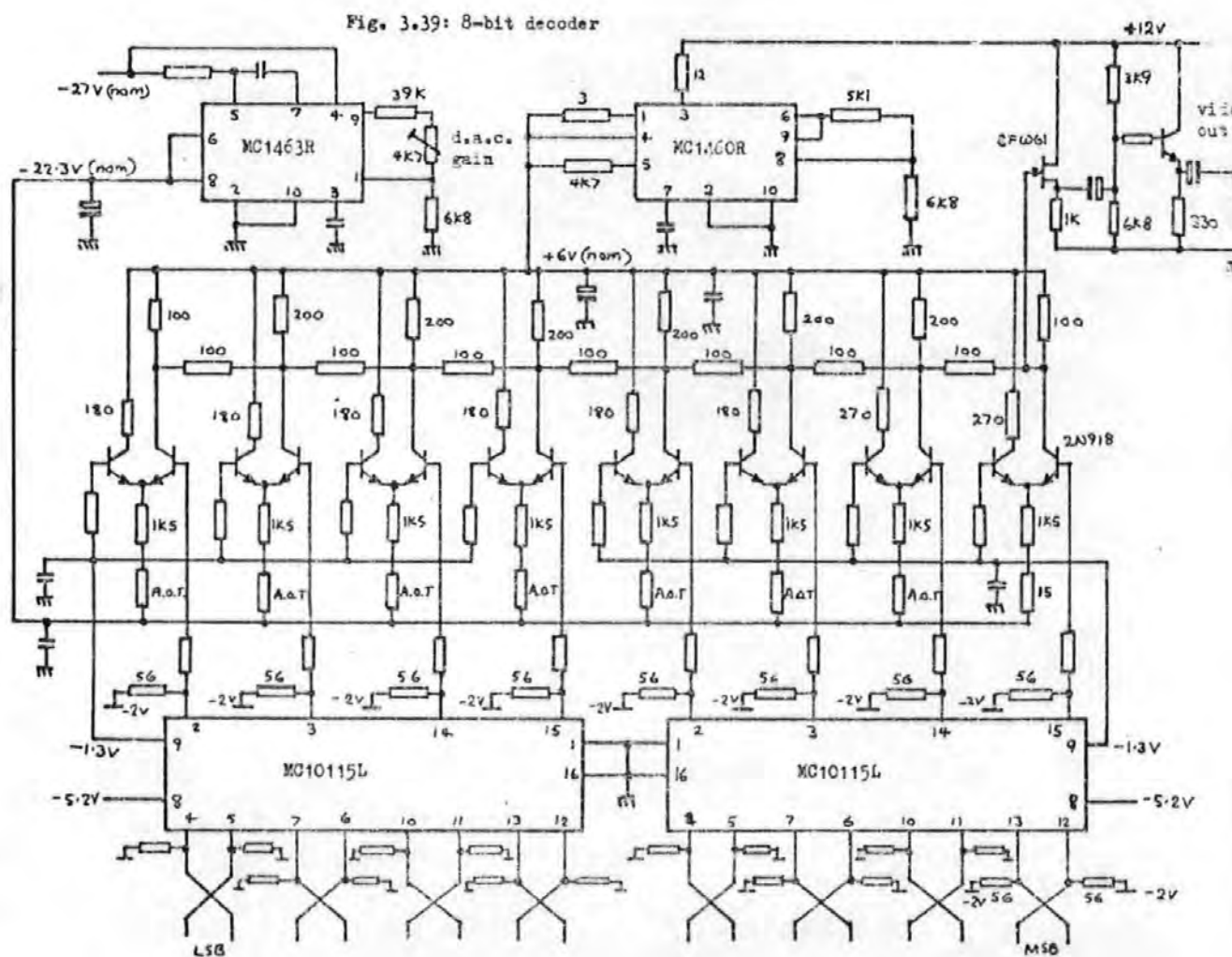
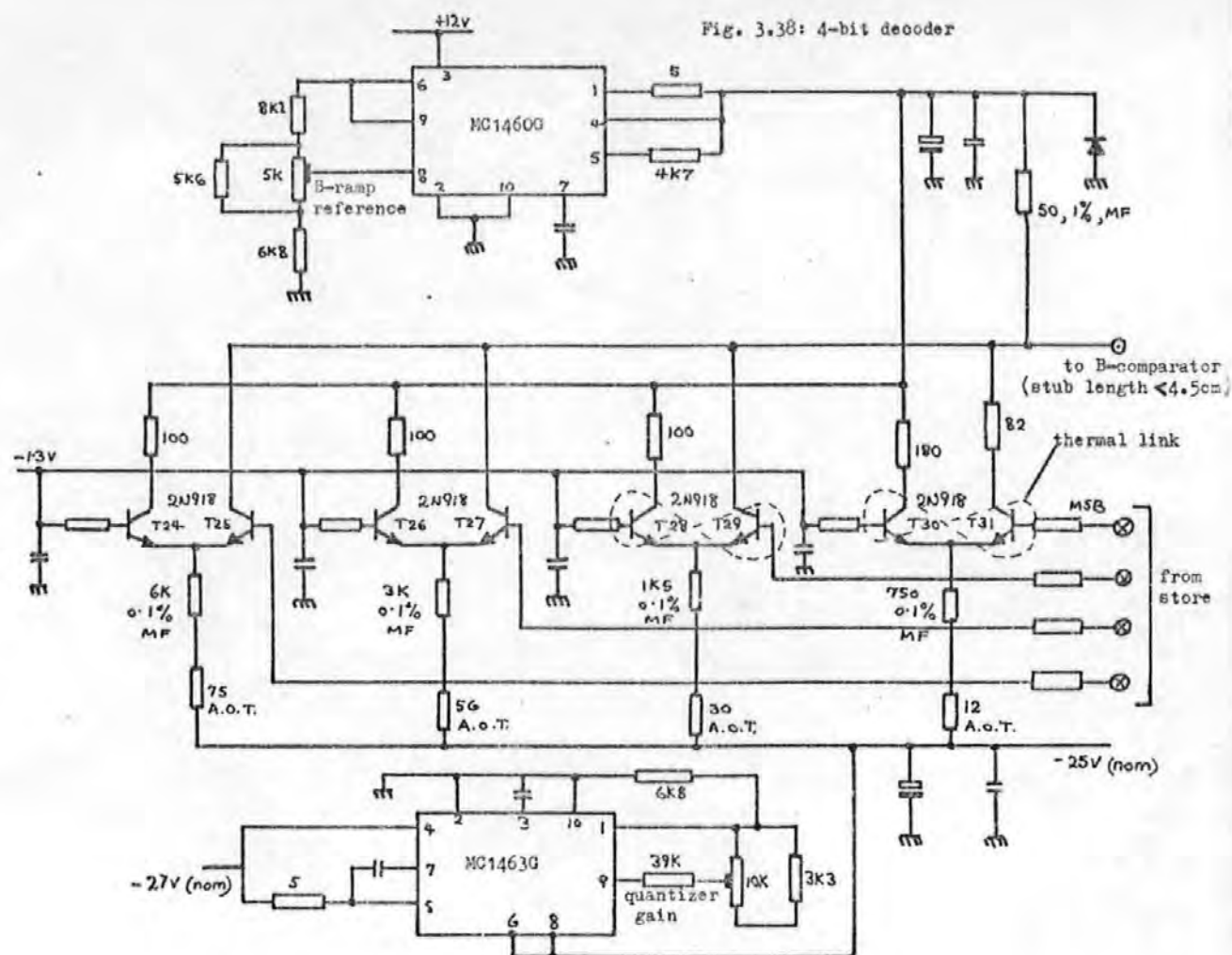
$$e = R_L \overline{I}(1) \sum_{n=1}^4 \left( \frac{K(n)}{2^{n-1}} \right)$$

Since this is an extreme case it is probably sufficient to require  $e < q$ .

Also, for simplicity all  $K(n)$  are assumed equal in magnitude in which case

$$|K(n)| < 0.42\% \quad \text{for 8-bit coding}$$





The manufacturing spreads in  $\Delta V_1$  and  $\Delta V_{BE}$  are typically  $\pm 75\text{mV}$  and  $\pm 20\text{mV}$  respectively for a specified temperature ( $25^\circ\text{C}$ ) and if  $R(n)$  has  $\pm 0.1\%$  tolerance it follows that  $V_{EE} > 30\text{V}$  approximately. Clearly a large  $V_{EE}$  also minimises the effect of temperature variation in  $V_1(n)$  and  $V_{BE}(n)$  and the error is negligible over a modest ambient temperature range ( $\pm 10^\circ\text{C}$ ) if  $V_{EE}$  is of the order of  $30\text{V}$ .

In practice  $V_{EE}$  was only  $-25\text{V}$  (due to power supply limitation) and to ensure precise binary weighting the  $R(n)$  were trimmed as shown in the circuit diagram, Fig. 3.38. When the encoder had reached its steady state temperature the gain (i.e.  $V_{EE}$ ) was adjusted to set the MSB output to  $1.5000\text{V}$  using a DVM accurate to  $\pm 0.1\text{mV}$  and the remaining bits were then aligned to the tolerances shown below

| Bit               | Theoretical output, V | Trimmed output, V( $\pm 0.1\text{mV}$ ) |
|-------------------|-----------------------|-----------------------------------------|
| 1                 | 1.5000                | 1.5000                                  |
| 2                 | 0.7500                | 0.7499                                  |
| 3                 | 0.3750                | 0.3753                                  |
| 4                 | 0.1875                | 0.1878                                  |
| full scale output | 2.8125                | 2.8130                                  |

Unfortunately, due to the high currents involved ( $I(1) = 30\text{mA}$ ) the MSB switch dissipates enough power to cause significant drift ( $7\text{mV}$ ) in the decoder output when  $T_{31}$  is first switched ON. This drift was reduced to 2 or  $3\text{mV}$  by providing a thermal link between  $T_{30}$  and  $T_{31}$  although the only really satisfactory solution is to integrate the decoder.

Dynamic measurements were made by applying a square wave to the store MSB data input with the transfer input enabled. The decoder output was found to settle to within  $q/2$  about  $10\text{ns}$  after the change at the data input. In other words, the decoder settling time is about  $8.2\text{ns}$  (assuming  $1.8\text{ns}$  delay



in the store) and this is well within the 12.2ns limit discussed at the beginning of this section. Finally it should be noted that overshoot and ringing on the stub connecting the store to the decoder can cause ripple on the decoder output. Ringing of 100mV peak to peak can significantly affect the output so the stub must be heavily damped.

Each sample is output from the encoder as an 8-bit parallel word in NRZ (100%) code and appears at the 8-bit decoder, Fig. 3.39, via line receivers. The 8-bit decoder uses an R, 2R ladder network ( $R = 100\Omega \pm 0.1\%$  50ppm/ $^{\circ}\text{C}$ ) in preference to a weighted current decoder since the latter requires a large current range for 8-bit resolution. The ladder network is driven by 8 switchable current sources each of 15mA and this gives a 2V full scale video signal which is then bandlimited to recover the baseband signal (filter not shown in Fig. 3.39). The current sources were trimmed such that the worst output error for any one bit was only 0.3mV; since  $q = 7.8\text{mV}$  this means that static error can be neglected for ambient temperatures near the alignment temperature ( $25^{\circ}\text{C}$ ). However, there is a small but significant dynamic error arising from the nature of the quantized video signal  $V(t)$ . Since the encoder output code is NRZ,  $V(t)$  can be considered as an amplitude modulated pulse train where the pulse duration is very nearly equal to the sample period  $t_s$ . This pulse train can be represented as the convolution of a gate function  $G(t)$  (unit amplitude and duration  $t_s$ ) with an impulse sampled signal, that is

$$V(t) = G(t) * f(t) \sum_{n=-\infty}^{\infty} \delta(t - nt_s) \quad (3.12)$$

Here  $f(t)$  represents the codec video input if all other codec errors including quantizing error are neglected. If

$$f(t) \longleftrightarrow F(\omega)$$

then impulse sampling theory gives

$$f(t) \sum_{n=-\infty}^{\infty} \delta(t - nt_s) \longleftrightarrow \frac{1}{t_s} \sum_{n=-\infty}^{\infty} F(\omega - n\omega_s)$$

where  $t_s = 2\pi/\omega_s$ . Also,

$$G(t) \longleftrightarrow t_s S_a\left(\frac{\omega t_s}{2}\right)$$

The time convolution theorem can now be applied to eqn.(3.12) to give the Fourier transform of  $V(t)$ ,

$$V(\omega) = S_a\left(\frac{\omega t_s}{2}\right) \sum_{n=-\infty}^{\infty} F(\omega - n\omega_s)$$

so that the base band signal is

$$F'(\omega) = S_a\left(\frac{\omega t_s}{2}\right) F(\omega) \quad (3.13)$$

Eqn. (3.13) shows that the video spectrum is distorted due to the finite duration of the decoder output pulses and the loss is about 1.6dB at subcarrier frequency and 2.5dB at 5.5MHz. No frequency compensation was applied although one solution would be to strobe the encoder output with narrow pulses so that the decoder output approximates to impulse sampling; 10ns strobe pulses would reduce the loss at 5.5MHz to 0.7dB.

### 3.3.5 IMPLEMENTATION

The use of very high speed logic means that logic interconnections very quickly become electrically long and so require correct termination to avoid overshoot or rise-time degradation. Many logic interconnections therefore use matched, wideband, microstrip transmission lines fabricated on low loss double sided p.c.b. and this also affords some intercomponent screening if the components are mounted close to the earth plane side of the board. A line can only be regarded as electrically short if the line delay  $t_d$

is significantly less than the signal rise-time  $t_r$  and according to JARVIS<sup>50</sup> this can usually be taken to mean when  $t_d < t_r/4$ . Taking  $t_r = 1\text{ns}$  and the line delay  $T = 5.6\text{ns/m}$  (section 3.3.2) this means that any stubs such as those between the store and the 4-bit decoder should be  $< 4.5\text{cm}$  unless series damping is used.

Other factors to bear in mind are earth loops, circuit delays, power dissipation and rf decoupling. Earth loops are minimised by implementing the encoder on a single p.c.b. and certain propagation delays, such as between the A-counter and store must also be minimised. The packing density can therefore be high and combining this with the high power dissipation of low impedance circuits (the encoder dissipation is about  $21\text{W}$ ) means that the power density could become a serious problem in this type of encoder<sup>50,86</sup>. The random noise level in the encoder was initially about  $10\text{mVrms}$  - presumably aided by the high operating temperature ( $100^\circ\text{C}$ ) of some components and careful decoupling using polystyrene capacitors was necessary to reduce this to the order of  $1\text{mVrms}$ .

### 3.4 SUMMARY

The design philosophy and circuit details for a prototype P.W.M. video encoder have been described and the more significant aspects of the chapter can be summarized as follows:

- (a) The rather difficult concept of aperture uncertainty error in sample and hold circuits is explained in relation to the circuit used and a design criterion is developed.
- (b) The need for a fast analog switch ( $10\text{ns}$  switching time) and a fast analog comparator ( $t_{pd} \approx 2\text{ns}$ ) have been met with some success although the performance of both circuits would undoubtedly be

improved if they could be integrated.

- (c) The proposed timing system requires pulse timing and pulse duration to be accurately controlled to within  $1\text{ns}$  and it has been demonstrated that this is quite feasible using SRD's. However it should be noted that the theory usually associated with these devices (eqns. (3.9) and (3.10)) should be modified if, as in this application, the diodes never reach their steady-state forward charge due to the high pulse repetition rate.
- (d) Decoders have been developed which have a settling time of less than  $10\text{ns}$  and which are compatible with ECL. In general the static accuracy is satisfactory for 8-bit resolution although drift was observed in the 4-bit decoder due to the relatively high power dissipation and discrete component construction. Also the problem of component spreads is considered in some detail.

8-bit video decoder



8-bit PWM video encoder



## CHAPTER 4: CODEC PERFORMANCE

This chapter describes aspects of the encoder alignment and the performance of the complete codec on monochrome and colour television signals. Unless otherwise stated, the signals are bandlimited to 5MHz at the codec input and output and no dither is used.

### 4.0 ENCODER ALIGNMENT

This involved two distinct stages; the alignment of the timing system and the alignment of the encoder preset controls. The timing system was aligned using a sampling oscilloscope (rise time 200ps) and a measured system that proved satisfactory is shown in Fig. 4.1. If the timing deviates too far from the theoretical system then an error occurs which usually results

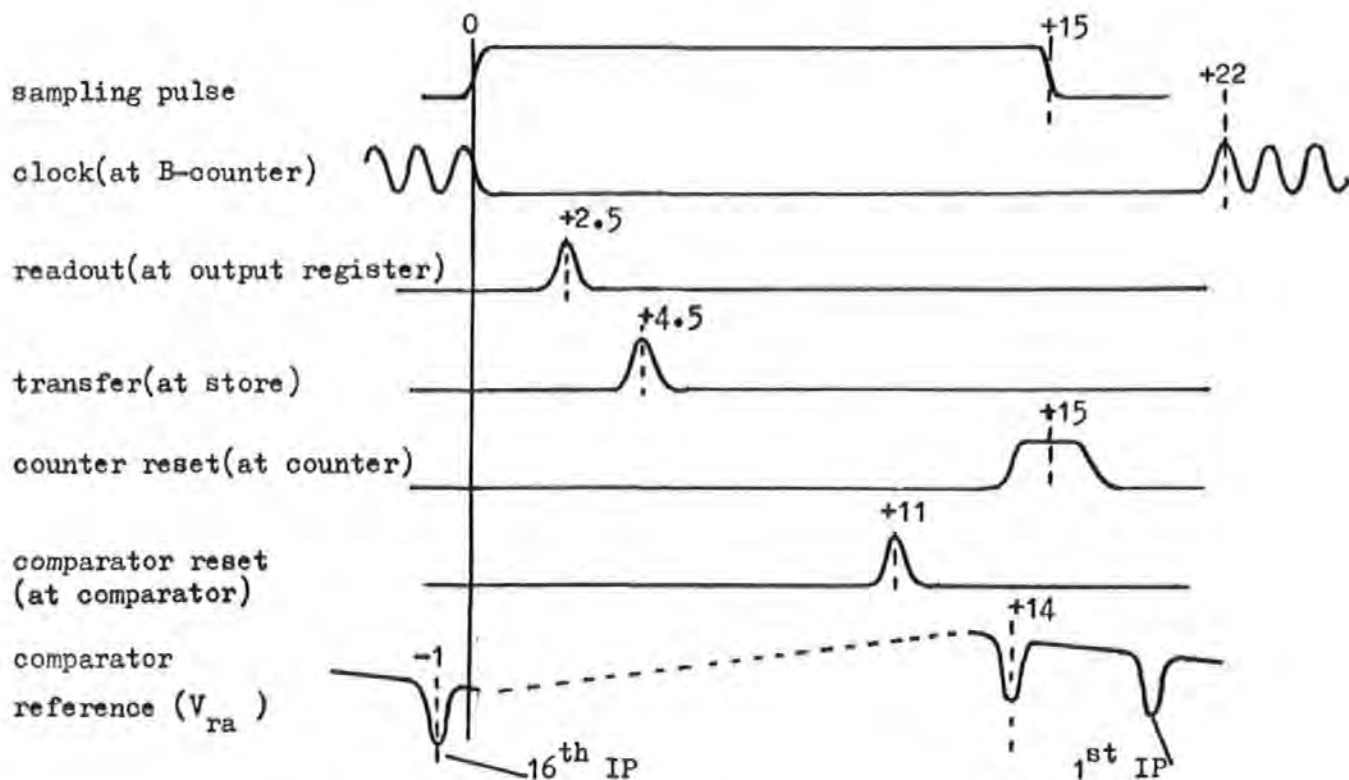
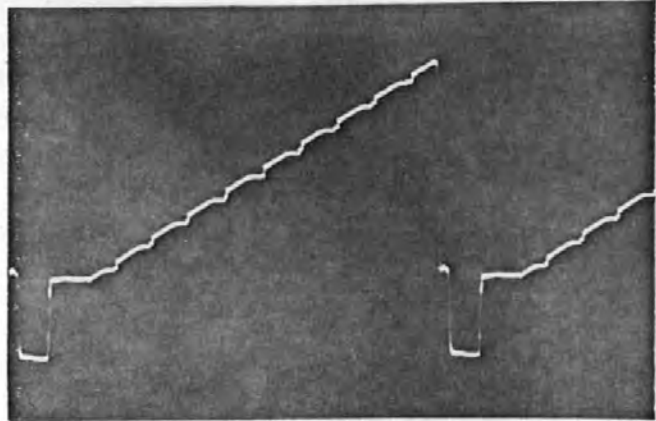
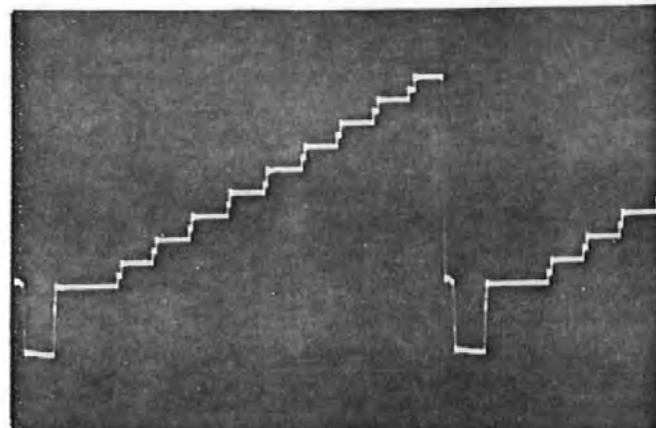


Fig. 4.1: relative timing for working codec  
(sampling locked to subcarrier, relative timing in ns)

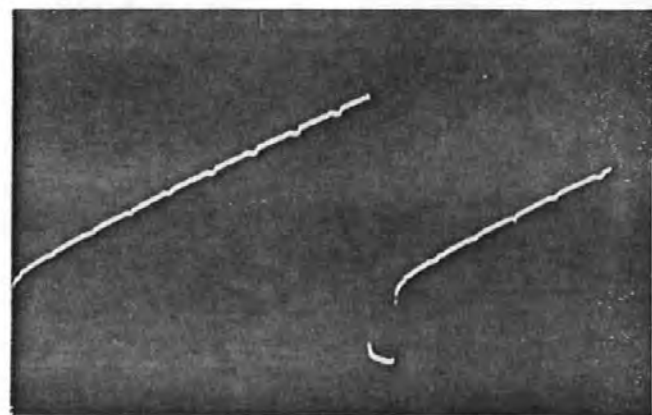
(a) small offset in the B-ramp  
reference (Fig.3.38)



(b) large offset in the B-ramp  
reference (Fig.3.38)



(c) incorrect quantizer gain (Fig.3.38)  
(simple ramp input to encoder)



(d) incorrect B-ramp amplitude (Fig.3.26)  
(simple ramp input to encoder)

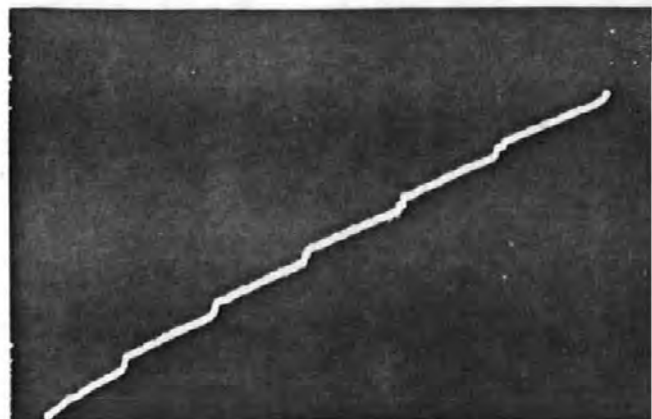


Fig. 4.2: illustrating the effect of encoder malalignment on the  
filtered codec output.



in an unstable system, or complete loss of output or severe coding error. For example, if the comparator reset pulse is advanced too far ( $< +10.2\text{ns}$  approximately) then an interrogation pulse on the rising part of the ramp reference waveform re-triggers the comparator and results in a constant digital output (00000000). On the other hand, if the inhibit pulse duration is in error by several nanoseconds then 16 clock pulses could be gated to the B-counter thereby resetting the counter. If a ramp signal is being encoded this results in a notch or 'glitch' in the decoded ramp and the glitch has an amplitude of  $16q$ . Both of these errors were observed during alignment.

In general the timing adjustments are critical although they could be simplified by incorporating preset controls into the S.R.D. circuits. Also, stabilized power supplies are essential for a stable and repeatable timing system since supply variation affects the charge stored in each S.R.D. - typically a  $\pm 5\%$  supply variation gives  $\pm 1\text{ns}$  timing variation between certain pulses.

Errors arising from malalignment of the encoder preset controls are apparent if a ramp signal is encoded and this is illustrated in Fig. 4.2. Figs. 4.2(a)(b) show the effect of malalignment in the B-ramp reference control upon an encoded, decoded and filtered 625-line composite ramp signal and Figs. 4.2(c)(d) illustrate the effect of incorrect quantizer gain and incorrect B-ramp amplitude respectively (the ramp used in the latter illustrations is a simple, unblanked ramp at approximately 625-line frequency). Note that malalignment generally results in locked code characters and this leads to missed code characters. The above results are simply qualitative examples of the type of errors involved and they are difficult to predict without resort to numerical analysis. The numerical analysis in chapter 6 shows for instance that, contrary to first impressions, there must be other, smaller errors present in Figs. 4.2(a)(d) since the



Fig.4.3(a):unblanked ramp:  
upper trace,filtered codec output  
lower trace,codec input

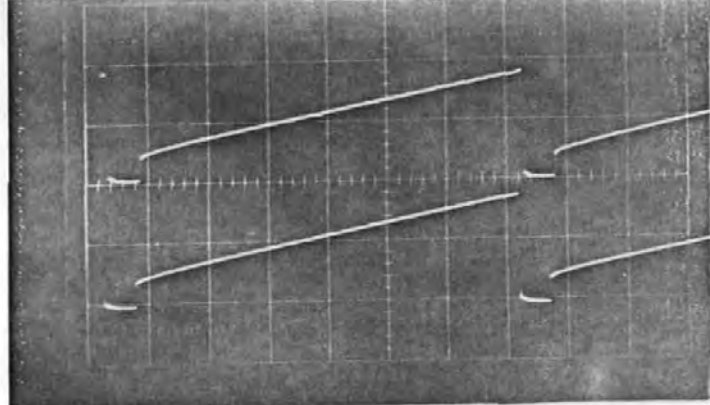


Fig.4.3(b):filtered codec output  
(625-line composite ramp)

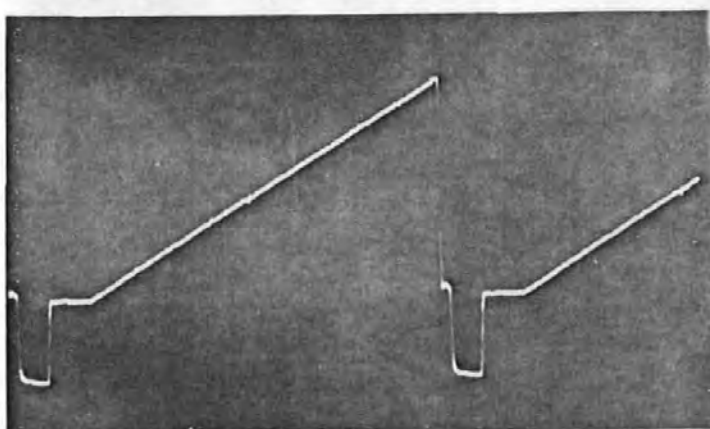


Fig.4.3(c):unfiltered codec output  
(unblanked ramp)

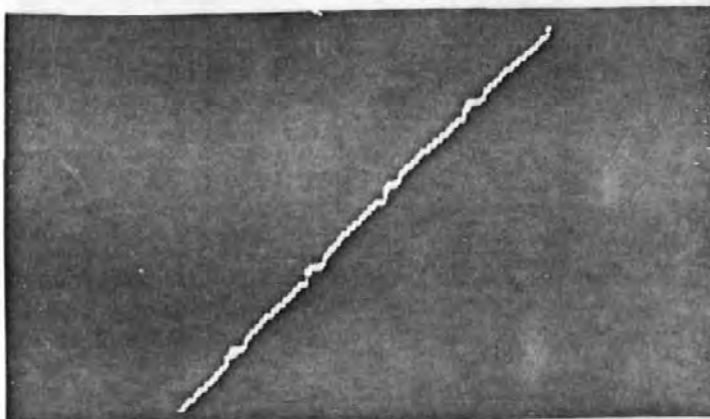


Fig.4.4:filtered codec output  
(the maximum errors correspond  
to 6-bit quantizing steps)

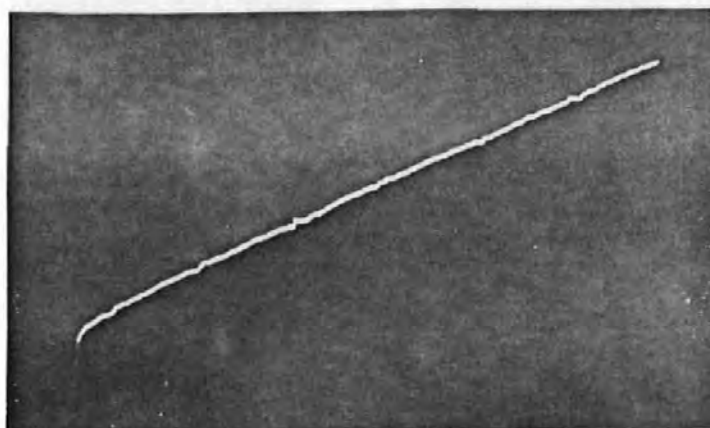
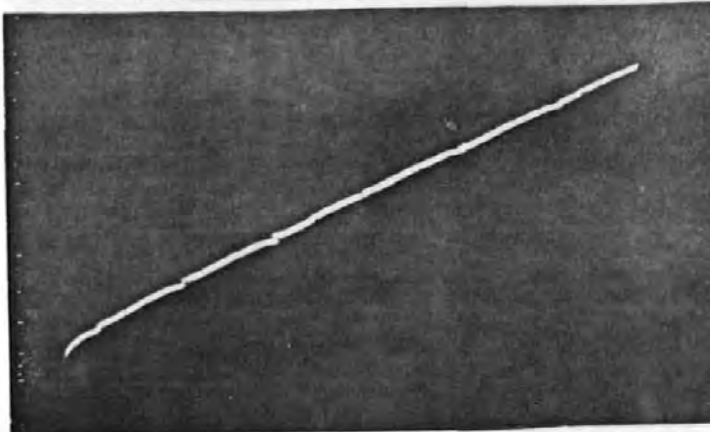


Fig.4.5:the effect of adding white  
noise to the codec input signal,  
 $SNR = 45dB$



exact shape of these waveforms could not be predicted solely by introducing a single error into the numerical analysis. However, the general shapes and trends are characteristic of malalignment in the particular encoder controls cited. Finally, an important practical factor is ease of alignment and using the above approach it is found that alignment of all encoder preset controls takes only a few minutes.

#### 4.1 MONOCHROME PERFORMANCE

The performance of the aligned codeo is illustrated in Fig. 4.3: Fig. 4.3(a) shows the simple unblanked ramp and Fig. 4.3(b) shows the conventional 625-line composite ramp. These figures show that the codeo is mostly monotonic (i.e. the slope of the transfer function is mostly positive) but there are still some missed code characters and perfect 8-bit coding cannot be achieved. The errors are shown in greater detail in Fig. 4.3(c) and they are attributed to the encoder since the decoder alignment is well within acceptable limits. The smallest steps correspond to 8-bit quantization but they are regularly interrupted by errors approximately equivalent to 7-bit or occasionally 6-bit quantization. These larger errors correspond to a change in one of the four MSB's and they tend to be more significant for the larger changes in the digital word e.g. at 01000000, 10000000, and 11000000.

It is well known that 6 and 7-bit quantizing error will be visible on a picture monitor if dither is not employed. On the other hand, DEVEREUX<sup>31</sup> has shown experimentally that for an n-bit code the effects of quantizing error can be virtually eliminated by white Gaussian noise at the codeo input if the input SNR is

$$SNR \lesssim 6n + 5 \text{ dB} \quad (4.1)$$

Here the SNR is expressed as peak luminance to rms noise and it is assumed that

100/0/100/0 colour bars would just fill the quantizing range. As an example, the typical unweighted SNR for continuous random noise at the output of a plumbicon camera channel is 45dB so that this is sufficient to eliminate any 7-bit quantizing error. Extending these results to the residual coding errors in Fig. 4.3 we conclude that a 45dB SNR should virtually eliminate many of these errors. This was verified by adding white Gaussian noise, bandlimited to 5MHz, to the ramp input signal and the improvement can be seen by comparing Figs. 4.4 and 4.5.

Spectral analysis of the unfiltered coded output for a bandlimited ramp input (Fig. 4.6(a)) is of interest since it highlights a problem peculiar to the encoding system. Assume for example that there is some asymmetry between the dual analog channels, such as a difference in clamp levels. As far as the quantizer is concerned the sampler appears to be non-ideal such that even for a constant analog input (between syno pulses) the sampler outputs a rectangular wave of periodicity  $\frac{4\pi}{\omega_s}$  (see Fig. 4.6(b)). Alternatively, the same wave will be obtained if a small  $\omega_s/2$  component is applied to the input of an ideal sampler and this model is useful in explaining the generation of unwanted, inband components when encoding PAL colour signals (section 4.2). In either case, the output of the quantizer clearly contains harmonics of  $\omega_s/2$  and in practice these could be observed up to 50MHz. For monochrome signals a clamp differential is not necessarily detrimental and, in theory if the amplitude of the rectangular wave is  $q/2$  the number of quantizing levels is effectively doubled for slowly changing signals<sup>31</sup>. In practice however other forms of asymmetry, such as gain differential and unequal adjacent sampling periods adversely affected the amplitude of the  $\omega_s/2$  component and the above dither effect would be difficult to achieve.

Missed code characters and clamp level differential effects can be described as static errors since they occur even for a static analog input.

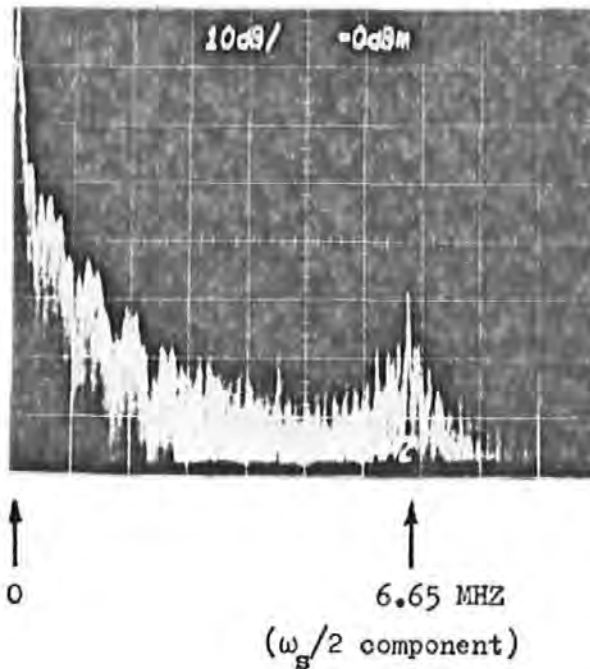


Fig. 4.6(a): Unfiltered codec output spectrum for ramp input.

Scales: 10dB/div, 1MHz/div.

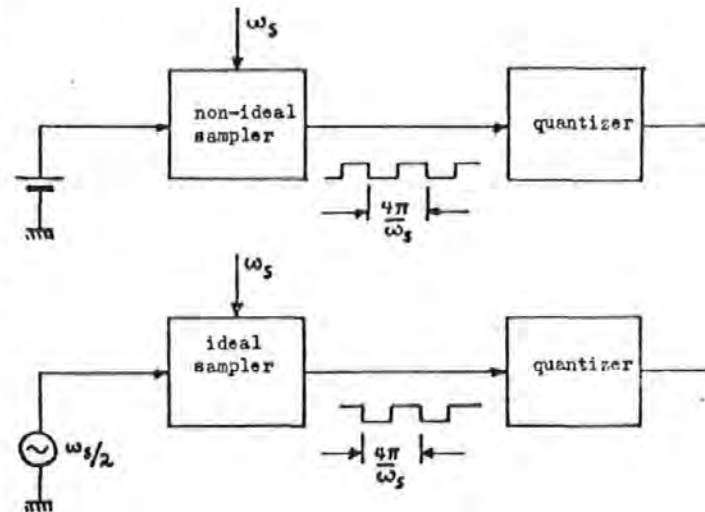
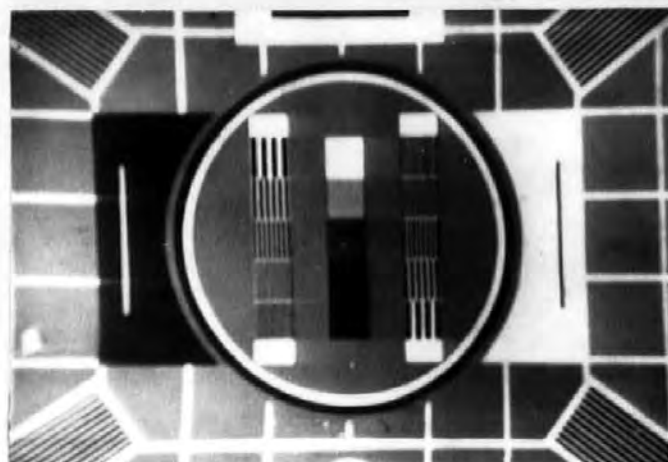


Fig. 4.6(b): Equivalent models for a clamp differential between analog channels.

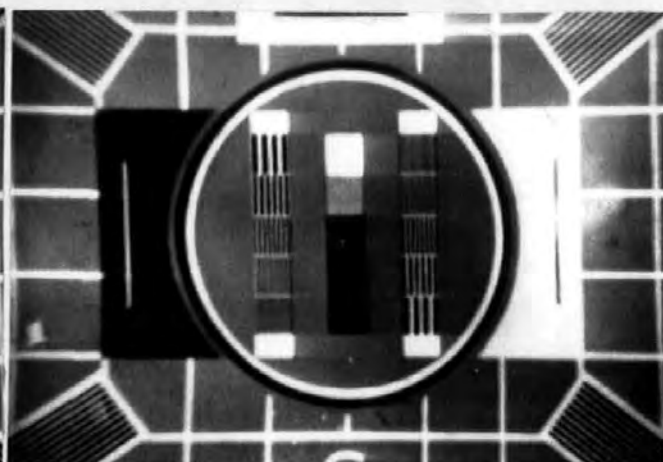
Dynamic errors were detected by making 2T pulse and bar measurements and these revealed significant hf loss even after allowing for the  $Sa(x)$  loss in the decoder. On the other hand, the performance on 625-line monochrome signals generated by a vidicon camera is still encouraging and examples of these pictures are given in Figs. 4.7 and 4.8. No strict quality assessment<sup>1</sup> was carried out but the non-expert observer generally assessed the pictures as acceptable whilst the expert observer detected hf loss on high detail pictures and slight contouring on some low detail pictures.

## 4.2 COLOUR PERFORMANCE

The codec performance on PAL colour signals was examined using EBU colour bars and the corresponding time and frequency domain measurements are



(a) codec input



(b) filtered codec output

Fig. 4.7: test card (frequency gratings correspond to 1.55, 2.42, 3.10, 3.88, and 4.66 MHz)



(a) codec input



(b) filtered codec output

(c) filtered codec output showing reduced resolution due to malalignment of D-ramp reference, see Fig.4.2(b)



Fig. 4.8: girl

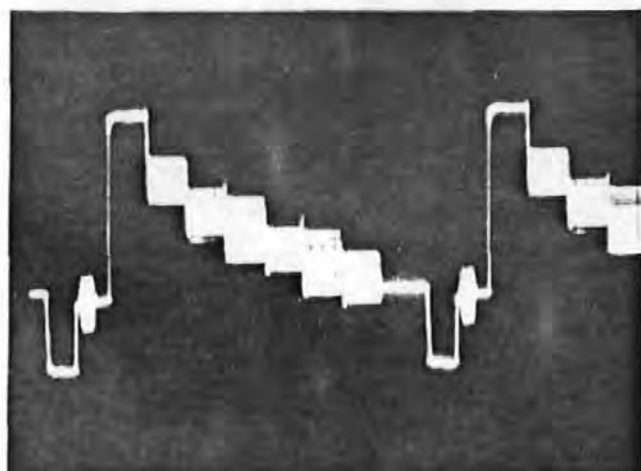
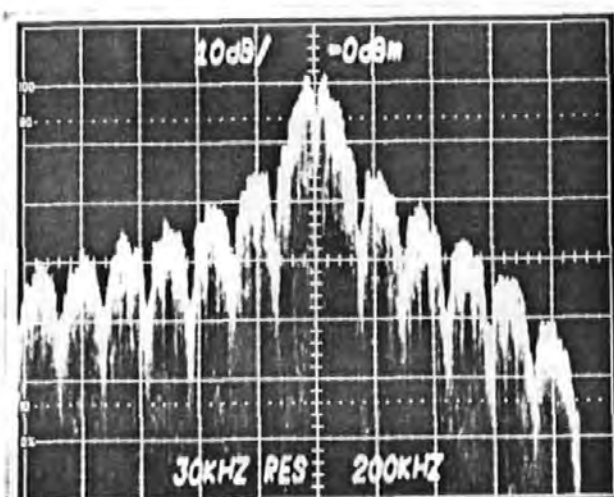
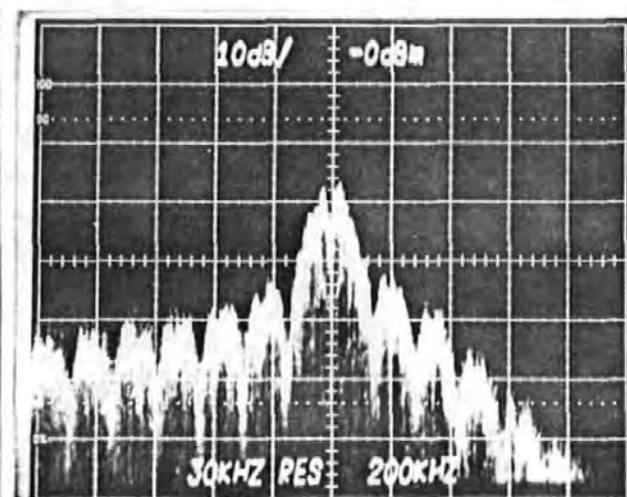


Fig. 4.9: decoded and filtered EBU colour bars (5.5MHz output filter and sampling locked to subcarrier)



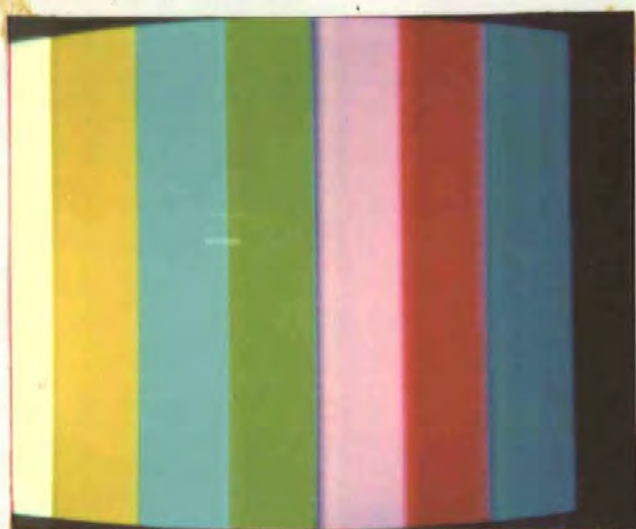
(a) codec input  
(bandlimited to 5MHz)



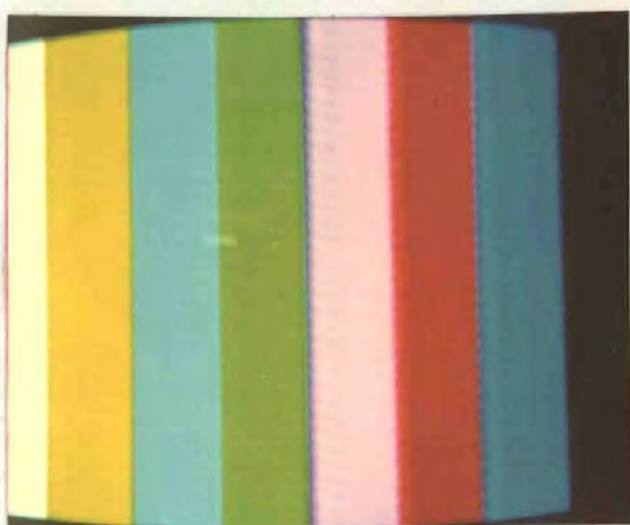
(b) filtered codec output  
(5MHz output filter and sampling locked to subcarrier)

Fig. 4.10: spectra of EBU colour bars over chrominance band  
(10dB/div., 200KHZ/div.)





(a) codec input



(b) filtered codec output,  
showing patterning



(c) filtered codec output showing patterning in more detail  
(the diagonal band is a camera aperture time effect)

Fig. 4.11: EBU colour bars(sampling locked to subcarrier)





shown in Figs. 4.9 and 4.10. As expected the results exhibit hf loss (chrominance-luminance gain inequality) as observed for monochrome signals but close examination of the colour display Fig. 4.11 also shows a patterning effect. Since sampling is locked to subcarrier then this is not the effect of quantization noise associated with a quantized subcarrier signal - this would in any case appear as a l.f. beat pattern as discussed in section 1.2. Instead, the patterning is due to a half subcarrier frequency component or subharmonic of subcarrier as shown in Fig. 4.12 and the generation of such a component can be explained by the model in Fig. 4.13. Assuming that the asymmetry between

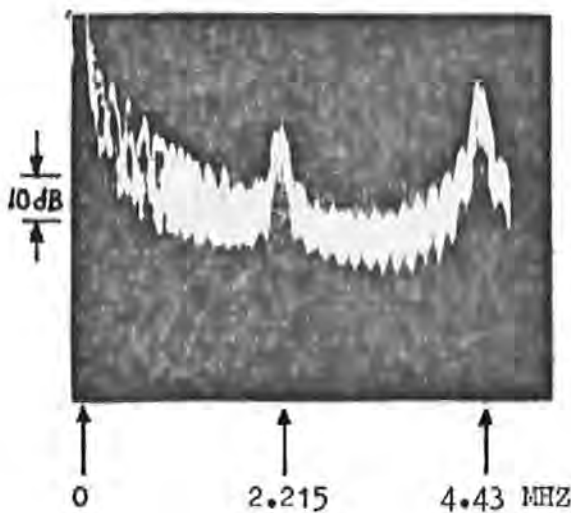


Fig. 4.12: Spectrum of coded, decoded and filtered EBU colour bar signal.

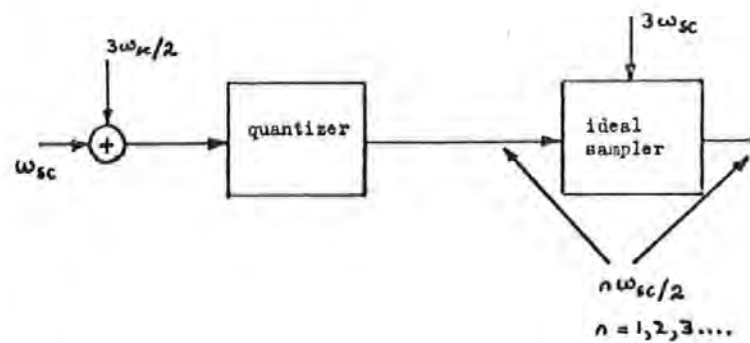


Fig. 4.13: Model for generation of the  $\omega_{sc}/2$  component

analog channels can be represented by a  $3\omega_{sc}/2$  component at the codec input then the non-linear quantizing process together with the sampling process gives rise to a  $\omega_{sc}/2$  component at the codec output. Clearly, removal of the subcarrier,  $\omega_{sc}$ , would remove the subharmonic and this was observed in practice. Also, any circuit changes adversely affecting the symmetry of the two channels would adversely affect the subharmonic amplitude. In practice for instance the subharmonic

amplitude increases for a change in the timing of the two sampling pulses such that adjacent sampling intervals are unequal and the amplitude can also be changed a few decibels by adjusting the gain balance control. Also, the amplitude goes through 4dB cycles as the video reference is varied. Finally, white noise was added at the codec input in an attempt to dither out any asymmetry between channels but this was only marginally successful; the subharmonic amplitude decreases by only 4dB relative to the chrominance components for a 20dB reduction in the input SNR.

Having established the identity of the patterning in Fig. 4.11 the diagonal structure of the pattern is easily explained. For a signal at half subcarrier frequency there is an odd  $1/8^{\text{th}}$  cycle of this component left each line (neglecting the 12.5HZ) so that on passing through the luminance channel of the monitor it is displayed as a diagonal luminance pattern. The mechanism is very similar to that for the conventional dot pattern.

#### 4.3 SUMMARY

The codec performance is encouraging and non-expert observers judge most 625-line monochrome pictures passed through the codec as satisfactory. Since the codec is a prototype some circuit deficiencies are to be expected and in particular, slight asymmetry between the two analog channels appears to be causing patterning on colour pictures. Circuit improvements must therefore be made to reduce the asymmetry and improvements must also be made to ease timing adjustments and to reduce the number of missed code characters. The following chapters are concerned with the type and magnitude of the circuit improvements required and a general circuit design criterion is developed.

## CHAPTER 5: NUMERICAL ERROR ANALYSIS

The experimental work has highlighted the need for reducing circuit errors and so a detailed error analysis is required. We must determine how much improvement is required and where it is required and this implies that some upper bound must be placed upon the impairment of the codec output signal. If a meaningful upper bound can be defined then it is conceivable that bounds can also be defined for circuit errors and it should be possible to formulate a general circuit design criterion for a P.W.M. video encoder.

### 5.0 CODEC ERRORS

The codec can be broadly divided into an analog section and a digital section and we can assign errors to each section. Two examples of analog errors are discrepancies in gain and clamp level between the two analog channels. Malalignment, such as error in ramp amplitude or mean level, and ramp nonlinearity can also be described as analog errors since they arise from analog rather than digital circuits. Digital errors are those errors arising from the digital section and in this we can include quantizing error, binary weighting error in the 4-bit decoder and pulse timing error. Each of the above errors will cause the output of the codec to differ from the ideal output - and here the ideal output must be taken as that from a codec with infinite resolution ( $n \rightarrow \infty$ ) in order to define quantizing error. Furthermore, this difference would be observed even for a static analog input and so the above errors will be referred to as 'static' errors as illustrated in Fig. 5.1. In contrast, aperture errors, aliasing and  $S_a(x)$  error in the 8-bit decoder are all very clearly dependent upon the rate of change of the codec input signal and so will be termed 'dynamic' errors.

Parasitic elements can give rise to both dynamic and static error;

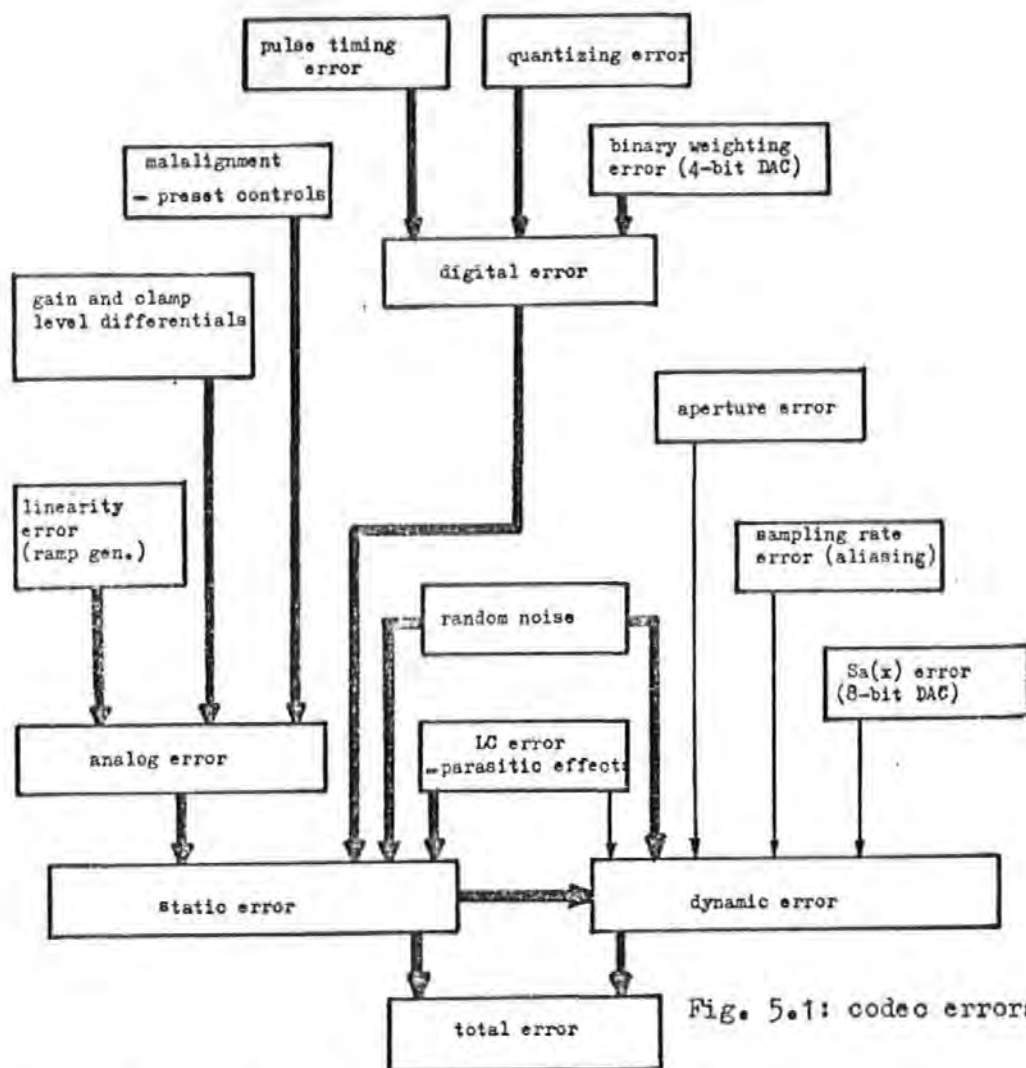


Fig. 5.1: codec errors

dynamic error occurs because they affect the analog circuits and static error occurs because they affect transient settling times (e.g. damped oscillation on each ramp) and so may result in missed codes. On the other hand, random noise may actually reduce static and dynamic error if it is applied as a dither signal at the codec input.

The analysis is primarily concerned with the assessment of errors which are peculiar to the encoding system and so any errors in the 8-bit decoder are ignored together with aperture error and sampling rate error. Also,  $Sa(x)$  error is implicit in some aspects of the analysis but otherwise is neglected. Quantizing error however is a useful criterion by which to compare other errors and so it is included in the analysis. The errors considered are denoted by broad interconnections in Fig. 5.1 and it will be noted that although some causes of dynamic error are neglected, a major source

of dynamic error is in fact static error - or rather the factors leading to it. Static linearity error for example will lead to phase and gain error when colour subcarrier is passed through the codec and since these errors are associated with a h.f. signal they will be referred to as dynamic errors.

### 5.1.0 CODEC SIMULATION

A main objective of the error analysis is to formulate some encoder design criterion and a convenient way of doing this is to examine the distribution law of the codec output error (where the term 'error' is to be interpreted in a general sense for the time being). The problem is therefore to determine the distribution law and this can be attempted analytically or numerically.

KHANTTEL<sup>87</sup> adopted an analytical approach and commenced by considering a system of random variables. He assumed that the (randomly varying) encoder conversion error  $y$  depends upon the (randomly varying) input signal  $x$  so that  $p(y)$  can be derived from a joint probability

$$p(y) = \int_{-\infty}^{\infty} p(x, y) dx = \int_{-\infty}^{\infty} p(x) p(y|x) dx$$

To evaluate  $p(y)$ , KHANTTEL made further assumptions such as

$$p(x) = \begin{cases} (x_{\max} - x_{\min})^{-1} & x_{\min} \leq x \leq x_{\max} \\ 0 & x_{\max} < x < x_{\min} \end{cases}$$

and

$$p(y|x) = \frac{1}{\sqrt{2\pi} \sigma} e^{-y^2/2\sigma^2}$$

where

$$\sigma = (ax + b)/3$$

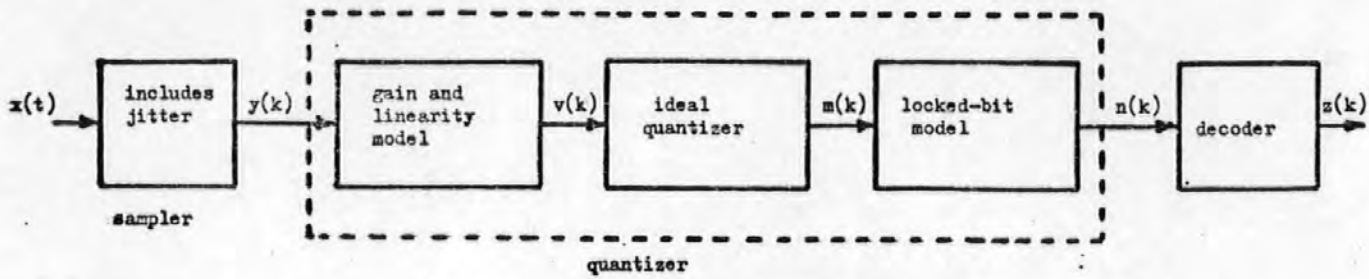


Fig. 5.2: codec model used by CALLAS<sup>89</sup>

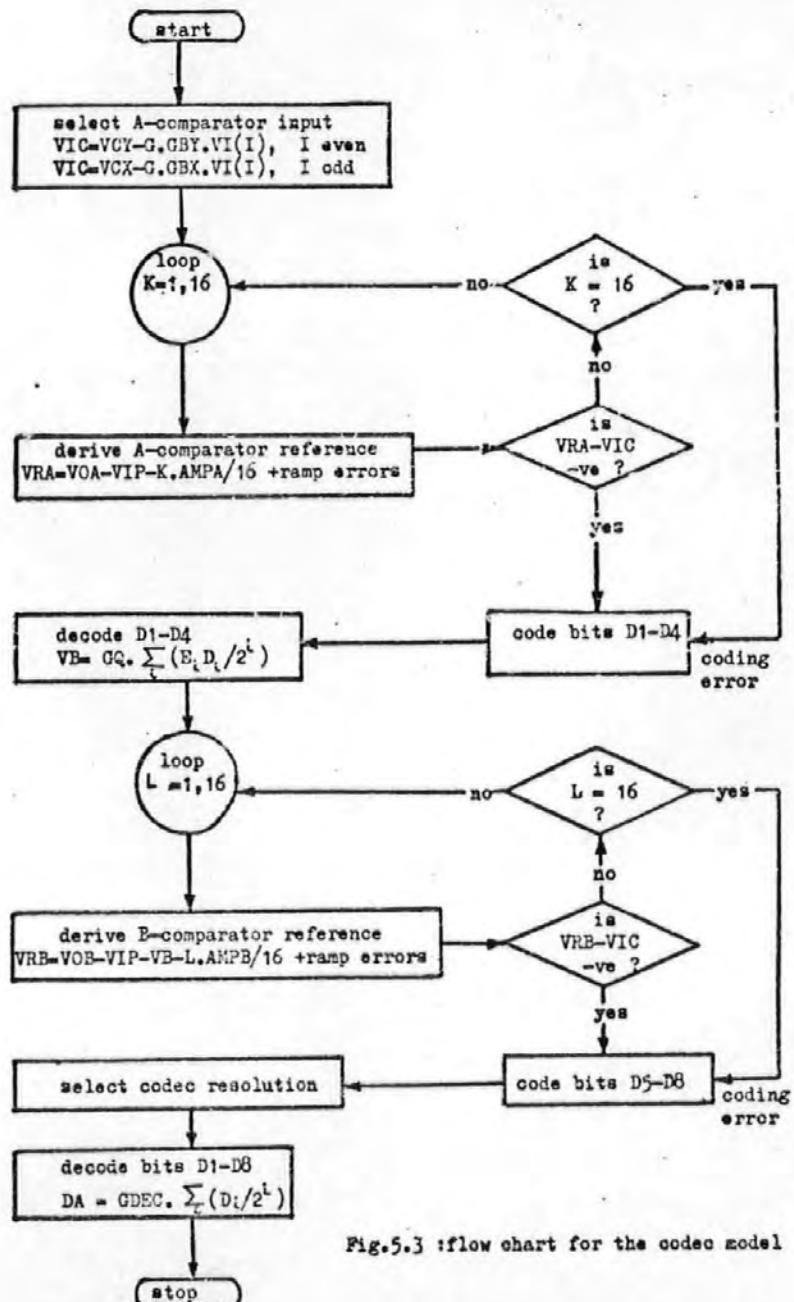


Fig.5.3 :flow chart for the codec model



$b$  = the zero error

$a$  = the relative error  $(0 \leq a \leq 1)$

The distribution  $p(y)$  is for static error i.e. for a constant but random input  $x$  and KHANTEL goes on to consider ways of determining the distribution of the dynamic error. His expressions for both static and dynamic error are complex and are based upon assumptions which are given little or no justification. They also refer to random input signals whereas for a video encoder it is considered more meaningful to evaluate a distribution law for one of the video test parameters such as differential phase and gain, chrominance-luminance crosstalk or line time nonlinearity. This is because tolerances for these parameters are defined for video equipment<sup>3,38</sup> and it means that the encoder input signal is defined rather than random. Besides its complexity, KHANTEL's approach is therefore felt to be rather abstract from the problem in hand and so a numerical solution for the distribution law was adopted by using a codec simulation.

SCHREIBER<sup>6</sup> describes the ideal simulation in which at least 100 pictures are processed by the software model of the codec and stored ready for fast readout so as to give a few seconds of moving picture. In this way the effect of simulated codec error can be readily observed but it has the disadvantage that a very high storage capacity is required, typically  $10^8$  bits. A less ambitious approach but one more akin to the determination of the output error distribution is described in the paper by TARNAY<sup>88</sup> and later in a paper by CALLAS<sup>89</sup>. TARNAY developed algorithms which simulated the codec and a number of programs were written around this basic mathematical model to find such parameters as differential nonlinearity and the codec output spectrum. The codec simulation used by CALLAS is illustrated in Fig. 5.2. Referring to this figure,  $x(t)$  is modelled as a sinewave and random jitter on the sampling pulses is modelled by expressing the sampled signal as

$$y(k) = x([k + \sigma u(k)]t_s) \quad k = 1, 2, \dots, N$$

where  $u(k)$  are samples of the normalized (unit variance) distribution which best represents jitter and  $\sigma^2$  is the variance (CALLAS assumes a uniform distribution for  $u(k)$ ). Encoder imperfections give unequal quantum intervals and this results in linearity error (a static error). If  $v(k)$  falls in the  $i^{\text{th}}$  quantum interval then the linearity error can be modelled using a linear quantizer of interval  $q$  providing it is preceded by a nonlinear amplifier of gain  $h[v(k)]$  such that

$$iq \leq v(k) h[v(k)] < (i+1)q$$

The locked bit model simulates the condition in which the digital output remains locked whilst the true output may differ from the actual output. CALLAS defines the  $k^{\text{th}}$  sample of the error signal from the codec as

$$e(k) = x(kt_s) - z(k)$$

and proceeds to find the power spectrum of  $e(k)$  by Fourier transform. Encoder errors are then identified by examining the power spectrum and comparing it with a predetermined table of spectra for different types and magnitude of encoder error.

CALLAS's power spectrum approach to the evaluation of dynamic codec errors is quite fundamental (see BENNETT<sup>10</sup>) in that errors can be related to the intrinsic codec error  $q^2/12$  but, like the work of KHANTEL, it is difficult to relate the results to the familiar video test parameters previously mentioned. A somewhat different approach is therefore required although the type of analysis adopted combines some aspects of the work discussed above i.e. a codec model is developed using simple algorithms to define the error sources and the model is incorporated into several analysis

programs, one of which is used to evaluate the distribution law for the codec output error.

### 5.1.1 THE CODEC MODEL

Fig. 5.3 shows a simplified flow chart of the model and the FORTRAN IV program is given in appendix 4. After repeated modification the model is thought to embrace all the major static errors of the encoder.

Array VI contains the input data and represents the codec input signal sampled at exactly 3 times subcarrier frequency; in the case of one analysis program array VI represents 853 samples of a composite 625-line ramp and for other programs it represents samples of subcarrier. The  $I^{\text{th}}$  sample is then applied to the A-comparator via one of the two analog channels according to the algorithm

$$VIC(I) = VCY(X) - G \cdot GBY(X) \cdot VI(I) \quad , I \text{ even } (I \text{ odd})$$

where  $VCY(X)$  represents the sync tip clamp levels and  $GBY(X)$  denotes the relative channel gains ( $GBX$  is usually held constant at 0.95 and  $GBY$  is allowed to deviate about 0.95). The video pre-amplifier gain  $G$  is usually set to ensure that the input signal just fills the quantizing range. The reference input to the A-comparator can be expressed as

$$VRA(k) = VOA - VIP - \left(\frac{k}{16}\right) AMPA \quad , k=1, 2 \dots 16$$

where  $VOA$  represents the A-ramp reference and  $VIP$  represents the interrogation pulses superimposed upon the ramp (since the quantizing range is +3V to +6V then ideally  $VOA - VIP = +6V$  and the ramp amplitude  $AMPA = +3V$ ). As mentioned in section 3.3.3, there is a possibility of slight damped oscillation at the start of the ramp and also slight ramp non-linearity and these can be modelled by modifying the above algorithm i.e.

$$VRA(K) = VOA - VIP - \left(\frac{K}{16}\right) AMPA + OSCA \sinh(\omega t(K)) e^{-\frac{t(K)}{4\tau_c}} + AMPA \cdot RAMPE(K) \quad ,$$

$$K = 1, 2, \dots, 16$$

The oscillation frequency is typically 500MHZ and the oscillation amplitude (typically 1q) is programmed to decay by an order in  $t_s/2$ . Ramp nonlinearity is modelled by the variable  $RAMPE(K)$ . The nonlinearity is most apparent at the start of the ramp so that  $RAMPE$  increases for  $K \leq 3$  and linearly decreases for  $K > 3$ . In practice the nonlinearity (measured as the maximum deviation from a straight line drawn between two fixed end points) is of the order of 1% of the ramp amplitude.

The binary action of the comparator is defined by the inequality

$$VRA(K) < VIC(I)$$

If this is true the comparator is said to have triggered and the value of  $K$  is used in a computed GOTO statement to determine the corresponding 4 MSB's. Should  $K = 16$  and  $VRA(K) > VIC(I)$  then D1 to D4 are set to 1 - signifying the situation in which the A-counter reaches full count but the A-comparator remains untriggered. This may arise simply because the sample is outside the quantizing range but more generally it denotes a static coding error.

At this point the actual encoder applies the next sample to the A-comparator but in the program it is more convenient to code one sample fully to 8-bits before starting to code the next sample. The next step is therefore to decode the 4 MSB's and the decoder output for the  $I^{th}$  sample is

$$VB(I) = GQ \sum_{i=1}^4 E_i D_i / 2^i$$

Coefficients  $E_i$  (ideally unity) account for the binary weighting errors and the variable  $GQ$  denotes the quantizer 'gain' (ideally +3V). For a particular bit the percentage error in the decoder output voltage is approximately equal to

the percentage error in the weighted current so that only the first two coefficients  $E_1$  and  $E_2$  are of any significance.

Note that the perfection of each sample and hold gate is implicit in the model by defining each sample  $VI(I)$  as a point exactly on the analog input signal and by using the same sample throughout the two coding intervals. In other words, each gate accurately follows the analog input (zero acquisition and zero aperture error) and no capacitor charge transfer occurs during the hold periods (zero hold error). Note also that the simulated comparators have (virtually) infinite resolution since the binary decision is achieved via digital arithmetic.

To summarize, the simulated static errors are as follows:

1. error in mean level of A-ramp
2. error in mean level of B-ramp
3. error in A-ramp amplitude
4. error in B-ramp amplitude
5. video reference (or clamp level) error
6. clamp level differential between analog channels
7. gain differential between analog channels
8. linearity and transient errors on each ramp
9. binary weighting errors in 4-bit decoder
10. gain error in 4-bit decoder
11. quantizing error

Two other effects can be modelled by suitably modifying the input samples  $VI(I)$ . One effect, which will be termed 'sampling time offset', refers to possible irregularity in the sampling period. This could arise since the sampling pulses to the two sample gates are generated independently so that two adjacent sample periods need not be identical (the measured error was about

lms). To model the effect upon a PAL signal corresponding to a large, uniform area of colour the input samples (taken at exactly  $3\omega_{so}$ ) can be written as

$$V_I(I) = V_0 + V \sin \left[ \phi_s + k \phi_e + (I-1) \frac{2\pi}{3} \right]$$

$$\begin{aligned} I &= 1, 2, \dots, N \\ k &= 0, I \text{ odd} \\ k &= 1, I \text{ even} \end{aligned}$$

where  $\phi_s$  is the sampling phase,  $\phi_e$  corresponds to the sampling time offset ( $\phi_e/\omega_{so}$ ) and  $V_0$  is the luminance level. Similarly, codec input noise can be simulated by adding a noise component to each array element and a suitable algorithm for white Gaussian noise is discussed below.

## 5.2 NOISE SIMULATION

Random noise has a marked effect upon the performance of an encoder. On the one hand it can be considered as a source of coding error (GORDON<sup>92</sup>) and in general terms this means loss of resolution and so limited accuracy<sup>85</sup> of the encoder. The finite comparator resolution discussed in section 3.3.3 for example has been attributed to random noise generated in the encoder itself. On the other hand, random noise added to the signal at the codec input can be regarded as an error reducing mechanism<sup>4,31,66</sup> and it is in this context that the effect of noise will be discussed.

Any signal bandlimited to  $\omega_0$  can be expressed as

$$n(t) = \sum_{n=-\infty}^{\infty} f_n \operatorname{Sa} \left[ \omega_c \left( t - \frac{n\pi}{\omega_c} \right) \right] \quad (5.1)$$

where  $f_n$  is the value of  $n(t)$  at times  $t = n\pi/\omega_0$ . If the signal is white Gaussian noise then the  $f_n$  will be samples from a Gaussian distribution. Now, the autocorrelation function of  $n(t)$  is

$$R_{xx}(\tau) = \overline{n(t) \cdot n(t-\tau)}$$

and for bandlimited white Gaussian noise this can be shown to be<sup>82</sup>

$$R_{xx}(\tau) = \overline{n^2(t)} S_n(\omega_c \tau) \quad (5.2)$$

Consideration of either eqn. (5.1) or (5.2) shows that samples of  $n(t)$  taken at the Nyquist rate will be completely uncorrelated.

It follows that if bandlimited white Gaussian noise is sampled by the codec at the Nyquist rate then the samples can be accurately simulated by generating random numbers which have a Gaussian probability distribution and adding them to the array elements  $VI(I)$ . Brief details of the Gaussian number generation are given below.

A stream of uniformly distributed (pseudo) random numbers  $x_i$  in the range 0-1 are first generated, usually by a residue method<sup>94</sup>. If  $k$  of these numbers are now summed ( $k \rightarrow \infty$ ) they will, from the central limit theorem, be normally distributed with mean  $k/2$  and variance  $k/12$ . A value of the Gaussian variable  $E_n$  which has zero mean is therefore

$$e_n = \sum_{i=1}^k (x_i) - k/2$$

According to HAMMING<sup>5</sup>,  $E_n$  is very nearly Gaussian for  $k$  as low as 10, and choosing  $k = 12$  gives  $E_n$  unit standard deviation. For continuous random noise the SNR at the codec input is defined as the ratio peak luminance (0.7V) to rms noise  $\sigma_n$  so a value  $e_n$  of the Gaussian noise voltage at the codec input can be closely approximated by

$$e_n = \sigma_n \left( \sum_{i=1}^{12} (x_i) - 6 \right)$$

This additive noise is on a mean value represented by the noiseless analog input so that each array element is of the form

$$VI(I) = \sigma_n \left( \sum_{i=1}^{12} (x_i) - 6 \right) + VI0(I) \quad (5.3)$$



where  $VIO(I)$  is the value of the noiseless codec input at the sample instant. The same algorithm is used to evaluate the distribution law for dynamic error (section 6.1).

### 5.3 OUTPUT FILTER SIMULATION

The analysis programs in chapter 6 code and decode each input sample  $VI(I)$  and store the result in an output array,  $VO$ . Taken in sequence these samples represent the unfiltered codec output in the time domain and they are used directly when investigating static errors (section 6.0). On the other hand, to assess dynamic error it is usual to apply a sinusoidal test signal and to examine the spectrum of the codec output (BENNETT<sup>10</sup>, CALLAS<sup>89</sup>, SMITH<sup>93</sup>, CONNOLLY<sup>96</sup>); in this application the test signal is colour subcarrier and the dynamic error is the amplitude and phase error exhibited by the output subcarrier. The filtering process required to extract the subcarrier can be achieved either numerically or by appropriate algorithms, depending upon the complexity of the codec output spectrum.

Consider a subcarrier signal (noise-free and at a constant luminance level) applied to the codec input and assume that the codec errors do not generate a subharmonic of subcarrier (section 4.2). Codec nonlinearity i.e. quantizing error and encoder errors will generate harmonics  $n\omega_{sc}$ ,  $n = 1, 2, 3, \dots$  and if sampling is at  $3\omega_{sc}$  all harmonics will be folded back into the baseband, falling either at 0 or  $\pm \omega_{sc}$ . In this case, if the codec is followed by a lowpass filter of cut-off frequency  $3\omega_{sc}/2$  the filtered codec output is simply

$$e(t) = e_0 + e_1 \sin(\omega_{sc} t + \phi)$$

where  $e_0$ ,  $e_1$  and  $\phi$  are functions of codec nonlinearity. Now assume that this system is simulated using a simulated subcarrier input, the codec model and

an appropriate filter. The filter can be realised by applying SHANNON's<sup>83</sup> classic interpolation

$$e(t) = \sum_{I=1}^N \left[ v_0(I) \text{Sa}(3\omega_{sc}(t - It_s)/2) \right] \quad (5.4)$$

Dynamic error could be investigated by varying the subcarrier luminance level and observing any change in amplitude and phase of the subcarrier (these parameters could be found by searching for the maximum and minimum of  $e(t)$  and this is done near the centre of the range ( $I \approx N/2$ ) in order to minimise end effects).

This numerical approach is tedious and subject to end effects and fortunately suitable algorithms can be derived since the codec output spectrum is relatively simple. Under the assumptions of a noise-free sinusoidal output and an output filter cut off frequency of  $3\omega_{sc}/2$  it follows from the orthogonality of eqn. (5.4) that the  $V_0(I)$  must lie on the subcarrier. Therefore, if  $V_0(1)$ ,  $V_0(2)$  and  $V_0(3)$  are time adjacent output samples taken in sequence and lying on a sinewave of mean value  $e_0$  it can be shown that

$$e_1 = \frac{1}{\sqrt{3}} \left[ \frac{1}{3} (2V_0(2) - V_0(1) - V_0(3))^2 + (V_0(3) - V_0(1))^2 \right]^{1/2} \quad (5.5)$$

$$e_0 = V_0(2) - \frac{1}{\sqrt{3}} \left[ 3e_1^2 - (V_0(3) - V_0(1))^2 \right]^{1/2} \quad (5.6)$$

Any phase discrepancy occurring between subcarrier on two different luminance levels  $m, n$  is given by

$$\Delta\phi = \sin^{-1} \left[ \frac{V_0(2)_m - e_{0m}}{e_{1m}} \right] - \sin^{-1} \left[ \frac{V_0(1)_n - e_{0n}}{e_{1n}} \right] \quad (5.7)$$

In section 4.2 it was shown that asymmetry between the two analog channels can give rise to a subharmonic of subcarrier at the codec output and a suitable algorithm can be derived for this case using Fourier analysis. To

illustrate the principle, assume that subcarrier is applied to a codec which has a clamp level differential ( $VCX \neq VCY$ ). For a  $0^\circ$  sampling phase and a sampling rate of  $3\omega_{sc}$  the comparator input signal approximates to the waveform shown in Fig. 5.4.

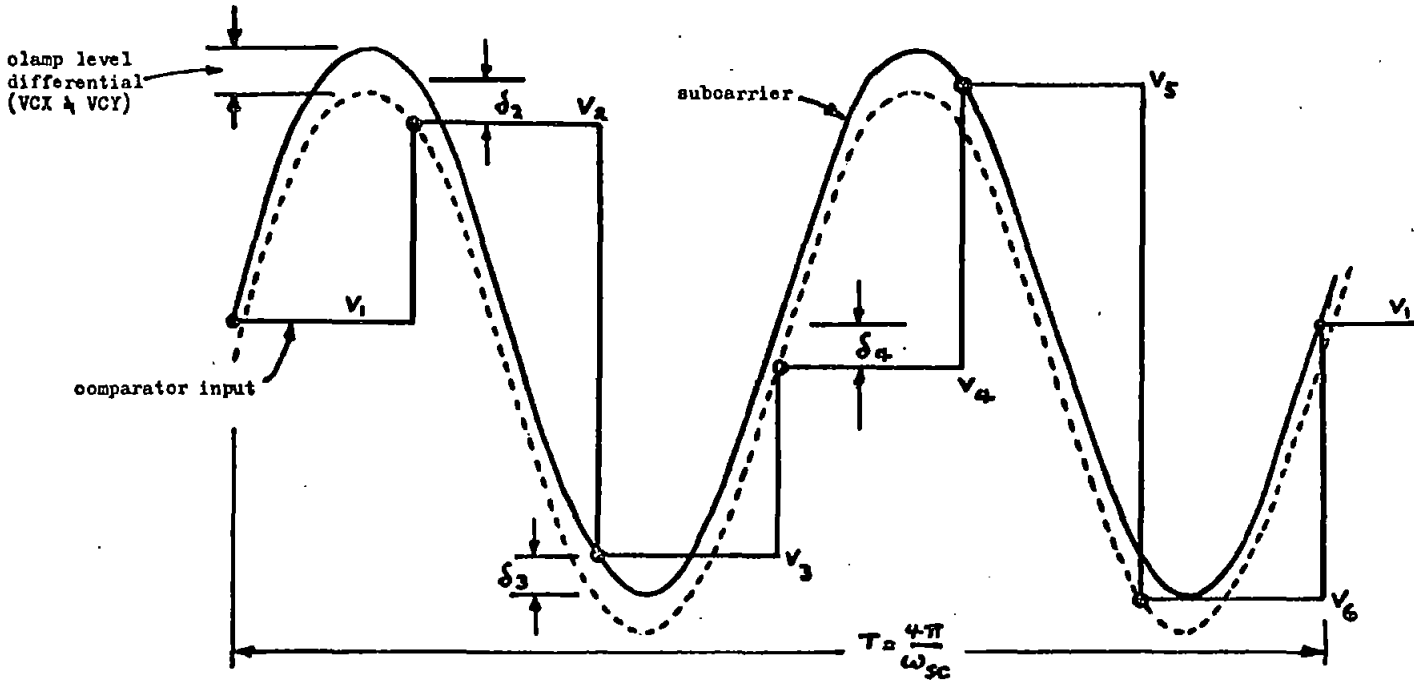


Fig. 5.4: comparator input for clamp level differential ( $VCX \neq VCY$ )

The codec output waveform will be similar except that generally

$$|\delta_2| \neq |\delta_3| \neq |\delta_4|$$

due to quantization and encoder errors. On the other hand the waveform is still periodic so the unfiltered or quantized codec output can be expressed as

$$e_q(t) = \sum_{k=-\infty}^{\infty} F_k e^{jk\omega_{sc}t/2}$$

where

$$F_k = \frac{1}{T} \int_0^T e_q(t) e^{-jk\omega_{sc}t/2} dt$$

Let the codec output levels in the period 0 to T be  $v_i$ ,  $i = 1, \dots, 6$  and for simplicity assume that the codec output updates instantaneously so that each  $v_i$  occupies a period  $T/6$ . We can extract any subharmonic component ( $k = 1$ ) and the subcarrier ( $k = 2$ ) and the results from appendix 3 are

$$e(t)|_{\omega_{sc}/2} = \frac{1}{\pi} [I_1^2 + R_1^2]^{1/2} \cos\left(\frac{\omega_{sc}t}{2} - \phi_1\right) \quad (5.8)$$

$$e(t)|_{\omega_{sc}} = \frac{1}{2\pi} [I_2^2 + R_2^2]^{1/2} \cos(\omega_{sc}t - \phi_2) \quad (5.9)$$

where

$$\begin{aligned} \phi_n &= \tan^{-1}(-R_n/I_n) \\ I_1 &= \sqrt{3} (V_1 + V_6 - V_4 - V_3)/2 \\ R_1 &= V_5 - V_2 + (V_6 + V_4 - V_1 - V_3)/2 \\ I_2 &= \sqrt{3} (V_1 - 2V_2 + V_3 + V_4 - 2V_5 + V_6)/2 \\ R_2 &= V_6 + V_3 - V_4 - V_1 - (V_1 + V_4 - V_3 - V_6)/2 \end{aligned}$$

Considering the subharmonic component

$$\begin{aligned} I_1 &= \sqrt{3} (\delta_4 - \delta_3)/2 \\ R_1 &= \delta_2 - (\delta_3 + \delta_4)/2 \end{aligned}$$

so generally there will be a subharmonic at the codec output even though the comparator input does not itself contain such a component. This result is in agreement with the model in Fig. 4.13 and the subharmonic can be considered as an intermodulation component. It is also clear that  $I_1$  and  $R_1$  are independent of the subcarrier amplitude (at least for this particular type of asymmetry) so the subcarrier-subharmonic ratio should tend to increase for increasing colour saturation.

Now consider the problem of evaluating subcarrier phase and gain errors when the codec output spectrum exhibits random noise. In analog video systems these errors (differential phase and gain) are usually measured by passing the (noisy) test signal through a bandpass filter; the filter is required primarily to remove the luminance component but it also provides a low noise bandwidth (300KHZ is regarded as a lower practical limit). In the simulation a similar filtering effect can be achieved if a narrowband sample of

the codec output spectrum is obtained via a Fourier transformation. A time sequence  $VO(I), I = 1, \dots, N$  is transformed to the set  $S(k), k = 1, \dots, N$  of harmonic components via the discrete Fourier transform<sup>95,98</sup>

$$S(k) = \sum_{I=1}^N VO(I) \exp \left[ -j \frac{2\pi(k-1)(I-1)}{N} \right] \quad , k = 1, \dots, N$$

In general all  $N$  discrete frequency components are evaluated requiring  $N^2$  multiplications and it is usual to reduce computation time by using a Fast Fourier transform<sup>89,95,98,99</sup>. On the other hand only  $N$  multiplications are required to extract the subcarrier term and if sampling is at  $3\omega_{so}$  then the (complex) subcarrier amplitude would be proportional to the term  $S(1 + N/3)$ .

Perhaps a more obvious and direct procedure for extracting the subcarrier from random noise is to use the principle of crosscorrelation detection. This readily gives both the amplitude and phase information of the subcarrier at the codec output (in contrast to autocorrelation) and it is this approach which is adopted in chapter 6.

#### 5.4 SUMMARY

The main points and conclusions of this chapter are as follows:

1. A breakdown of the possible types of error exhibited by a P.W.M. video encoder has been given and an attempt is made to group the errors under certain broad headings. In particular the errors can be grouped into static and dynamic errors and a different analysis is required for each type of error.
2. A mathematical model of the codec is developed in which simple algorithms are used to describe one or more of the encoder errors. This model will be used in chapter 6 to evaluate the effect of encoder errors upon a slowly varying test signal (static error) and upon subcarrier (dynamic

error). In the latter case the objective is to derive distribution laws for dynamic error and hence a general circuit design criterion.

3. The analysis programs require software simulations of a normal distribution and a narrow band codeo output filter and suitable algorithms are described. The normal distribution will be used for random noise simulation and in a Monte Carlo analysis for the error distribution laws. In the absense of noise, output filtering will be achieved by Fourier analysis and in the presence of noise filtering will be via crosscorrelation. The following analysis therefore involves several useful techniques which, at the time of writing, do not appear to have been applied to codeo error analysis.

The full modelling facilities are summarised in Fig. 5.5.

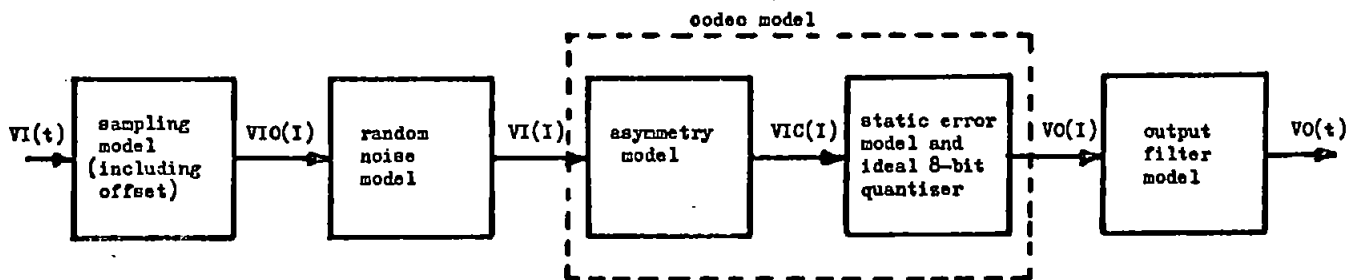


Fig.5.5: illustrating modelling facilities

## CHAPTER 6: THE ANALYSIS PROGRAMS & RESULTS

The codec model is incorporated as a subroutine into three analysis programs and the primary function of each program is summarized below:-

**Program 1:** To assess the effect of the encoder error sources (singularly and collectively) upon the static transfer characteristic of the codec. A triangular wave test<sup>89,93,85</sup> is applied by coding and decoding a ramp signal and the codec output is displayed on a computer graph plotter. The results are used as a starting point for Program 2.

**Program 2:** To assess the effect of the encoder error sources upon the transformation error suffered by a high frequency test signal passed through the codec. Colour subcarrier is applied to the codec and random errors are generated by Monte Carlo sampling of the error sources. It is considered that differential phase and gain is a sufficiently critical measure of dynamic error to permit formulation of a design criterion and to this end the probability distributions for differential phase and gain are evaluated.

**Program 3:** To assess the effect of white Gaussian noise as an error reducing mechanism.

### **6.0 PROGRAM 1: TRIANGULAR WAVE TEST**

In this test the codec output is usually subtracted from the oodeo input and the error wave displayed on an oscilloscope but here the actual codec output is displayed rather than the error wave so that the results can be



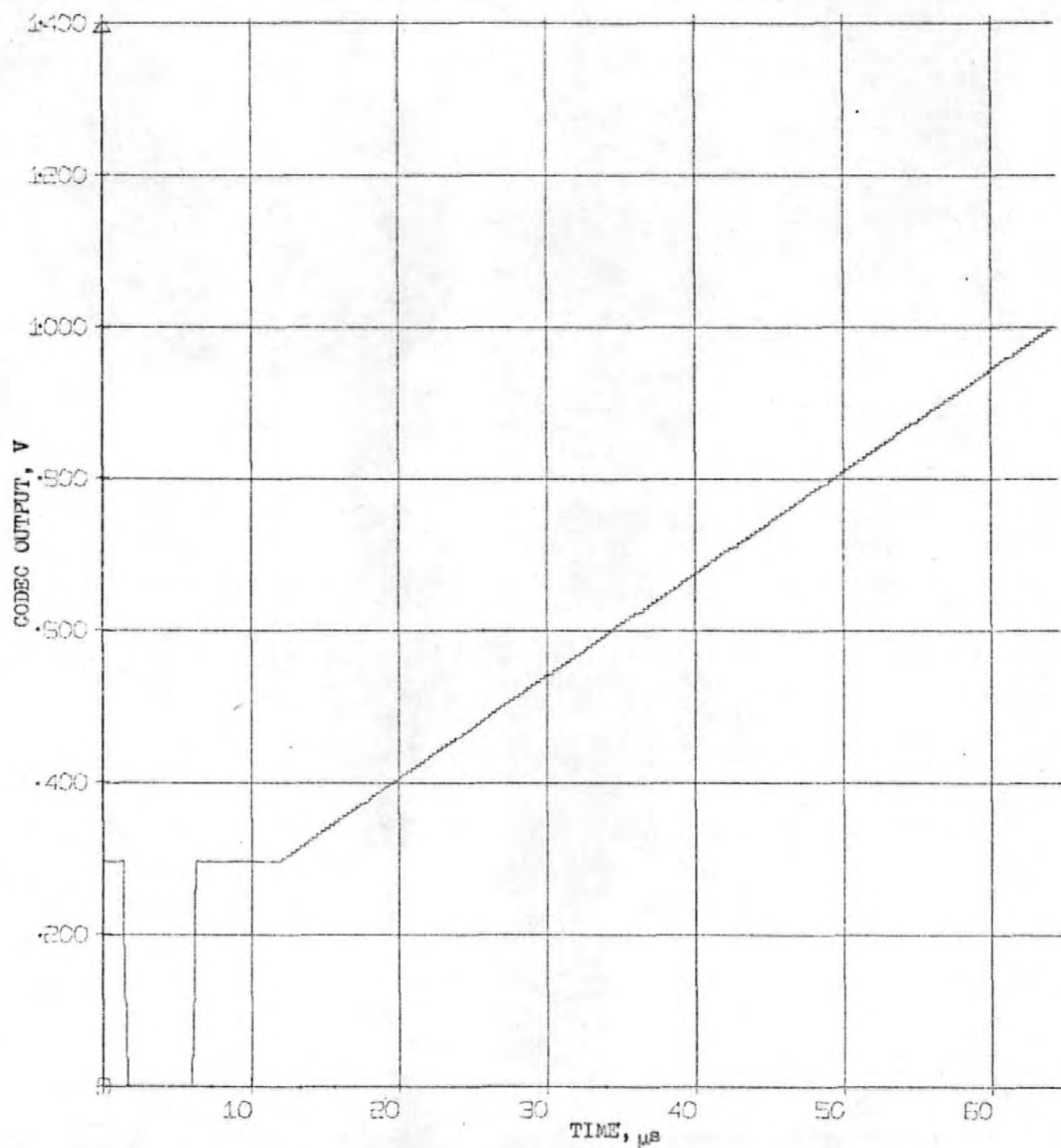


Fig. 6.1 Unfiltered output of an ideal 8-bit codec. Codec input is a noise-free 625-line composite ramp.

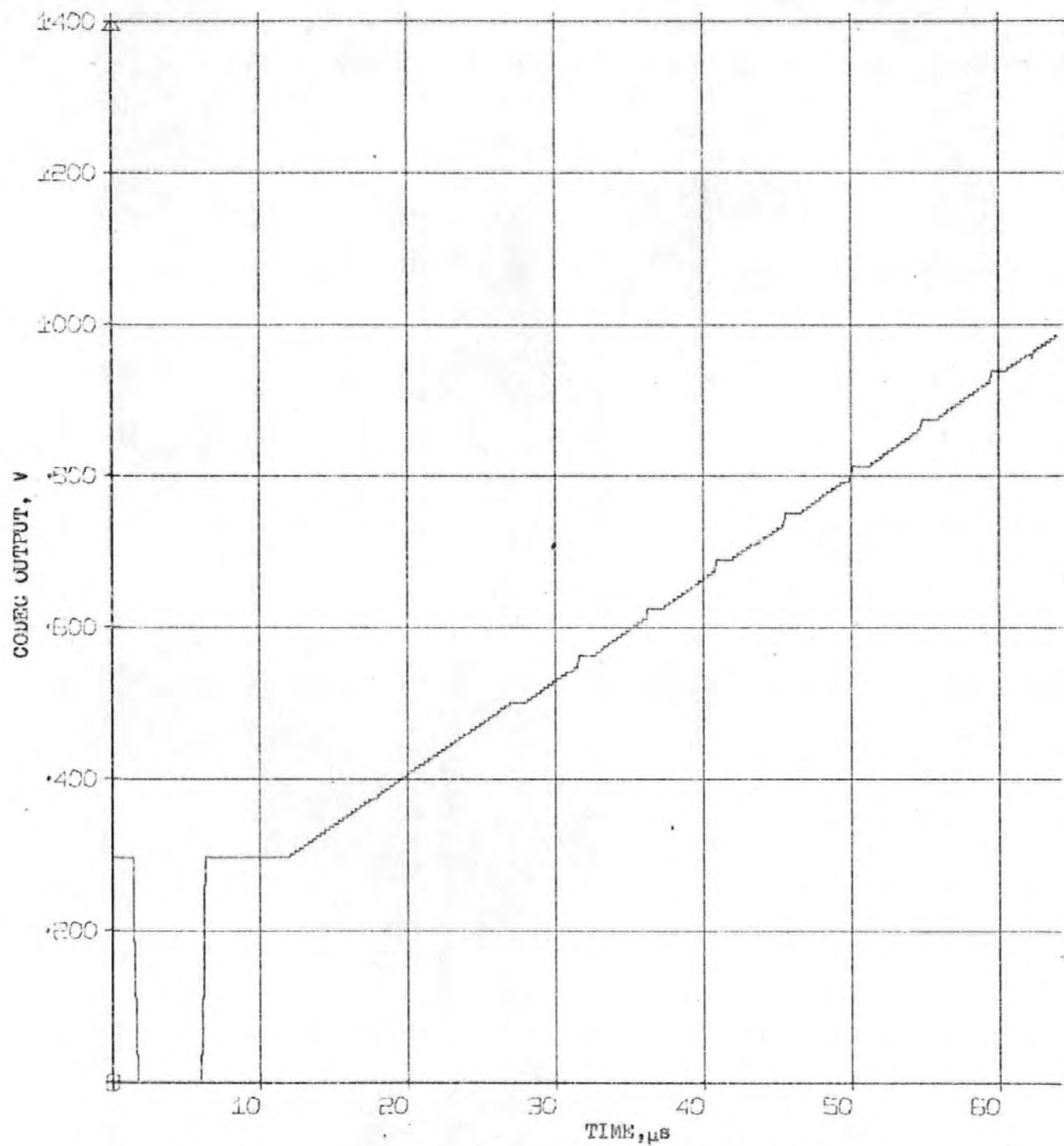


Fig. 6.2 Illustrating the effect of a +3q error (+2.34%) in the MSB of the 4-bit decoder.

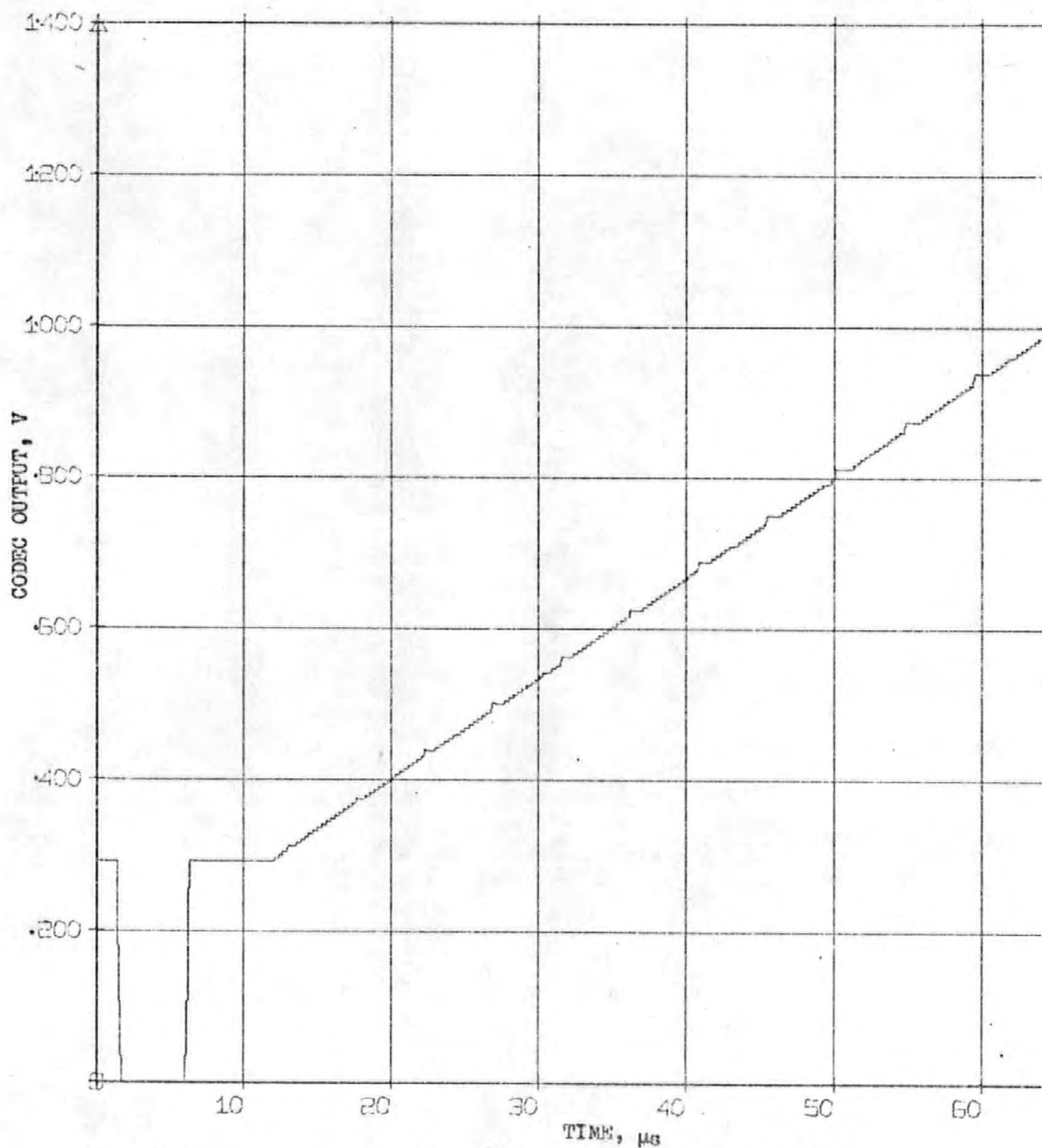


Fig. 6.3 Illustrating the effect of incorrect quantizer gain resulting in a  $+3q$  error (+1.25%) in the full scale output of the 4-bit decoder.

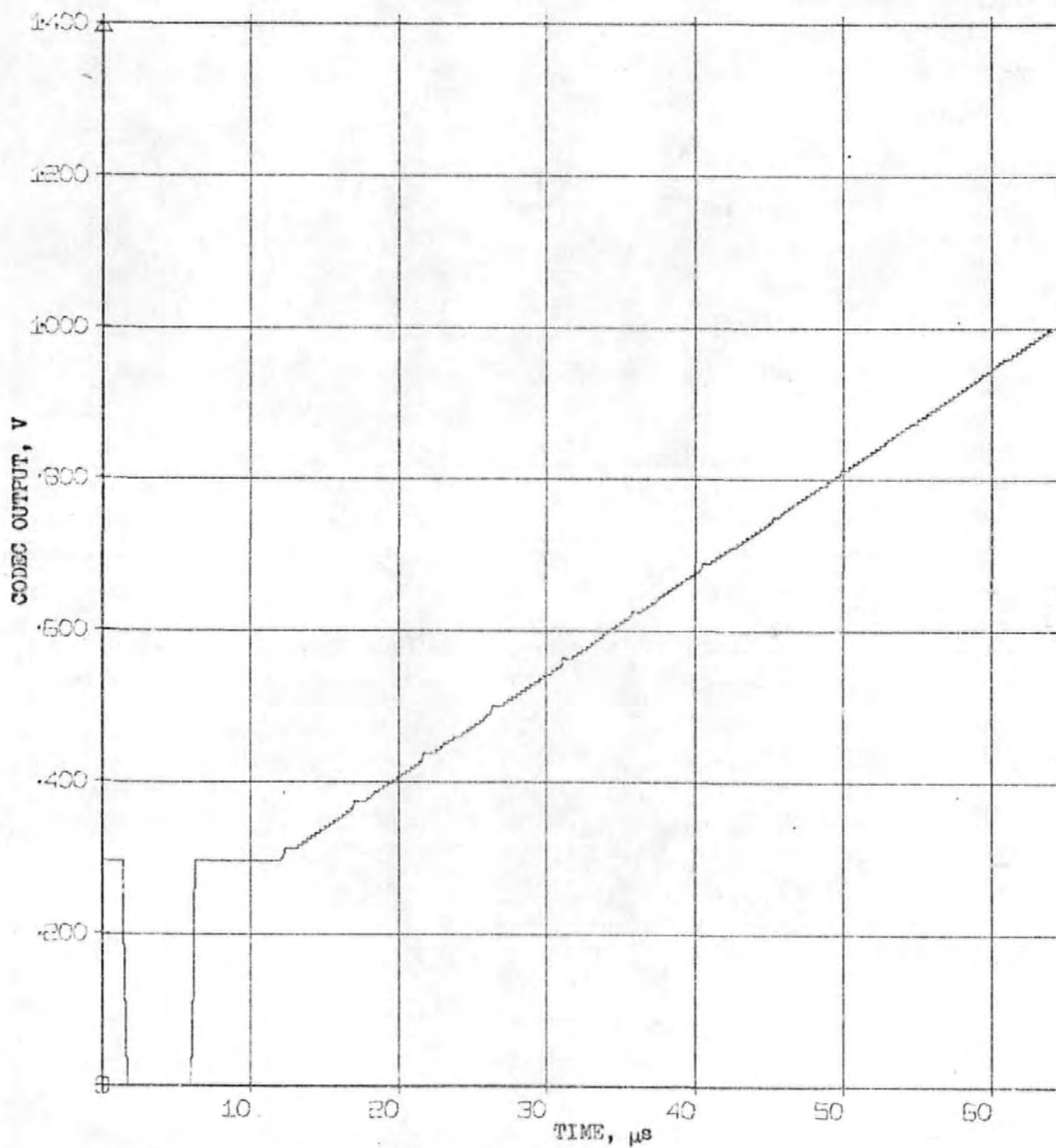


Fig. 6.4 Illustrating the effect of a  $3\sigma$  maximum deviation from ramp linearity (1.17% ramp nonlinearity)

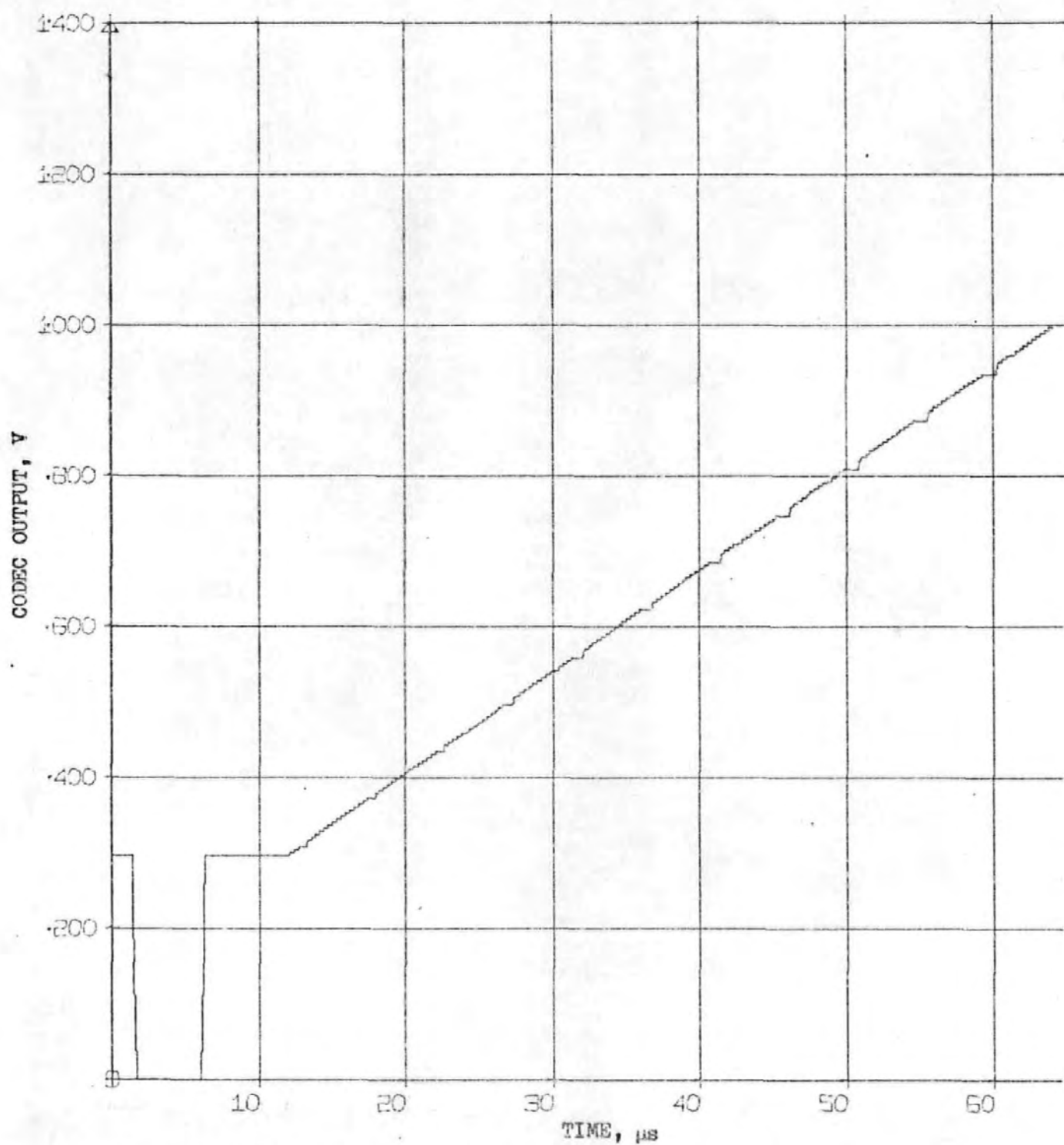


Fig. 6.5 Illustrating the effect of a  $+3q$  ( $+1.17\%$ ) error in the A-ramp amplitude.

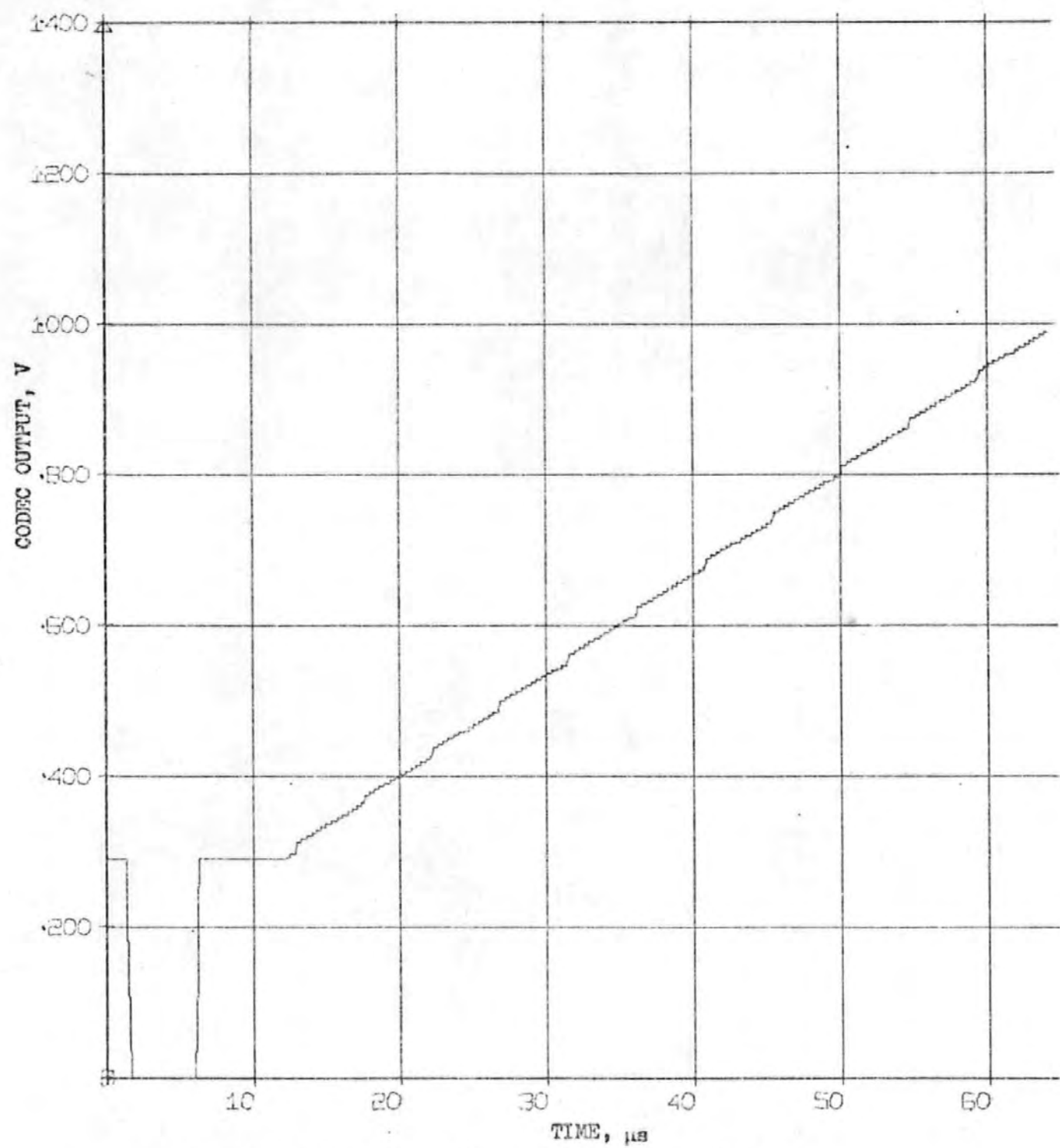


Fig. 6.6 Illustrating the effect of a  $+3q$  (+18.75%) error in the B-ramp amplitude.

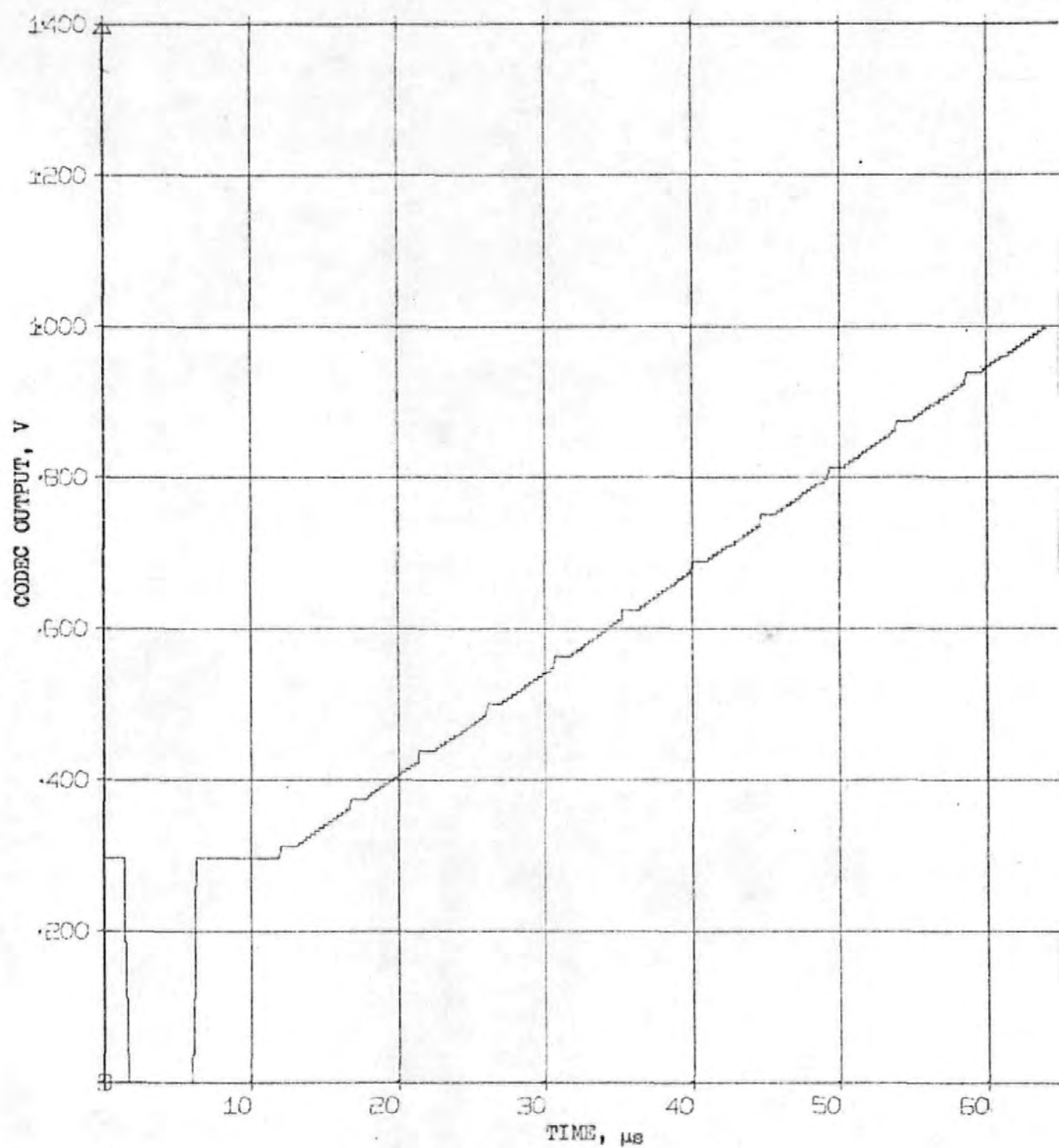


Fig. 6.7 Illustrating the effect of a  $+3q$  ( $+0.47\%$ ) error in the mean level VOA of the A-ramp.



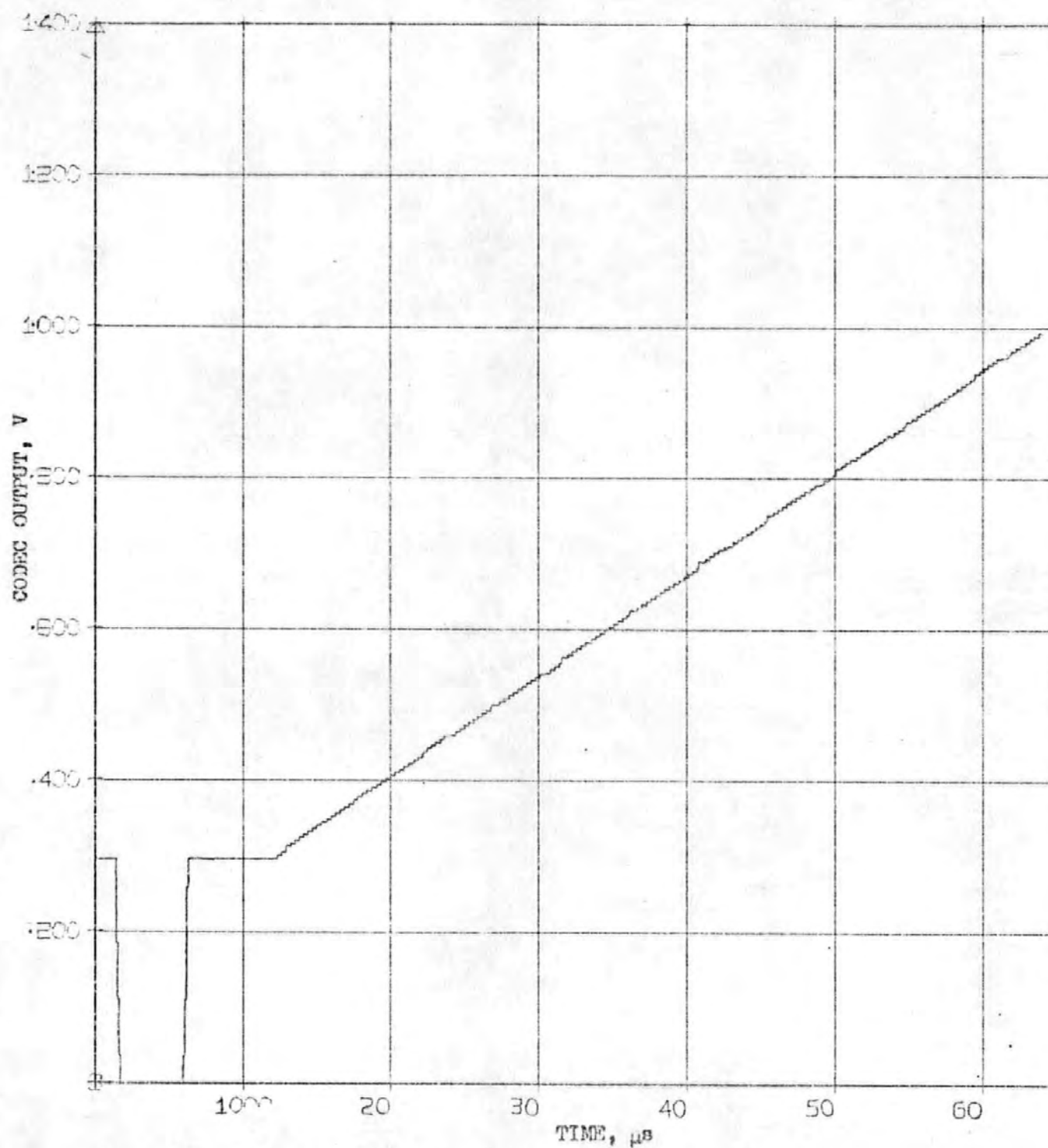


Fig. 6.8 Illustrating the combined effect of a random set of 6 codec errors. Individually each error generates a maximum voltage error of  $1q$ .

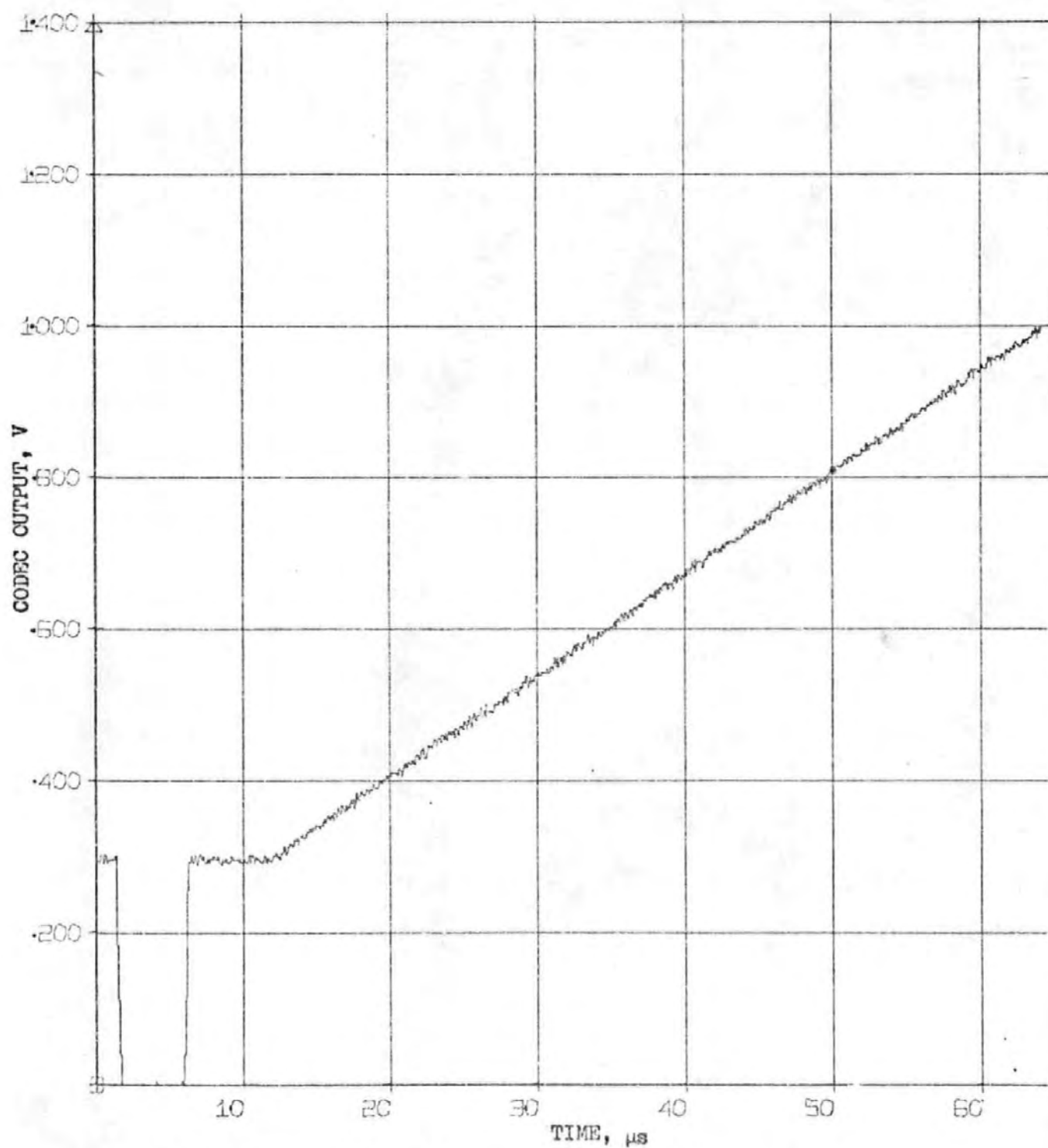


Fig. 6.9 Masking of the codec errors in Fig. 6.8 by Gaussian noise at the codec input, SNR = 47dB.

compared directly with the experimental results in Chapter 4. Also for comparison purposes the simulated ramp is at 625-line frequency but the results are actually independent of the rate of change of the ramp i.e. this is really a pure dc test.

Referring to the program in appendix 4, the input array VI holds data corresponding to a 625-line composite ramp sampled at 3 times subcarrier frequency. This signal is coded and decoded using subroutine CODEC (which differs from CODEX only in the input and output procedures) and the unfiltered codec output is then displayed on a graph plotter. Output filtering could have been achieved using SHANNON's interpolation (section 5.3) or, more accurately, by using the sine integral since in practice rectangular pulses are applied to the filter. However, both of these processes involve considerable computation and were considered unnecessary in this preliminary analysis. The plotter scale is small enough to conveniently display the complete ramp in the time domain whilst being large enough to resolve 8-bit quantizing steps, see Fig. 6.1. The slight irregularity in the 8-bit quantizing steps and on the sync pulse is due to plotter interpolation between sampling points.

The characteristic effect of a specific error will be clearly evident if the error is made artificially large e.g. each error source could be arranged to generate a (maximum) voltage error of  $+3q$  or  $+35.1mV$  (the maximum voltage error is taken since the error generated by a source could be a function of other variables - such as luminance level). Consider the gain and weighting errors in the 4-bit decoder. The MSB voltage of the 4-bit decoder would be in error by  $+3q$  ( $+2.34\%$ ) and the quantizer gain would be such as to give a maximum error of  $+3q$  in the decoder output i.e. the full-scale output error would be  $+3q$  ( $+1.25\%$ ). Fig. 6.2 and 6.3 correspond to these particular errors respectively and in each case the encoder is assumed to be otherwise ideal and the input signal is noise-free. The effects of different types of ramp

error are illustrated in Figs. 6.4 - 6.7. Fig. 6.4 shows the effect when the maximum deviation from ramp linearity is  $3q$  (as defined in section 3.3.3) and in Fig. 6.5 the A-ramp amplitude is +3.0351V instead of +3.0V, all other parameters being ideal. The effect of a  $+3q$  error in the B-ramp amplitude is markedly different from most errors so that this form of error is easily detected if present. The predicted distortion in Fig. 6.6 is very similar to that observed in practice, Fig. 4.2(d).

Now consider a more realistic situation in which each error is limited to a maximum of  $1q$  and where multiple errors are simultaneously present. Assume for example that all 6 error sources corresponding to Figs. 6.2 - 6.7 are present but that each error source only gives a maximum voltage error of  $1q$  and that the errors are selected on a random basis i.e. some positive, some negative. The effect of one random combination is shown in Fig. 6.8 and Fig. 6.9 illustrates the error masking effect of random noise. Assuming the error to be masked corresponds to 7-bit quantizing error then, using eqn. (4.1) (since the same conditions apply), the codec input SNR should be  $< 47\text{dB}$  approximately. Fig. 6.9 therefore provides some support for DEVEREUX's<sup>31</sup> empirical law.

The usual way of expressing the static error in Fig. 6.8 is in terms of the relative dc accuracy<sup>93,85</sup>. This is the maximum deviation from the ideal static transfer characteristic (a straight line through zero and full-scale) expressed as a percentage of full-scale and for Fig. 6.8 it is nearly 0.8% (including quantizing error) or  $0.6\% \pm \frac{1}{2}\text{LSB}$ . A second random combination of  $1q$  errors generated a maximum impairment similar to 6-bit quantizing error - corresponding to a relative dc accuracy of nearly 1.6% or  $1.4\% \pm \frac{1}{2}\text{LSB}$  (this is about the same as the accuracy exhibited in Fig. 4.3(b)). In contrast, the accuracy in current high-speed 8-bit encoders<sup>85</sup> is typically  $0.1\% - 0.4\% \pm \frac{1}{2}\text{LSB}$  so, as a rough design criterion, it is clear that the

random voltage errors in the encoder should usually be significantly less than  $1q$ . More detail can be added to this design criterion by examining the dynamic error suffered by a high frequency signal and this is studied using Program 2.

#### 6.1 PROGRAM 2: MONTE CARLO ANALYSIS

The classical method of measuring dynamic error is to apply a high frequency sinusoidal signal and to examine the codec output spectrum<sup>10,89,93,96</sup>. SMITH<sup>93</sup> suggests that dynamic error in video encoders should be characterised by the relative amplitude of wanted and unwanted components in the spectrum and he defines a 'dynamic linearity' on this basis. However, it is considered that differential phase and gain measured at subcarrier frequency is a more relevant measure of dynamic error since its subjective effects are well understood and its limits for video equipment are reasonably well defined<sup>3</sup>. The error distributions used to derive a design criterion are therefore derived in terms of differential phase and gain, although we must first define the meaning of phase and gain error in a digital system.

In an ideal codec (no errors) colour subcarrier suffers small phase and gain errors due to nonlinearity arising from quantization. The errors vary cyclically with luminance level and the variation is only on a microscopic basis due to the fine structure of 8-bit quantizing error. To examine these phase and gain errors some way of changing the subcarrier luminance level on a microscopic basis is required and a suitable test signal would comprise low level subcarrier superimposed upon a ramp. Clearly these errors are not differential phase and gain in the conventional sense since, conventionally, differential phase and gain is a measure of subcarrier phase and gain variations over the whole luminance range i.e. on a macroscopic basis. We might refer to the above phase and gain errors generated by an ideal codec as



'quantizing phase and gain error' and this is discussed further in appendix 2. On the other hand it is possible for the practical P.W.M. encoder to possess nonlinearity on a macroscopic basis, see for example Figs. 6.3 - 6.5. Whilst the error in these figures still varies cyclically with luminance level (i.e. it still tends to be localized) the error tends to be worse at one end or the other of the luminance range. If the codec is to be of practical use the nonlinearity will be less pronounced, as in Fig. 6.8 for example, but a macroscopic variation is still to be expected in most cases and the conventional test signal could be a useful measure of chrominance nonlinearity. In the United Kingdom this test signal is a 5-riser luminance staircase with 140mV peak to peak subcarrier superimposed upon each of the 6 luminance levels. The phase and amplitude of the subcarrier on 5 luminance levels is compared with the phase and amplitude of the subcarrier at black level and the largest error is taken as the differential phase and gain respectively. We will refer to this signal in the following analysis.

In practice a codec will possess a random set of errors and this situation can be simulated by assigning a probability law to each error source and then sampling each error source on a Monte Carlo basis. The choice of law is discussed in chapter 7 and it suffices here to state that a normal law  $N(\mu_1, \sigma_1)$  is a reasonable assumption for all error sources, see Fig. 6.10. The differential phase and gain for this particular set of encoder errors can now be found and probability distributions for differential phase and gain can be obtained by repeating the above procedure for many random sets of errors. In effect we are simulating the results of measurements on many codecs built to the same specification. Suppose for example that the magnitude of the differential phase  $p_d$  is 'measured' for many codecs using the Monte Carlo simulation. Since  $p_d$  arises from a complex combination of normally distributed random variables it is reasonable to expect  $|p_d|$  to be a continuous random

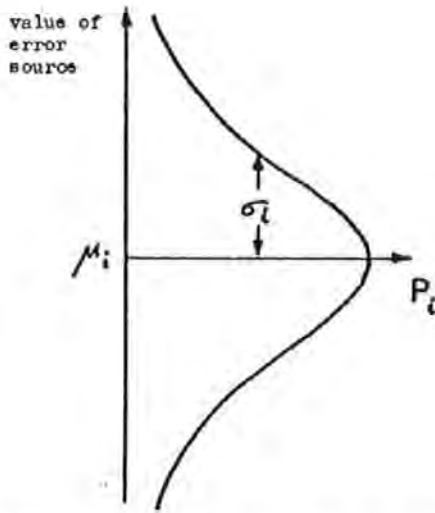


Fig. 6.10: normal p.d.f. assigned to an error source.

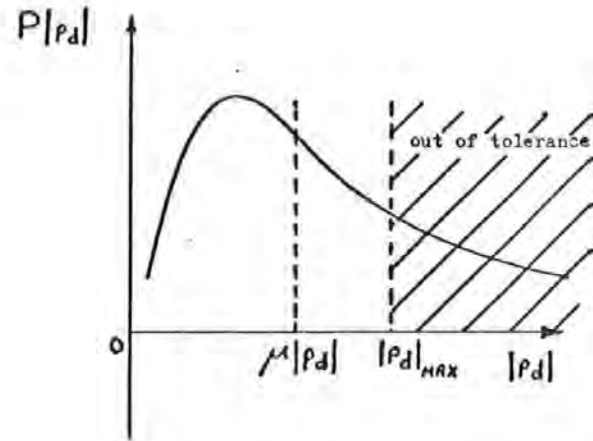


Fig. 6.11: generalized p.d.f. for a differential phase measurement.

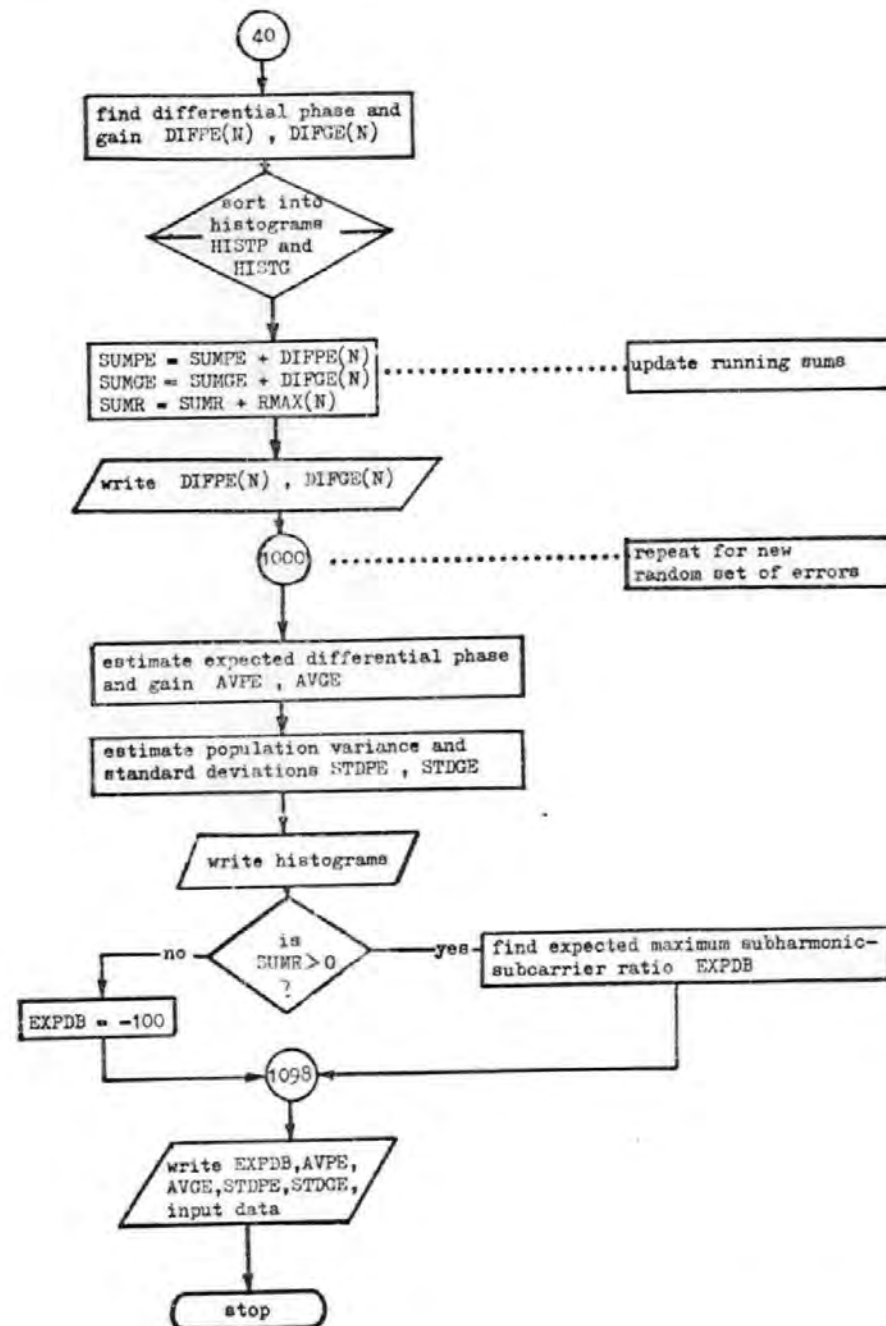
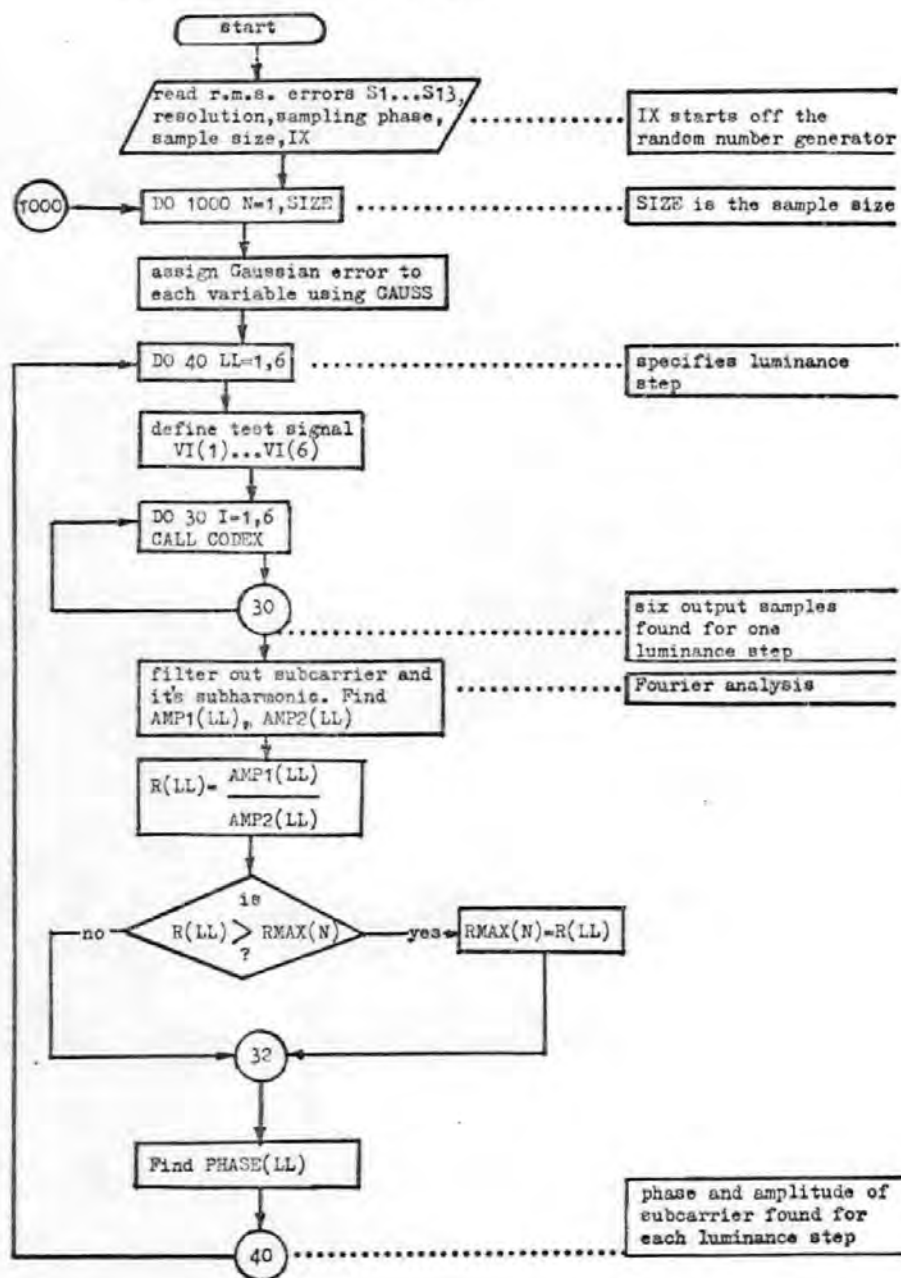
variable as suggested in Fig. 6.11 and the encoder design might be regarded as acceptable if, say,

$$\int_0^{|p_d|_{\max}} P|p_d| d|p_d| > 0.9$$

where  $|p_d|_{\max}$  is some limit imposed by current codes of practice for analog video systems<sup>3</sup>. The objective is therefore to reduce  $\mu|p_d|$  and the variance  $\sigma^2|p_d|$  until some such inequality is reached and this is achieved by progressive constraining of the rms errors  $\sigma_i$ . The significant point is that if the  $\sigma_i$  are carefully chosen each time they are constrained then it is possible to derive a general circuit design criterion for the codec. Put more specifically, it is necessary that the (maximum) voltage error for all error sources should be within the same prescribed limit (say  $q/2$ ) for 95% of the time. A random selection of the  $\sigma_i$  would in any case be unrealistic since on average some error sources would then contribute significantly more error than others whereas consistent circuit design is more likely to result in all errors contributing approximately equally to picture impairment.



Fig. 6.12: Flow chart for Program 2



The flow chart for Program 2 is shown in Fig. 6.12 and the corresponding program is given in appendix 4. Referring to the flow chart, the rms errors  $S_i$  ( $\equiv \sigma_i$ ) are read in for 13 error sources and subroutine GAUSS uses the Gaussian random number generator outlined in section 5.2 to assign a normal probability law to each source. The input array VI corresponds to a stable noise-free 5-riser staircase test signal sampled at 3 times subcarrier frequency and, as indicated in Fig. 5.4, only 6 samples or 2 cycles are required per luminance step in order to completely define any subharmonic of subcarrier. Each luminance step is coded and decoded by the codec model (subroutine CODEX) and the output is filtered by Fourier analysis. This yields the amplitude (AMP 2) and phase of the subcarrier on each luminance step and also the amplitude (AMP 1) of any subharmonic component. The maximum subharmonic to subcarrier ratio is searched for as the computation progresses through each luminance step and the result is stored in RMAX(N). The differential phase and gain (DIFPE(N) and DIFGE(N) respectively) are then found for the  $N^{\text{th}}$  random set of errors and these values are sorted into their respective histograms. Running sums of DIFPE(N), DIFGE(N) and RMAX(N) are kept and the whole process is repeated for a new random set of errors. When the required sample size N has been reached the population mean and variance are found using the best estimates e.g. for differential phase

$$\mu |P_d| \approx \frac{1}{N} \sum_N |P_d(N)|$$

$$\sigma^2 |P_d| \approx \frac{1}{N-1} \sum_N \left( |P_d(N)| - \frac{1}{N} \sum_N |P_d(N)| \right)^2$$

Finally, the subharmonic to subcarrier ratio will vary with luminance level and the program computes the maximum ratio that might be expected.

The video gain in the model is adjusted so that in the absence of errors a 100/0/100/0 colour bar signal just fills the quantizing range. These

colour bars are 1.234V peak to peak at the codec input compared with 1.07V peak to peak for the test signal so that the test signal falls well within the quantizing range. The sample size is a compromise between a low sampling error and a reasonable central processor time. For example, we can be 95% confident that the population mean lies within the following bounds

$$\mu |p_d| = \frac{1}{N} \sum_N |p_d(N)| \pm \frac{1.96 \sigma |p_d|}{\sqrt{N-1}}$$

Typical, although not necessarily acceptable, values might be  $4^\circ$  for the sample mean and  $2^\circ$  for the standard deviation. In this case, if the 95% confidence limits are to be  $< 5\%$  of the sample mean then  $N > 400$  and in fact  $N = 500$  is used for all computer runs. The processing time for 500 samples is over 2 hours on an IBM1130 computer or about 1 hour on an ICL 1905 machine.

### 6.1.0 RESULTS

In section 6.0 codec errors are related to the quantum interval  $q$ ; a  $1q$  error in an error source for instance means that the maximum possible voltage error incurred by that source is  $1q$  or 11.7mV. The concept is easy to apply in most cases although it is less apparent for some parameters such as 'gain differential' or 'sampling time offset'. Essentially, a gain differential error of  $1q$  means that a discrepancy between analog channel gains lead to a maximum voltage difference of  $1q$  between channels and clearly this occurs for the maximum input signal (1.234V). A  $1q$  sampling time offset error means that a sampling pulse is offset in time such that the maximum voltage error incurred when sampling a chrominance signal is  $1q$ . The maximum error occurs when sampling coincides with the maximum rate of change of the signal but it also depends upon the chroma amplitude and a nominal peak to peak chroma amplitude of 33% of the quantizing range is assumed in the following analysis.

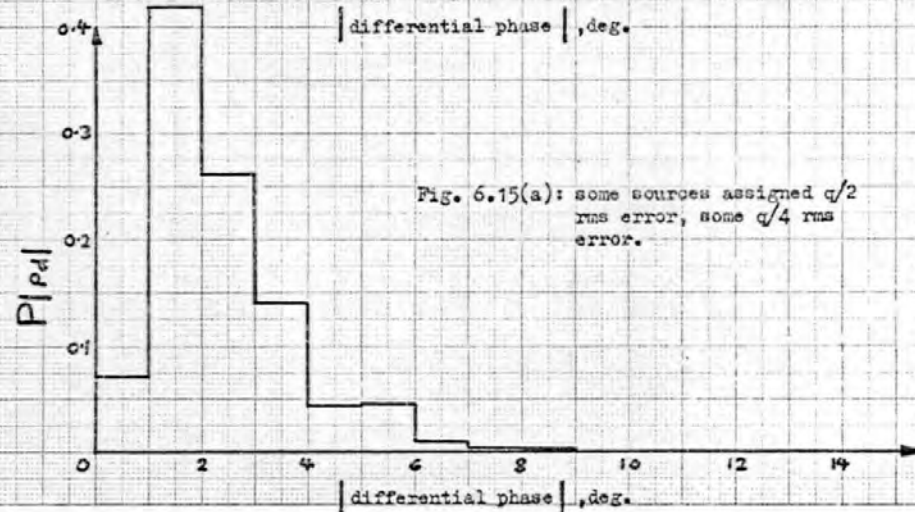
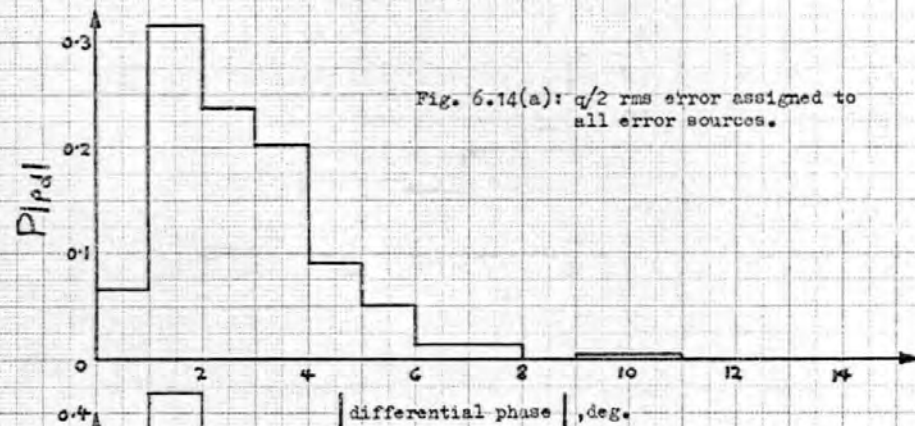
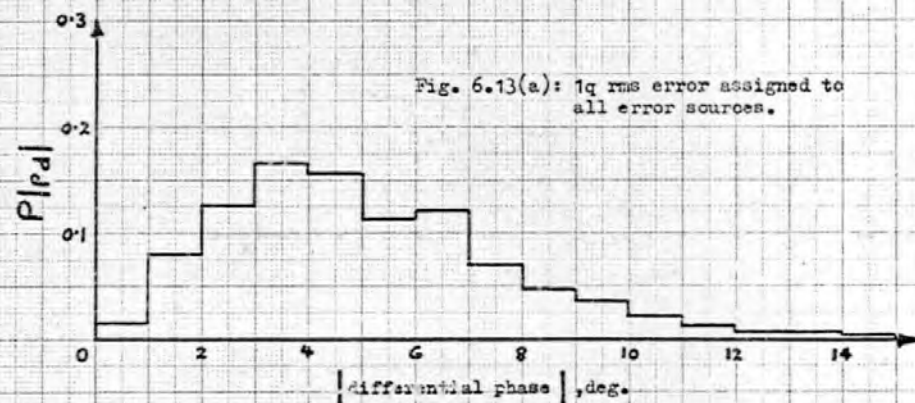
The above concept is retained for the Monte Carlo analysis although now a lq error corresponds to the rms error  $\sigma_i$ . Suppose for example that  $\sigma_i$  corresponds to a lq error in the sampling time offset; this means that the maximum possible voltage error arising from sampling time offset is within  $\pm lq$  for 68% of codecs measured. In this particular case, and using the above mentioned chroma amplitude,  $\sigma_i \approx 1ns$ . Program 1 indicates that a lq error is a reasonable starting point for the analysis and initially a lq error is assumed for all error sources. These initial conditions are summarized in table 6.1 and the table should be read in conjunction with the relative part of Program 2 (taking  $\sigma_i \equiv S_i$ ).

TABLE 6.1

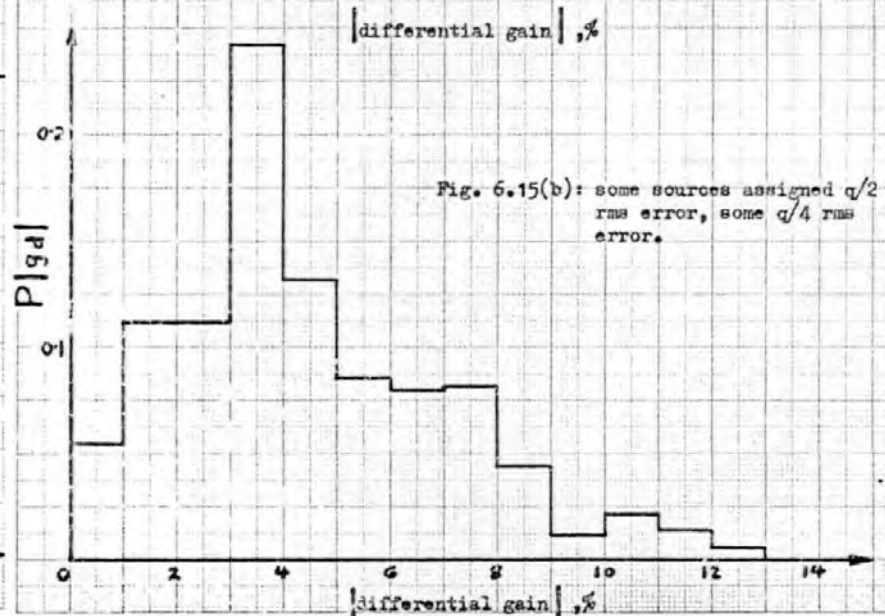
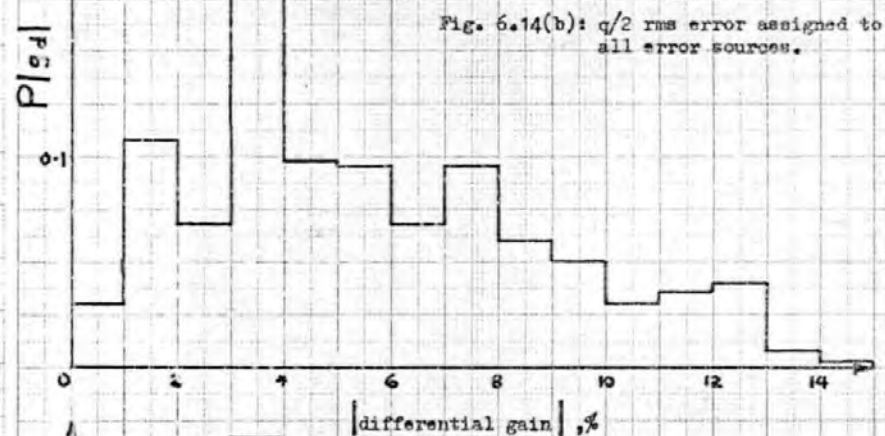
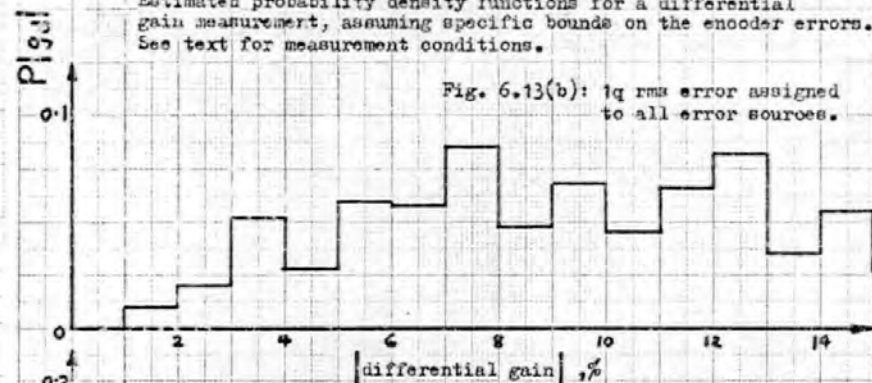
| i  | $\sigma_i$ for lq error | source of error                      |
|----|-------------------------|--------------------------------------|
| 1  | 0.0037                  | gain differential                    |
| 2  | 0.0117                  | clamp level                          |
| 3  | 0.0117                  | clamp level differential             |
| 4  | 0.0117                  | A-ramp reference                     |
| 5  | 0.0117                  | B-ramp reference                     |
| 6  | 0.0117                  | A-ramp amplitude                     |
| 7  | 0.0117                  | B-ramp amplitude                     |
| 8  | 0.0117                  | max. oscillation amplitude on A-ramp |
| 9  | 0.0023                  | ramp nonlinearity                    |
| 10 | 0.0117                  | quantizer gain                       |
| 11 | 1.0000                  | sampling time offset                 |
| 12 | 0.01                    | quantizer binary weighting, MSB      |
| 13 | 0.02                    | quantizer binary weighting, NMSB     |

The results of this and subsequent Monte Carlo runs depend upon the

Estimated probability density functions for a differential phase measurement, assuming specific bounds on the encoder errors. See text for measurement conditions.



Estimated probability density functions for a differential gain measurement, assuming specific bounds on the encoder errors. See text for measurement conditions.





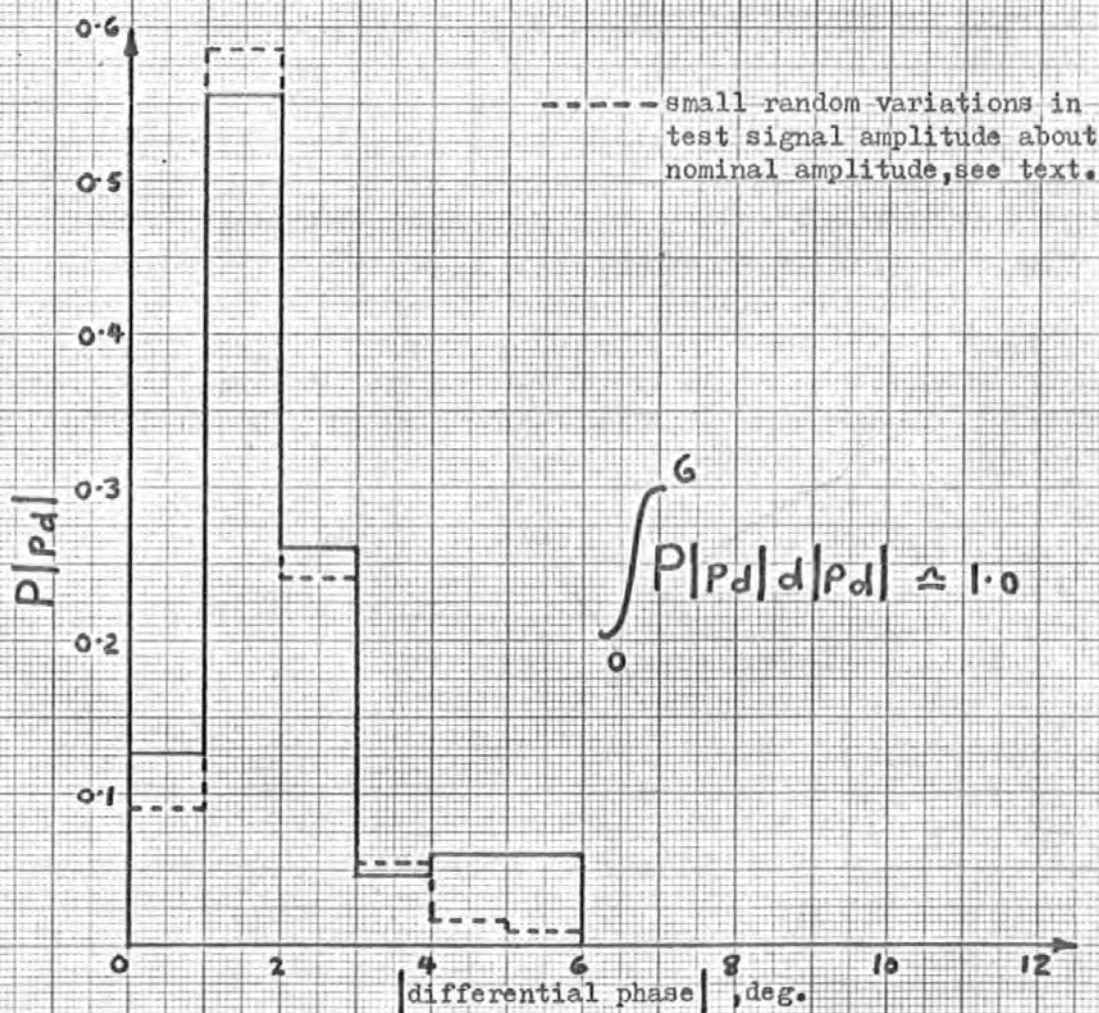
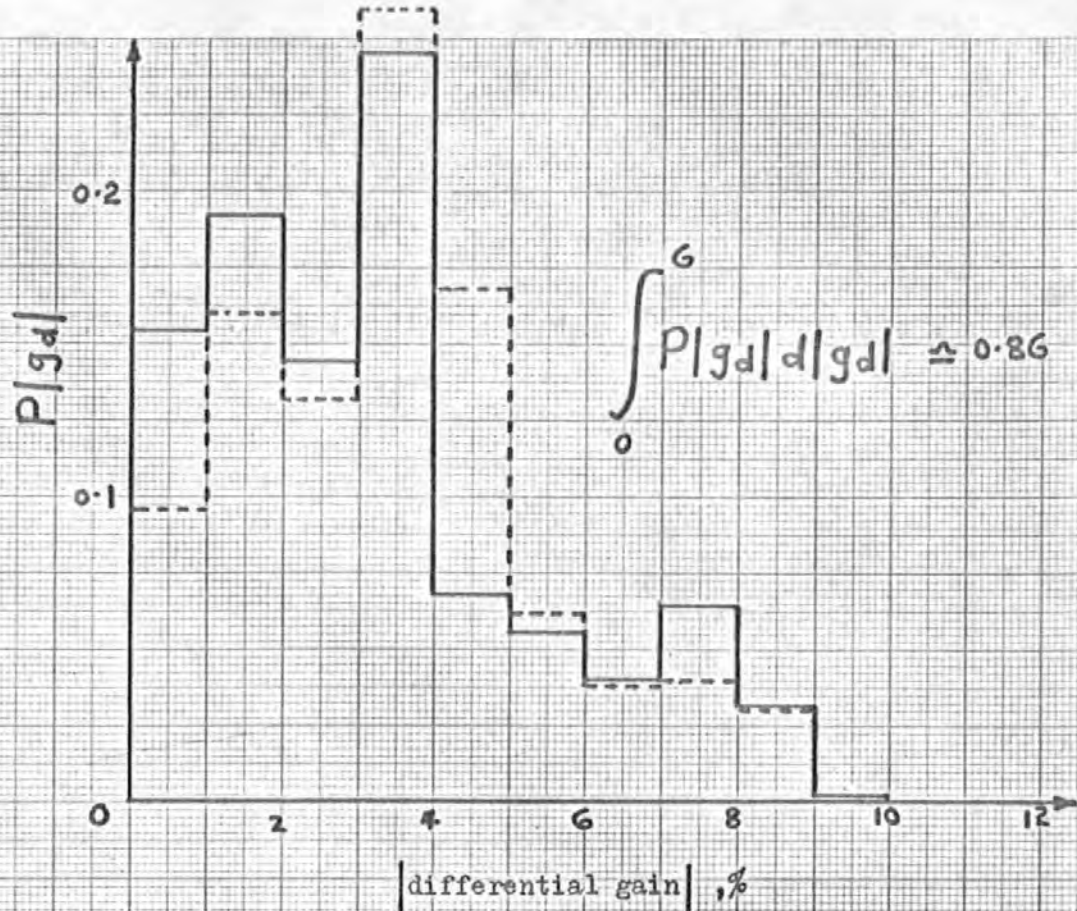
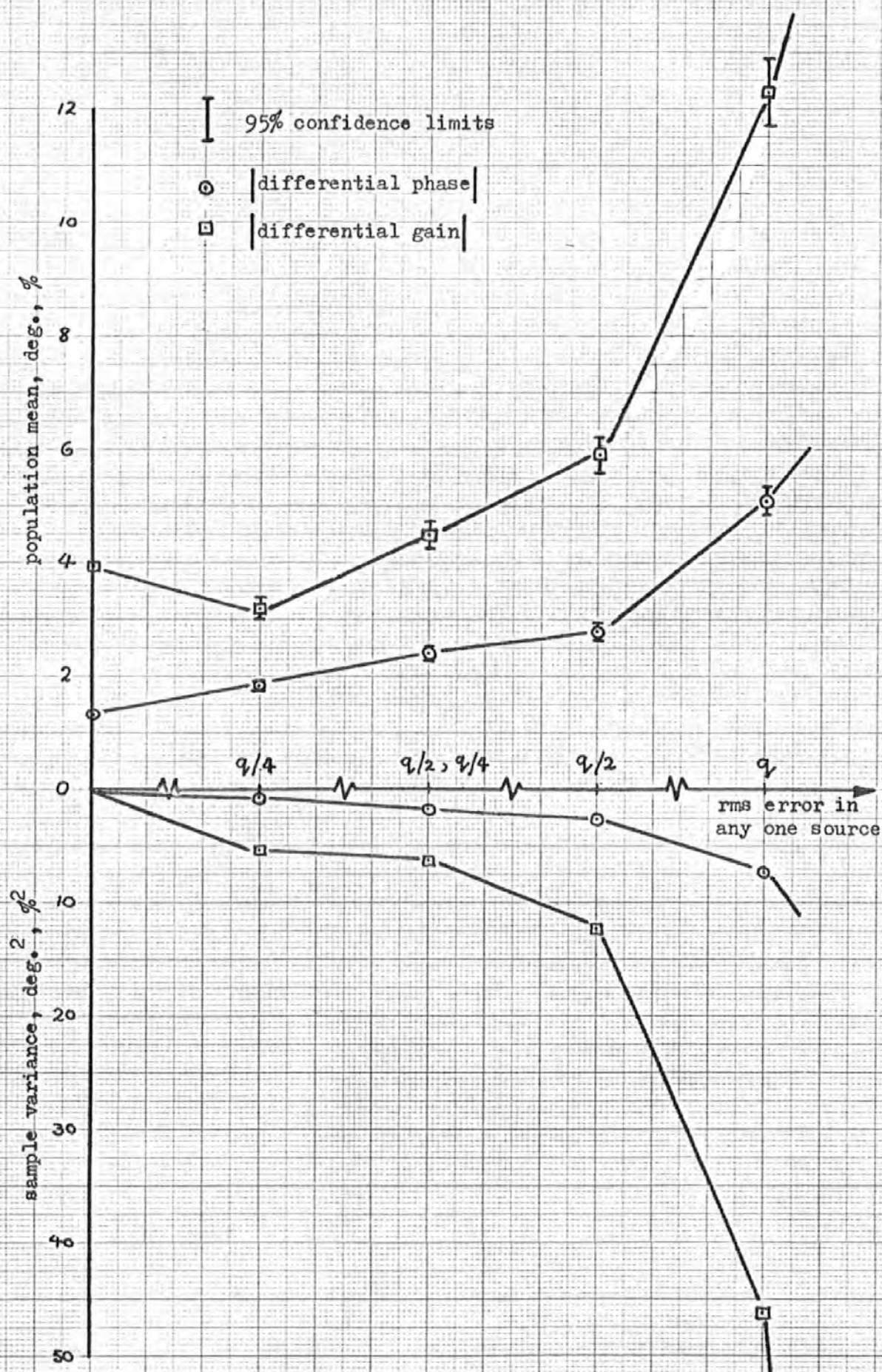


Fig. 6.16: estimated probability density functions for differential phase  
 and gain measurements assuming  $q/4$  rms error in all error sources  
 See text for measurement conditions.

Fig. 6.17: Estimated mean and variance for differential phase and gain measurements as a function of encoder error. See text for measurement conditions.





measurement conditions and these can be stated as follows: the test signal is a noise-free, composite 5-riser luminance staircase with 140mV peak-peak subcarrier on each luminance level. Also, the subcarrier is sampled in an arbitrary but fixed phase ( $0^\circ$ ) and the full scale codec input is set to 1.234V so that 100/0/100/0 colour bars just fill the quantizing range. Having stated these conditions we can proceed with the analysis for the  $\sigma_i$  shown in table 6.1 and the results are summarized in Figs. 6.13 and 6.17. These graphs can be interpreted as the results of measurements on 500 codecs when random circuit errors are such that each error source produces a maximum voltage error that is within  $\pm q$  for 68% of codecs measured. Circuit errors of this magnitude are unacceptable for a broadcast quality codec since they result in unacceptably high mean and variance for differential phase and gain. For the purposes of defining performance limits we can regard the codec as 'studio equipment' and at present such equipment should have a high probability of not exceeding  $\pm 6^\circ$  differential phase and  $\pm 6\%$  differential gain<sup>3</sup>. Clearly, to meet this specification, the circuit errors must be reduced and, for the same sampling phase, the mean and variance are significantly improved if all  $\sigma_i$  correspond to  $q/2$  error as in Figs. 6.14 and 6.17. These graphs can be interpreted as the results of measurements on 500 codecs when the random circuit errors are such that each error source produces a maximum voltage error within  $\pm q$  for 95% of codecs measured. The results in Fig. 6.14 and Fig. 6.17 indicate that there is a 96% probability of a differential phase measurement not exceeding  $6^\circ$  and that there is a 58% probability of a differential gain measurement not exceeding  $\pm 6\%$ . This is much nearer the above specification for studio equipment although the mean and variance for differential gain is still too high and further iteration is required.

An improvement can be achieved by reducing some rms errors to

$q/4$ . For instance,  $\sigma_3$  represents a clamp level differential which arises from the difference in offset voltage for the two clamp transistors. If these transistors are matched the offset voltages can be within several millivolts so that it would be more appropriate if  $\sigma_3$  corresponds to  $q/4$ . Similarly, it is reasonable to expect the percentage current error to be the same for each bit in the 4-bit decoder so that the voltage error for the NMSB must be half that of the MSB. This means that if  $\sigma_{12}$  corresponds to  $q/2$  then  $\sigma_{13}$  should correspond to  $q/4$  thereby giving a NMSB voltage error of  $<3\text{mV}$  for 68% of codecs measured. Inserting  $q/4$  errors for  $\sigma_3$  and  $\sigma_{13}$  and  $q/2$  errors for all other  $\sigma_i$  gives the results shown in Fig. 6.15 and Fig. 6.17; the mean differential gain is now  $4.5 \pm 0.22\%$  to 95% confidence and there is now a 74% probability of the differential gain not exceeding the  $\pm 6\%$  limit.

This is still unsatisfactory as far as a production yield is concerned and a further iteration was carried out where all  $\sigma_i$  correspond to  $q/4$  errors. The results in Fig. 6.16 and Fig. 6.17 are now more acceptable and they can be interpreted as follows; there is quite a high probability (86%) that both differential phase and gain will fall within the bounds normally accepted for analog studio equipment provided that the circuit design is such that there is a high probability (95%) that the maximum voltage error incurred by each error source is  $< q/2$ . It is expected that this probability will be further increased if white Gaussian noise or a more deterministic dither is added to the codec input signal so this seems a reasonable point to terminate the iteration.

The 'zero error' values for  $\mu|g_d|$  and  $\mu|p_d|$  are 3.97% and  $1.32^\circ$  although in general these particular values are of no particular significance and they are not likely to be measured on a near ideal codec. Any variation in measurement conditions, such as small variations in test signal amplitude will give different zero error values and this is easily demonstrated by incorporating a further variable  $\sigma_{14}$  into Program 2. Setting  $\sigma_{14} = 0.01$  for example simulates

the situation where the test signal peak-peak amplitude is within  $\pm 1\%$  of the ideal value (1.07V) for 68% of the measurements and for the above measurement conditions analysis shows that the zero error values will now average 2.7% and  $1.9^\circ$ . The same test signal perturbation applied to the case for  $q/4$  errors gave some change in the p.d.f.'s (see Fig. 6.16) but there is no significant change in the probability integral when integrated over the 6% and  $6^\circ$  limits.

Program 2 also computes the subharmonic to subcarrier ratio for each different set of errors and, as expected, the expected maximum ratio improves as the asymmetry between the analog channels is reduced. The results are given below:-

| rms error  | expected maximum subharmonic to subcarrier ratio, dB |
|------------|------------------------------------------------------|
| $q$        | - 24.3                                               |
| $q/2$      | - 29.2                                               |
| $q/2, q/4$ | - 30.1                                               |
| $q/4$      | - 32.1                                               |

On this analysis it appears that the ratio will be acceptable providing the maximum voltage error incurred by each error source has a high probability (0.95) of being  $< q$ . In this case the expected maximum ratio is approximately - 30dB which means that the subharmonic amplitude is less than the maximum 8-bit quantizing error at the codec output and so should be undetectable on a display.

## 6.2 PROGRAM 3: CROSSCORRELATION ANALYSIS

The Monte Carlo analysis has given an idea of the mean and variance to be expected for differential phase and gain measurements made on codecs which are subject to certain design constraints. The results assume that the

test signal is virtually noise-free. On the other hand, it is well known that even simple dither like white Gaussian noise can give a significant improvement in picture quality so the results of the Monte Carlo analysis should be improved if white noise is added to the test signal. Ideally random noise should have been incorporated into the Monte Carlo analysis but this would have resulted in prohibitably long computer runs. As a compromise, Program 3 computes the differential phase and gain in the codec output as a function of the codec input SNR and this is done for random sets of encoder errors. The conventional 5-riser staircase test signal is applied to the codec model.

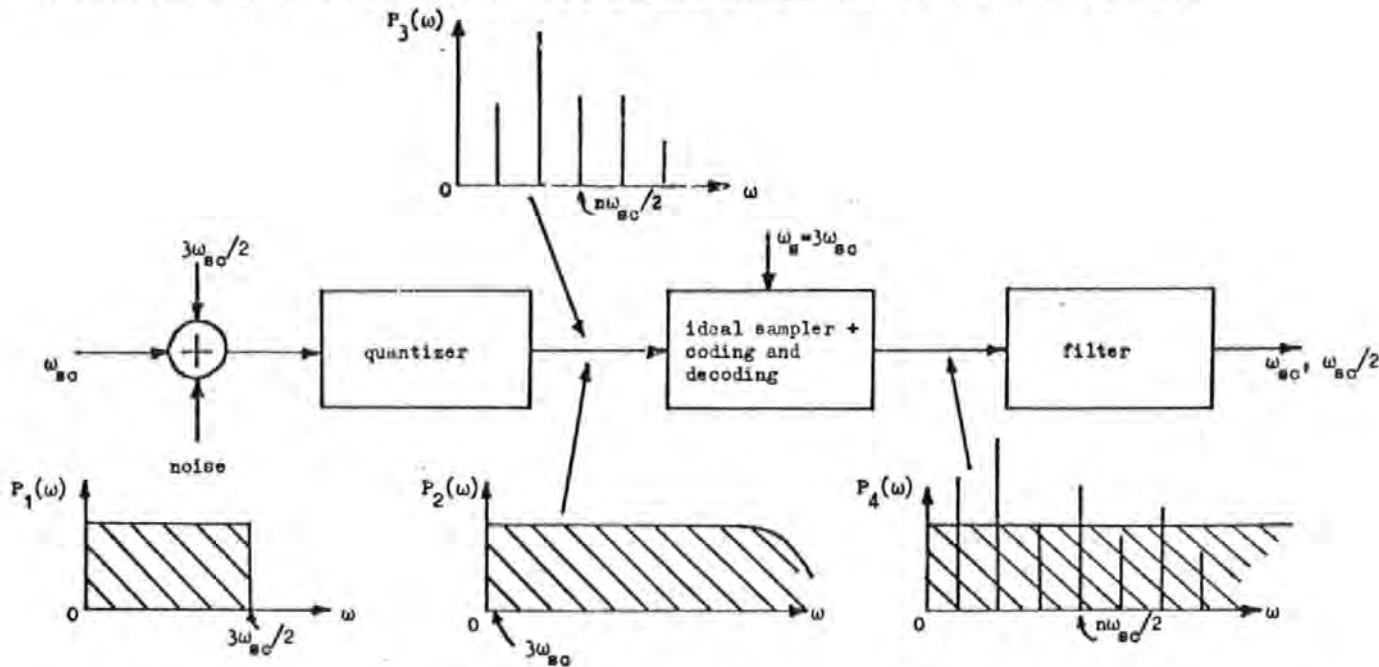


Fig. 6.18: power spectra associated with the practical codec system for a noisy subcarrier input signal.

Assume that the practical codec system with bandlimited white Gaussian noise and subcarrier at its input can be represented by Fig. 6.18. The third input signal is a half sampling frequency component representing asymmetry between analog channels (section 4.1). It is clear that intermodulation and harmonic components generated by the quantizer will give components  $\omega_n = n\omega_{sc}/2, n = 1, 2, 3, \dots$  at the codec output. The power spectrum  $P_2(\omega)$  of a quantized, bandlimited, random signal (noise in this case) was first derived by BENNETT<sup>10</sup> and it is flat well beyond the sampling frequency

as indicated. It follows that the spectrum of the coded output noise can also be considered white so the complete spectrum is quite complex and narrow band filtering is required to separate the subcarrier and its subharmonic.

Computer simulation of the above system is achieved by using the noise model developed in section 5.2 and filtering is achieved by cross-correlation detection. Consider the crosscorrelation function

$$R_{xy}(\tau) = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T x(t - \tau) y(t) dt \quad (6.1)$$

where

$$x(t) = E_r \sin \omega_{sc} t$$

and

$$y(t) = E_0 + E_2 \sin(\omega_{sc} t - \phi_2) + \sum_{m=1,3,4,\dots}^{\infty} [E_m \sin(m\omega_{sc} t/2 - \phi_m)] + e_n(t)$$

$x(t)$  is a subcarrier reference signal and  $y(t)$  represents the unfiltered coded output, with a noise component  $e_n(t)$ . In the limit the crosscorrelation terms tend to zero leaving the autocorrelation function of the subcarrier component on luminance level '1' as

$$\begin{aligned} R(\tau, l) &= \lim_{T \rightarrow \infty} \frac{E_2(l) E_r}{T} \int_0^T \sin \omega_{sc} (t - \tau) \sin(\omega_{sc} t - \phi_2(l)) dt \\ &= \frac{E_2(l) E_r}{2} \cos(\omega_{sc} \tau - \phi_2(l)) \end{aligned} \quad (6.2)$$

The mean subcarrier phase  $\phi_2(l)$  and amplitude  $E_2(l)$  can be found for each luminance step by searching for the peak of  $R_{xy}(\tau)$  and hence the differential phase and gain can be found. The function is found numerically by expressing eqn. (6.1) as

$$R_{xy}(\tau) = \lim_{M \rightarrow \infty} \frac{1}{M} \sum_{k=1}^M x(kt_s - \tau) y(kt_s) \quad (6.3)$$

where  $t_s$  is the sample interval.  $M$  is a compromise between sampling error and computing time and some idea of the value required can be obtained by



considering the residual crosscorrelation terms. In general these terms will vary with luminance level, encoder error and SNR at the codec input so that for negligible sampling error the overall residue should be significantly less than the peak of the required function, eqn. (6.2). A residual term that varies with luminance level has magnitude

$$\left| \frac{E_o E_r}{T} \int_0^T \sin \omega_{sc} (t - \tau) dt \right| \leq \frac{2 E_o E_r}{\omega_{sc} T} \quad (6.4)$$

Similarly the crosscorrelation term for the  $m^{\text{th}}$  component is

$$\left| \frac{E_m E_r}{T} \int_0^T \sin \omega_{sc} (t - \tau) \sin (m \omega_{sc} t / 2 - \phi_m) dt \right| \leq \frac{2 E_r}{\omega_{sc} T} \left| \frac{E_m}{\frac{m^2}{4} - 1} \right| \quad (6.5)$$

Combining all residues so as to form the worst possible combination (but neglecting the residue due to noise) gives a residual error

$$e \leq \frac{2 E_r}{\omega_{sc} T} \left[ E_o + \sum_{m=1,3,4,\dots}^{\infty} \left| \frac{E_m}{\frac{m^2}{4} - 1} \right| \right] \quad (6.6)$$

Fourier components  $E_m$  are unknown but it is reasonable to assume that they are less than the wanted component  $E_2$ . To obtain an estimate of  $M$  we assume  $E_o = E_m \leq E_2$  and eqn. (6.6) reduces to

$$e \leq \frac{53 E_2 E_r}{6 \omega_{sc} T}$$

If the time window extends over  $N$  subcarrier cycles i.e.  $M = 3N$  samples then

$$e \leq \frac{53 E_2 E_r}{4 M \pi}$$

and an estimate of the maximum possible value of the crosscorrelation function is

$$\hat{R}_{xy}(\tau) \leq \frac{E_2 E_r}{2} \left( 1 + \frac{53}{2 \pi M} \right) \quad (6.7)$$

The error in  $E_2$  should preferably be  $< 0.1\%$  for reliable differential gain calculations in which case  $M > 8430$  samples are required. This represents an upper bound since the worst possible combination of errors has been taken. A lower bound might be obtained by simply taking the residue in eqn. (6.4) since this itself is a worst case; for the same error in  $E_2$  we obtain  $M > 1911$  samples or  $M > 955$  samples for  $0.2\%$  error in  $E_2$ .

For a finite value of  $M$  the random noise at the codec output gives rise to an rms error  $\sigma(\tau)$  in the value of the crosscorrelation function. To estimate this error we assume that the wanted signal  $E_2 \sin(\omega_{so} t - \phi_2)$  is to be extracted from a noise component  $e_n(t)$  by crosscorrelation. Therefore

$$\begin{aligned} R_{xy}(\tau) &= \frac{1}{M} \sum_{k=1}^M \left[ E_2 \sin(\omega_{sc} t - \phi_2) + e_n(kt_s) \right] E_r \sin \omega_{sc} (kt_s - \tau) \\ &= A + \frac{1}{M} \sum_{k=1}^M e_n(kt_s) E_r \sin \omega_{sc} (kt_s - \tau) \end{aligned}$$

where  $A$  denotes the constant term (the autocorrelation term) obtained for each computer run. The variance of  $R_{xy}(\tau)$  is

$$\begin{aligned} V[R_{xy}(\tau)] &= V \left[ \frac{1}{M} \sum_{k=1}^M e_n(kt_s) E_r \sin \omega_{sc} (kt_s - \tau) \right] \\ &= V \left[ \frac{1}{M} \sum_{k=1}^M (e_k b_k) \right] \end{aligned}$$

where  $E_r \sin \omega_{sc} (kt_s - \tau)$  is denoted by a constant  $b_k$ ; it is invariant for each computer run unlike the corresponding noise term  $e_k$ . Assuming the terms  $e_k b_k / M$  to be independent random variables then



$$\begin{aligned}
 V[R_{xy}(\tau)] &= \sum_{k=1}^M V(e_k b_k / M) \\
 &= \sum_{k=1}^M \left(\frac{b_k}{M}\right)^2 V(e_k) \\
 &= \left(\frac{\sigma_n}{M}\right)^2 \sum_{k=1}^M [E_r \sin \omega_{sc}(k t_s - \tau)]^2
 \end{aligned}$$

where  $\sigma_n$  denotes the rms value of the codec output noise. Hence, it is certain that

$$\sigma(\tau) < (\sigma_n E_r) / \sqrt{M}$$

and this must be  $< 0.1\%$  of the peak of  $R_{xy}(\tau)$  to obtain the required order of accuracy for a differential gain calculation. Hence

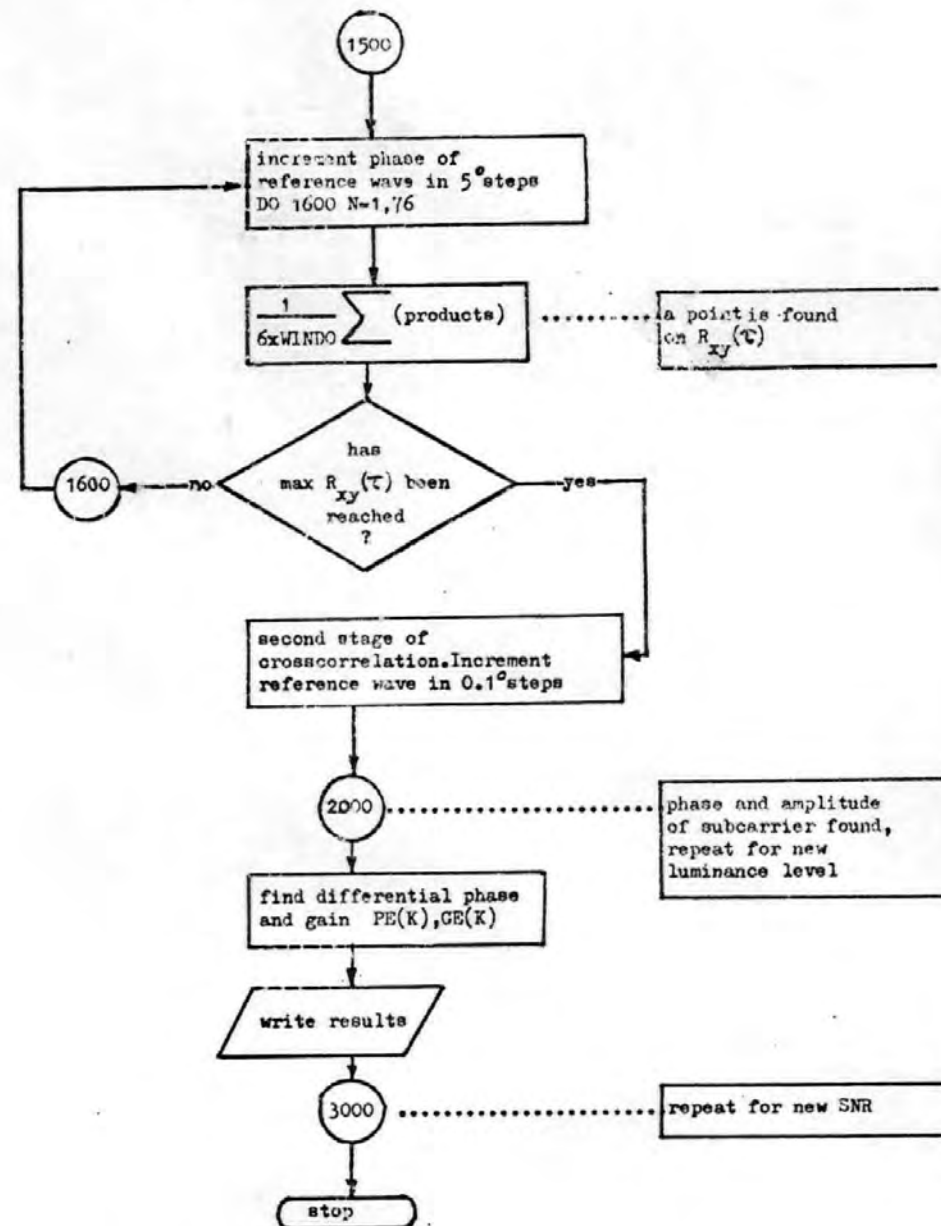
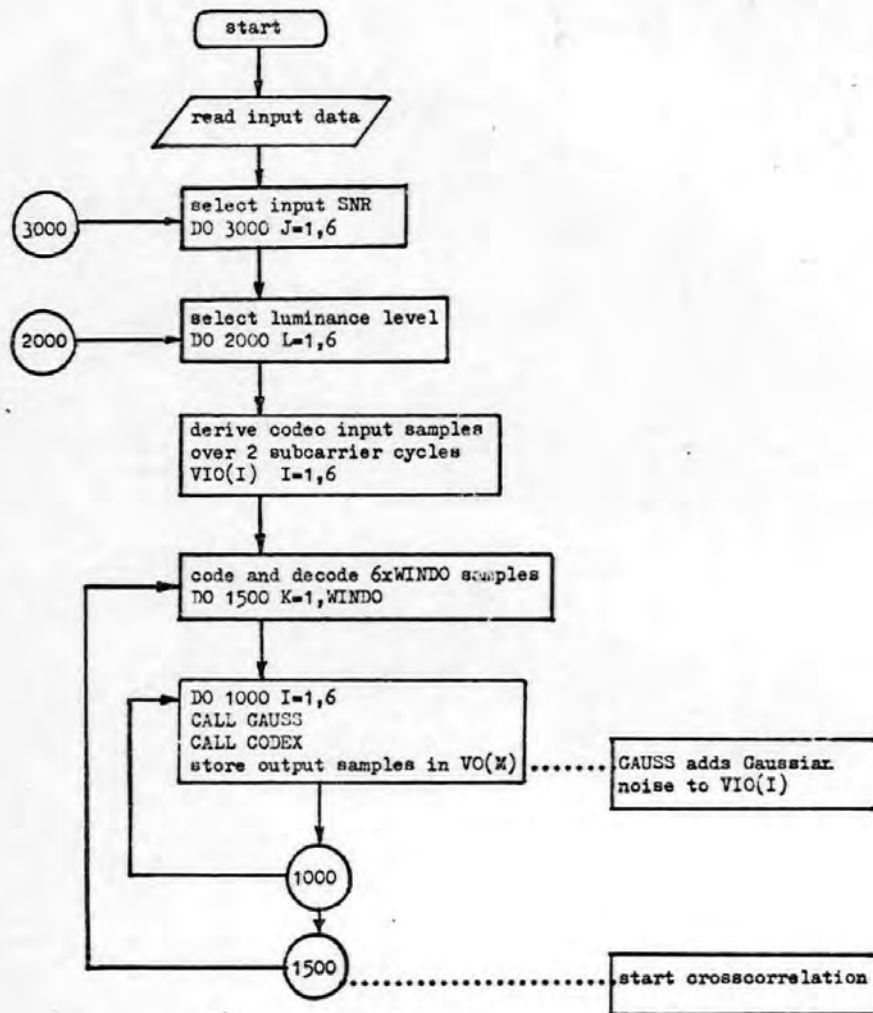
$$\frac{E_2}{2} > 10^3 \sigma_n / \sqrt{M}$$

$$M > 4 \cdot 10^6 \left(\frac{\sigma_n}{E_2}\right)^2 \quad (6.8)$$

This result can also be obtained by considering the mean noise at the codec output. Over  $M$  samples the mean has a 95% chance of falling within the limits  $0 \pm 2 \sigma_n / \sqrt{M}$  (from the central limit theorem) and if the  $2\sigma$  limit is to correspond to less than 0.1% of the subcarrier amplitude  $E_2$  then the number of samples required is given by eqn. (6.8).

To obtain an estimate of  $M$  it is helpful to consider the codec simply as a sampling system (in any case, the contribution of the quantizing noise to  $\sigma_n$  is negligible when the codec input SNR  $< 50\text{dB}$ ). If band limited white Gaussian noise of rms value  $\sigma_{in}$  is sampled by the codec then the noise

Fig. 6.19: Flow chart for Program 3



samples at the codec output will have precisely the same p.d.f. i.e.  $\sigma_n = \sigma_{in}$ . Eqn. (6.8) can now be evaluated for various values of codec input SNR and the results are given in table 6.2, assuming  $E_2 = 70\text{mV}$ .

TABLE 6.2

| codec input SNR, dB | Sample size, M |
|---------------------|----------------|
| 58                  | 634            |
| 52                  | 2535           |
| 46                  | 10,140         |
| 40                  | 40,560         |

The above analysis gives a broad guide as to the size of the crosscorrelation window and some general conclusions can be drawn. Firstly, worst case analysis indicates that a sample size of the order of  $10^4$  is sufficient to reduce all sampling errors to negligible proportions. This is true providing the SNR  $> 45\text{dB}$  approximately but below this value analysis appears to be difficult since the sample size quadruples for every 6dB decrease in the SNR. Looking at the problem more optimistically, (avoiding worst case situations), a sample size of about  $10^3$  might be sufficient to make the effects of changes in encoder error and luminance level negligible, at least for a relatively high SNR.

The FORTRAN program is given in appendix 4 and the program operation is summarised in Fig. 6.19. The input data defines all codec parameters including the specific error(s) that is being simulated. The data also defines the sampling phase, the input SNR, the crosscorrelation window (WINDO) and a random number which initializes the noise generator GAUSS. The simulated input signal is the conventional 5-riser staircase with 140mV peak to peak subcarrier on each luminance step. Six input samples  $VIO(I)$ ,  $I = 1,6$  are selected for the first luminance step, a Gaussian noise component is added

to each sample and the samples are coded and decoded to give a succession of output samples  $VO(M)$ ,  $M = 1, 6 \times \text{WINDO}$ . These samples can now be multiplied by points on the reference sinewave and the products summed to find a value of  $R_{xy}(\tau)$ . The peak in  $R_{xy}(\tau)$  is searched for in two stages to reduce computation time; a coarse search is first made by incrementing the phase of the reference wave in  $5^\circ$  intervals (equivalent to incrementing  $\tau$  in 3.14ns steps). When the peak is located approximately the search increments in  $0.1^\circ$  intervals (63ps steps) so that the subcarrier phase is resolved to within  $\pm 0.05^\circ$  providing sampling errors are negligible, see Fig. 6.20. The whole process is repeated for the remaining luminance steps so that the differential phase and gain can be found.

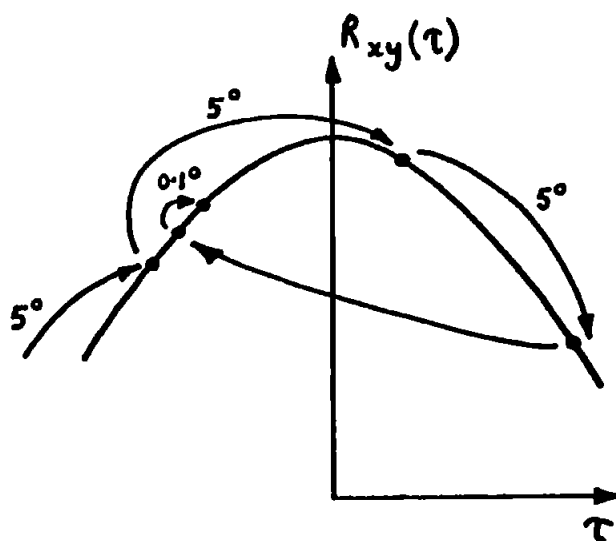
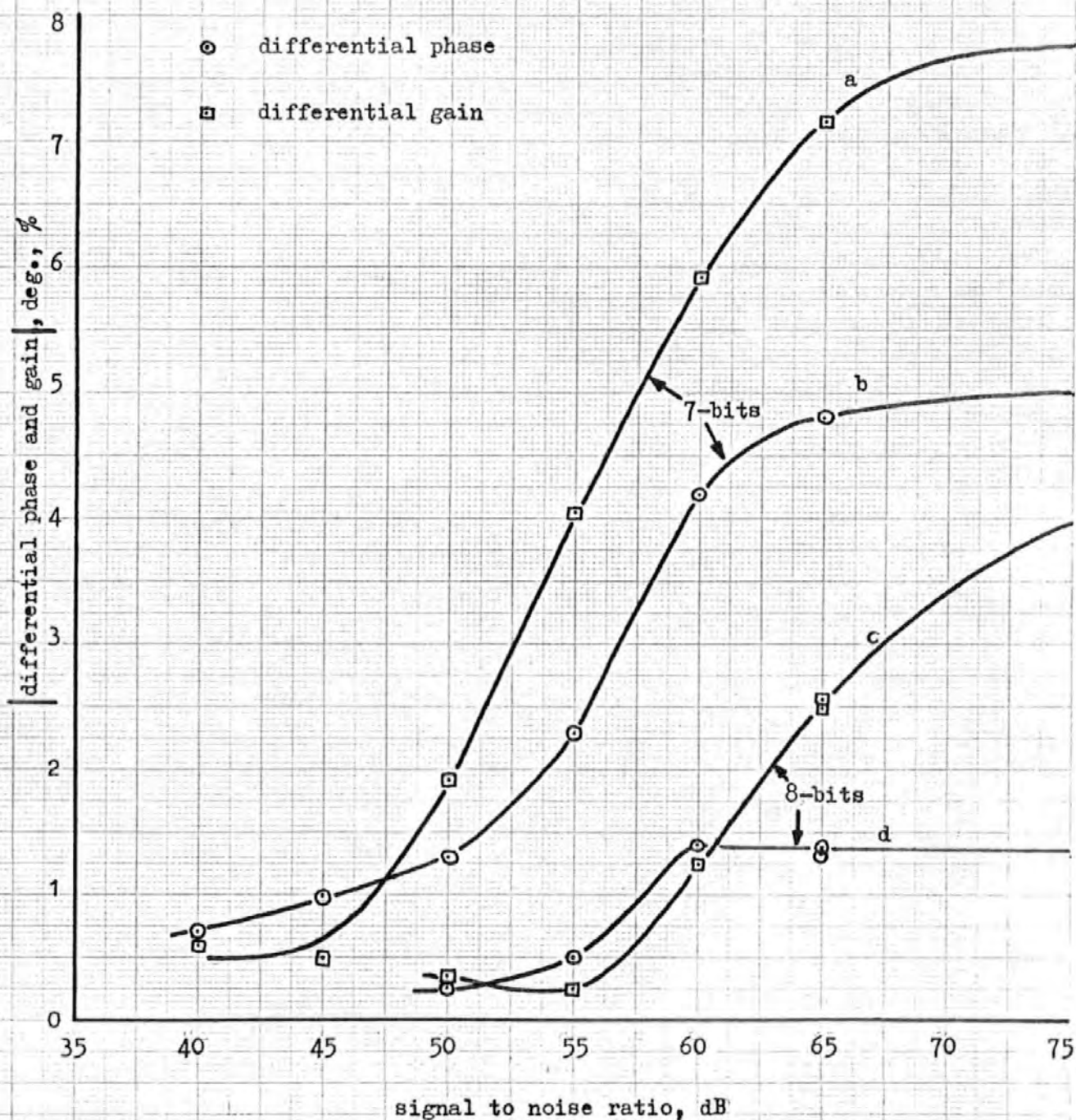


Fig. 6.20: Resolving the peak of the crosscorrelation function

The calculation of the subharmonic amplitude follows a similar procedure and the related steps are omitted from the flow chart for clarity. The subharmonic to subcarrier ratio can be computed as a function of the codec input SNR although to do this thoroughly requires two crosscorrelations, one for the subharmonic and one for the subcarrier. The latter crosscorrelation can be eliminated if the subcarrier output is taken as the ideal output i.e.

$$E_s = 70 S_a(\omega_{sc} t_s/2) = 57.89 \text{ mV}$$

Fig. 6.21: the effect of white Gaussian noise at the codec input upon differential phase and gain arising from quantization. See text for measurement conditions.



This simplifying assumption is reasonable since even if the output subcarrier amplitude varies by 10% the resulting error in the computed subharmonic to subcarrier ratio is still  $< 1\text{dB}$ .

## 6.2.0 RESULTS

In the following analysis the (unweighted) signal to random noise ratio at the codec input is defined as peak luminance (0.7V) to rms noise and it is assumed that 100/0/100/0 colour bars (1.234V peak-peak) just fill the quantizing range. Differential phase and gain is found using the standard test signal (140mV peak-peak subcarrier on a 5-step luminance staircase) and the sampling phase is fixed at  $0^\circ$ .

The objective of this analysis is to assess the effect of random noise as an error reducing mechanism. It was hoped for example that random noise at the codec input would give a useful reduction in subharmonic-subcarrier ratio but in fact the effect is quite small, as observed in practice (section 4.2). Analysis shows that noise merely has the effect of reducing the variance of the ratio with luminance level - typically by a factor 10 as the SNR is reduced to 50dB (a variation with luminance level is of course to be expected when sinusoidal signals are applied to a quantizer).

On the other hand, random noise is found to have a significant effect upon differential phase and gain generated by the codec. Consider first an ideal codec (i.e. the effects of an ideal linear quantizer). The program was used to evaluate the effect of codec input noise upon differential phase and gain generated by quantization (WADE<sup>66</sup>) and the results are given in Fig. 6.21. The sample size was a compromise between low sampling error and low central processor time. For relatively high SNR 600 samples per luminance level gave reasonable results and the sample size was increased to 1800 for low SNR. In the latter case, analysis for one value of SNR (6 luminance levels) corresponds

to 10800 evaluations of the codec model and takes nearly 4 hours on an IBM 1130 computer or over 2 hours on an ICL 1905 computer. The graphs exhibit an upper threshold (particularly for differential phase) above which the error approaches a value depending upon such factors as the sampling phase and upon the positioning of the test signal relative to the quantizing scale (see appendix 2). Since the same conditions were used as in the Monte Carlo analysis the 'zero error' values of 3.97% and  $1.32^\circ$  in Fig. 6.17 provide asymptotes for curves 'c' and 'd' at high SNR.

It is interesting to note that the lower threshold agrees well with DEVEREUX's<sup>31</sup> experiments in which he found that, for a near ideal codec, contouring and beat patterns are virtually eliminated providing the SNR at the codec input is  $< 6n + 5\text{dB}$ , approximately. We can express this lower threshold more fundamentally by considering the probability of an incorrect decision by the comparator. Let  $\sigma_n$  be the rms value of the random noise at the comparator (the noise may be from codec input noise or from the encoder itself). If the input sample coincides with the centre of the quantum ( $E = 0$  in Fig. 6.22) then

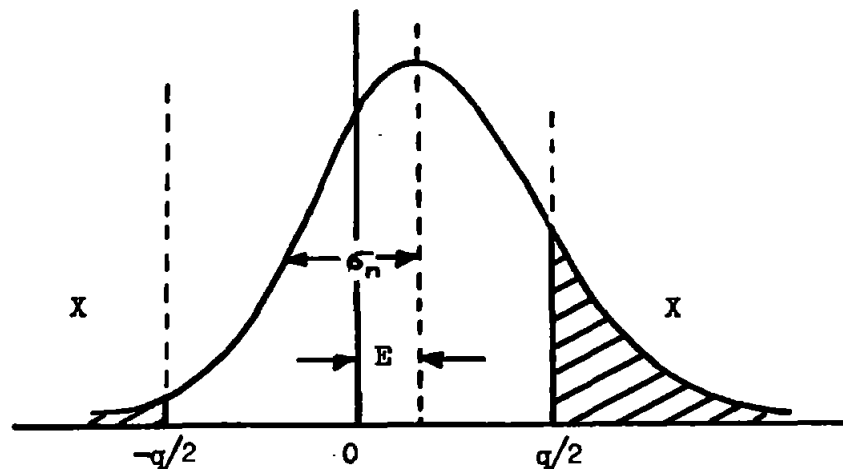


Fig. 6.22: generation of coding error by random noise

the probability of a coding error is



$$p(X) = 1 - \operatorname{erf} \left[ \frac{q/2}{\sigma_n \sqrt{2}} \right]$$

Assuming the masking threshold for the above conditions to be 53dB for  $n = 8$  and that this also represents the SNR at the comparator then  $\sigma_n = 3.8\text{mV}$  and  $p(X) \triangleq 0.15$ . More generally the sample will be displaced an amount  $E$  from the centre so we must define a joint probability

$$p(X, E) = p(E) p(X|E)$$

Therefore

$$p(X) = \int_{-\infty}^{\infty} p(E) p(X|E) dE$$

and assuming a uniform distribution for  $E$

$$p(X) = \frac{1}{q} \int_{-q/2}^{q/2} p(X|E) dE, \quad |E| \leq q/2$$

GORDON<sup>92</sup> has evaluated this integral numerically and inserting the above values into his results gives  $p(X) \triangleq 0.27$ . The lower threshold may now be restated as follows: for the specified conditions, masking of quantizing effects by bandlimited white Gaussian noise is virtually complete provided the noise generates a coding error at least 27% of the time and this is true for all values of  $n$ .

We now extend the analysis to the case of a non-ideal 8-bit codec. Assume for example that random  $q/2$  error is assigned to each of the 13 error sources listed in table 6.1, that is, each error source generates a maximum voltage error of  $q/2$  and the errors are assigned on a random basis, some positive, some negative. Since the errors are chosen at random the results are expected to be typical and one random set should be sufficient (the analysis is

Fig. 6.23(a): the effect of white Gaussian noise at the codec input upon differential phase arising from a random set of  $q/2$  errors in the encoder.

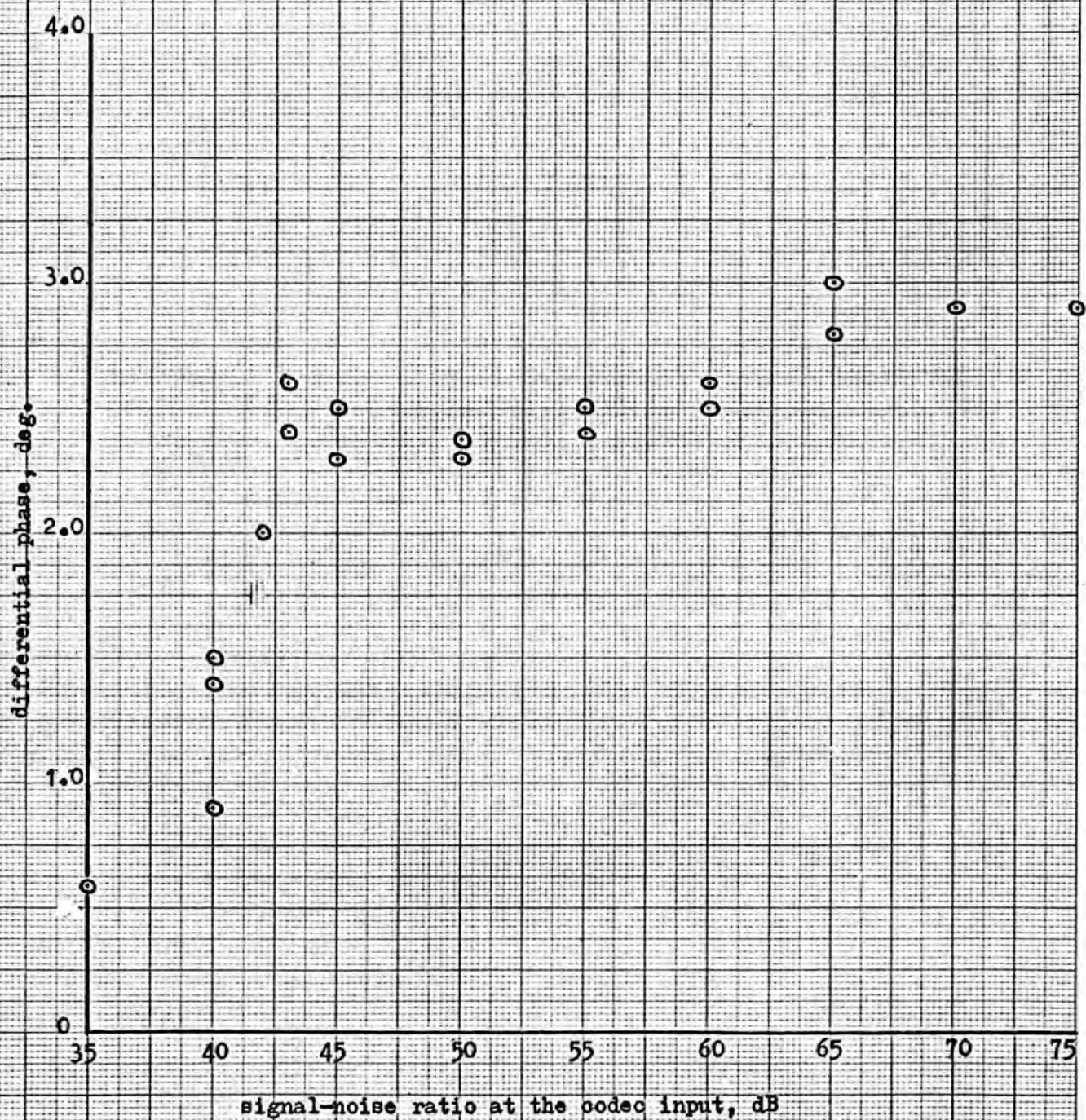
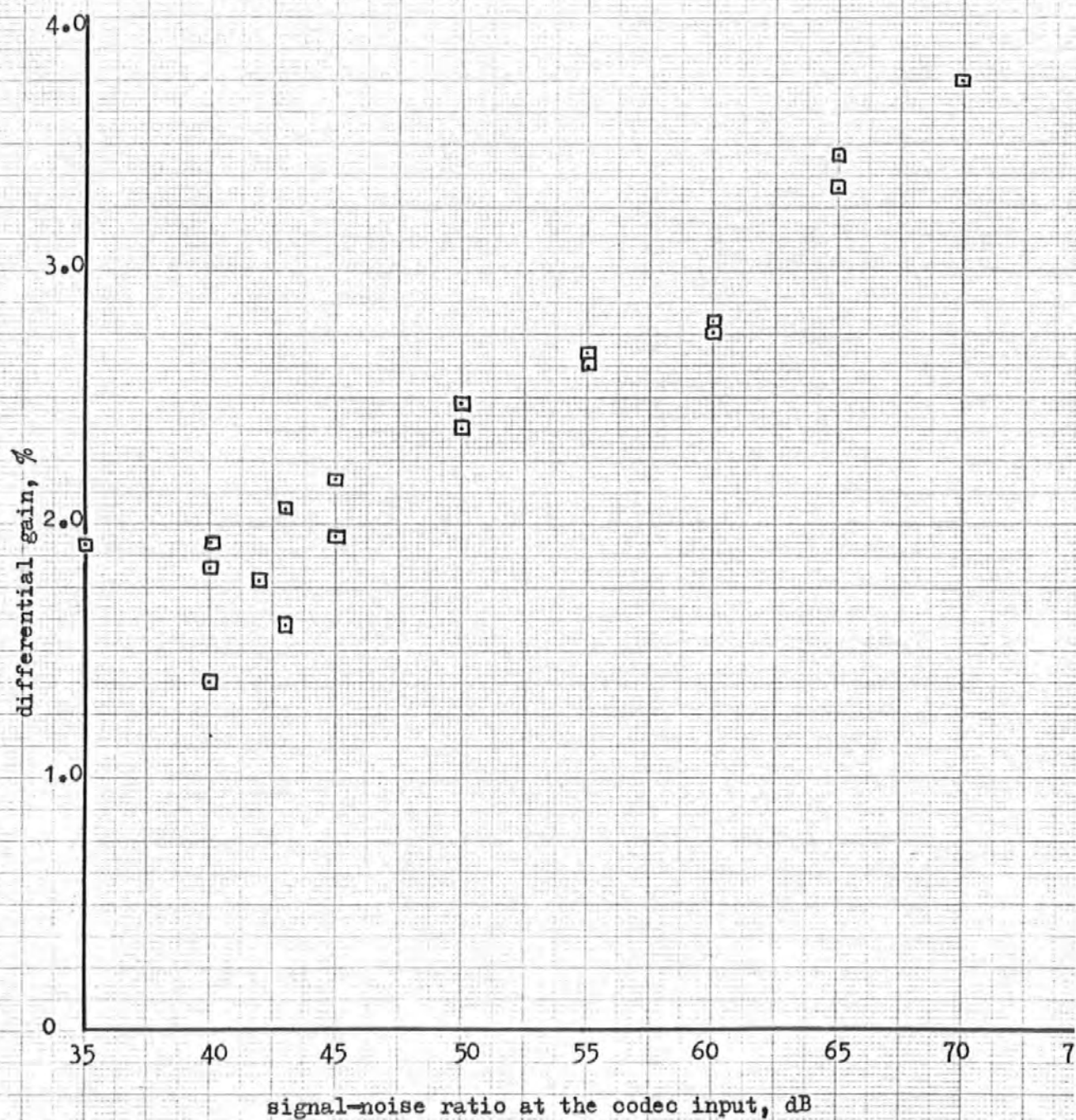


Fig. 6.23(b): the effect of white Gaussian noise at the codec input upon differential gain arising from a random set of  $q/2$  errors in the encoder.



also very expensive in terms of processor time). The following observations can be made from the results in Fig. 6.23:

- (a) sampling error tends to increase at low SNR, as expected.
- (b) there is very significant reduction in differential gain, typically by 50% as the input SNR is reduced to 45dB.
- (c) the reduction in differential phase is less pronounced but there appears to be a threshold (at about 43dB in this case) below which the error decreases more rapidly.

The results imply that the distributions in Figs. 6.13 - 6.16 will be contracted towards the origin by random noise so that the increase in codec output noise is traded for the increased probability of a practical codec falling within the required bounds for differential phase and gain.

### 6.3 SUMMARY

This chapter is a numerical evaluation of the effect of errors and noise in a P.W.M. video encoder and the chapter is summarised as follows:-

1. A triangular wave test is applied to examine the effect of encoder errors upon the static transfer characteristic of the encoder. The test shows the characteristic effect of a number of encoder errors and also that the encoder is particularly susceptible to missed codes at 15 regularly spaced intervals in the quantizing range. It is also concluded that voltage errors in the encoder should be significantly  $< 1q$  for satisfactory dc accuracy.
2. Dynamic errors are investigated by applying a high frequency sine wave (subcarrier) to the codec simulation and observing the phase and gain errors at the filtered codec output. Using differential phase and gain, an attempt is made to determine a circuit design and alignment criterion



such that most practical codecs will fall within specific bounds on these parameters (taken as  $\pm 6^\circ$  and  $\pm 6\%$  respectively). A detailed, but not exhaustive Monte Carlo analysis suggests that the circuit design and alignment should be such that the (maximum) voltage error incurred by each error source should have a high probability (95%) of being  $< q/2$ . With this criterion, and under the assumptions of the analysis, it is probable that 85 - 90% of codecs measured will fall within the above bounds and that the patterning effects due to asymmetrical analog channels will be negligible.

3. A numerical crosscorrelation procedure has been developed for studying the effects of random noise in a codec simulation. Analysis shows that random noise can virtually eliminate the differential phase and gain generated by quantizing error and on average significant reduction in differential phase and gain will also occur even when the encoder possesses significant instrumental error (random voltage errors of the order of  $q/2$ ). Increased random noise at the codec output may therefore be traded for an increased probability of an encoder falling within the above bounds for differential phase and gain and this point is further discussed in section 7.0.

## CHAPTER 7: DISCUSSION AND CONCLUSIONS

It has been shown that there is a useful trade-off between encoder speed and encoder complexity and that encoders of near minimal complexity can now be considered for video encoding. The PWM video encoder studied in this work is considered, in its simplest form, to have about  $1/3$  the complexity of the more highly developed straight PCM video encoders<sup>25</sup> and this improvement is traded for an average increase in circuit speed of 7 or 8 times. In absolute terms this means that the propagation delay per gate must be reduced to 1 or 2ns and this is achieved by exploiting improvements in technology, such as fast logic and higher transistor  $f_T$ .

The prototype encoder is considered to achieve 7-bit resolution at a sample rate of about 13.3MHz and its performance is encouraging, particularly on monochrome signals. On the other hand, full benefit from the speed-complexity trade-off is not yet apparent since implementation involves state of the art techniques and much of the encoder is in discrete component form.

### 7.0 THE ERROR ANALYSIS

The philosophy, achievements and limitations of the numerical error analysis are summarized below, beginning with the assumptions. It is assumed that

1. a practical PWM video encoder will exhibit small, random errors which cause nonlinear distortion of a decoded PAL signal.
2. the encoder errors only affect its static transfer characteristic (dynamic errors such as aperture error and aliasing are neglected).
3. the distortion of the decoded PAL signal can be adequately monitored using only one colour signal parameter (differential phase and gain) and that

this parameter can be adequately measured using the conventional 5-riser staircase test signal.

4. the test signal is (initially) noise free and stable and is sampled in a fixed phase ( $0^\circ$ ).
5. the specification for differential phase and gain in a broadcast quality codec is known<sup>3</sup>.
6. all significant encoder errors leading to error in the static transfer characteristic are known and can be adequately modelled by simple algorithms.
7. each encoder error source can be characterised by a normal probability law  $N(\mu_1, \sigma_1)$ .

The reasons for assuming a normal law are as follows. Firstly, errors of observation or errors of repeated measurement of a given parameter are hypothesised to follow a normal law so that this hypothesis can be applied to any encoder error source which has to be aligned. In other words it is reasonable to assume that there will always be a small alignment error and that this is normally distributed. Errors in ramp amplitude, ramp reference level, quantizer gain, sampling time error, etc., all come into this category since they have to be aligned.

Secondly, any error source that cannot be aligned must be dependent instead upon close tolerance components, and if the components are selected from a combination of many production lots then it is reasonable to assume that they are normally distributed (PINEL and ROBERTS<sup>103</sup>). Taking the example of a clamp level differential, this can be considered to arise from the normally distributed  $V_{oesat}$  of the two clamp transistors. As far as this differential voltage,  $u$ , is concerned, the distributions could have zero mean, and for simplicity we could assume unit variance. Then  $u$  is the difference of two values taken from the same normal distribution



$$u = x - y$$

where  $\rho(x) = \frac{1}{\sqrt{2\pi}} e^{-x^2/2}$ ,  $\rho(y) = \frac{1}{\sqrt{2\pi}} e^{-y^2/2}$

Since  $x, y$  are independent, the joint distribution is

$$\rho(x, y) = \frac{1}{2\pi} e^{-(x^2+y^2)/2}$$

and applying the transformation,  $u = x - y, v = x + y$  gives

$$\begin{aligned} \rho(u, v) &= |J| \cdot \frac{1}{2\pi} e^{-(u^2+v^2)/4} \\ &= \frac{1}{4\pi} e^{-(u^2+v^2)/4} \end{aligned}$$

If this is integrated w.r.t.  $v$  over the limits  $\pm\infty$  we have

$$\rho(u) = \frac{1}{2\sqrt{\pi}} e^{-u^2/4}$$

and so the assumption of a normal law for the clamp level differential is justified.

As a second example we might derive the p.d.f. for the factors  $E_i$ ,  $i = 1, \dots, 4$  which model the binary weighting errors in the 4-bit decoder. Assuming all parameters ideal except the binary weighted resistors  $R_i$  then the modelling factors can be expressed as

$$E_i = \frac{k_i}{R_i} \quad (k_i = \text{constant})$$

Ideally  $E_i$  should be unity but it will spread as  $R_i$  spreads. Let the p.d.f. for  $R_i$  be

$$\rho(R_i) = \frac{1}{\sigma\sqrt{2\pi}} e^{-(R_i-\mu)^2/2\sigma^2}$$

and make the transformation  $E_i = k_i/R_i$ . The Jacobian of the transformation is simply

$$J = \frac{\partial R_i}{\partial E_i} = -\frac{k_i}{E_i^2}$$

thus

$$\begin{aligned} p(E_i) &= |J| \cdot \frac{1}{\sigma\sqrt{2\pi}} e^{-\left(\frac{k_i}{E_i} - \mu\right)^2 / 2\sigma^2} \\ &= \left(\frac{k_i}{\sigma\sqrt{2\pi}}\right) E_i^{-2} e^{-\left(\frac{k_i}{E_i} - \mu\right)^2 / 2\sigma^2} \end{aligned}$$

Inserting a few values shows that  $p(E_i)$  is virtually symmetrical for  $E_i \gtrless 1$  although it is much steeper than a normal distribution. The assumption of a normal distribution for  $E_i$  has therefore resulted in a larger variance in  $E_i$  than would arise solely from variance in  $R_i$  and to represent the effect of  $R_i$  accurately the simplest method is to express the decoder output voltage in terms of  $R_i$ , rather than  $E_i$ . On the other hand, there are other parameters such as the potential across  $R_i$  which will be randomly distributed and in general  $p(E_i)$  is a multivariate function.

Clearly, a normal law is only a convenient approximation to the complex random variations in binary weighting error and the same goes for ramp nonlinearity. In the latter case the philosophy is simply to account for the general case where nonlinearity can be in either sense i.e. a convex or concave ramp. A normal law is convenient because it gives the same probability for either sense of error and it also emphasises the smaller, intuitively more probable errors.

Before discussing the derived design criterion we might comment on the localised peak in the p.d.f.'s of Figs. 6.13 - 6.16. The peak is particularly prominent for differential gain in Fig. 6.16 and it can be explained by the fact that whenever the overall encoder error tends to be small then the (non

zero) differential gain arising from quantization tends to dominate. In the absence of dither and for the measurement conditions used, the peak occurs at 3.97% (and  $1.32^\circ$  for differential phase). Fortunately the peak is expected to lie below the 6% integration limit for most measurement conditions so it should not significantly affect the probability integral.

The design criterion is based upon the requirement that the integral

$$\int_0^{6\%} \int_0^{6^\circ} P|p_d| P|g_d| d|p_d| d|g_d|$$

is acceptably large ( $p_d$  is assumed independent of  $g_d$ ). The iteration was stopped when the joint probability for both differential phase and gain falling within the above limits was 0.86 and it is expected that further improvement in this figure can be obtained by the use of dither. Confirmation of this improvement is provided by the cross-correlation analysis (Fig. 6.23) but in order to estimate the improvement to the above figure of 0.86 it is helpful if we can assign a standard probability law to the functions in Figs. 6.13 - 6.16. These distributions arise from a combination of many (up to 13) independent random normal variables, so taking  $|g_d|$  as an example, we can tentatively express it as

$$|g_d| = \sum_{i=1}^k (z_i^2)$$

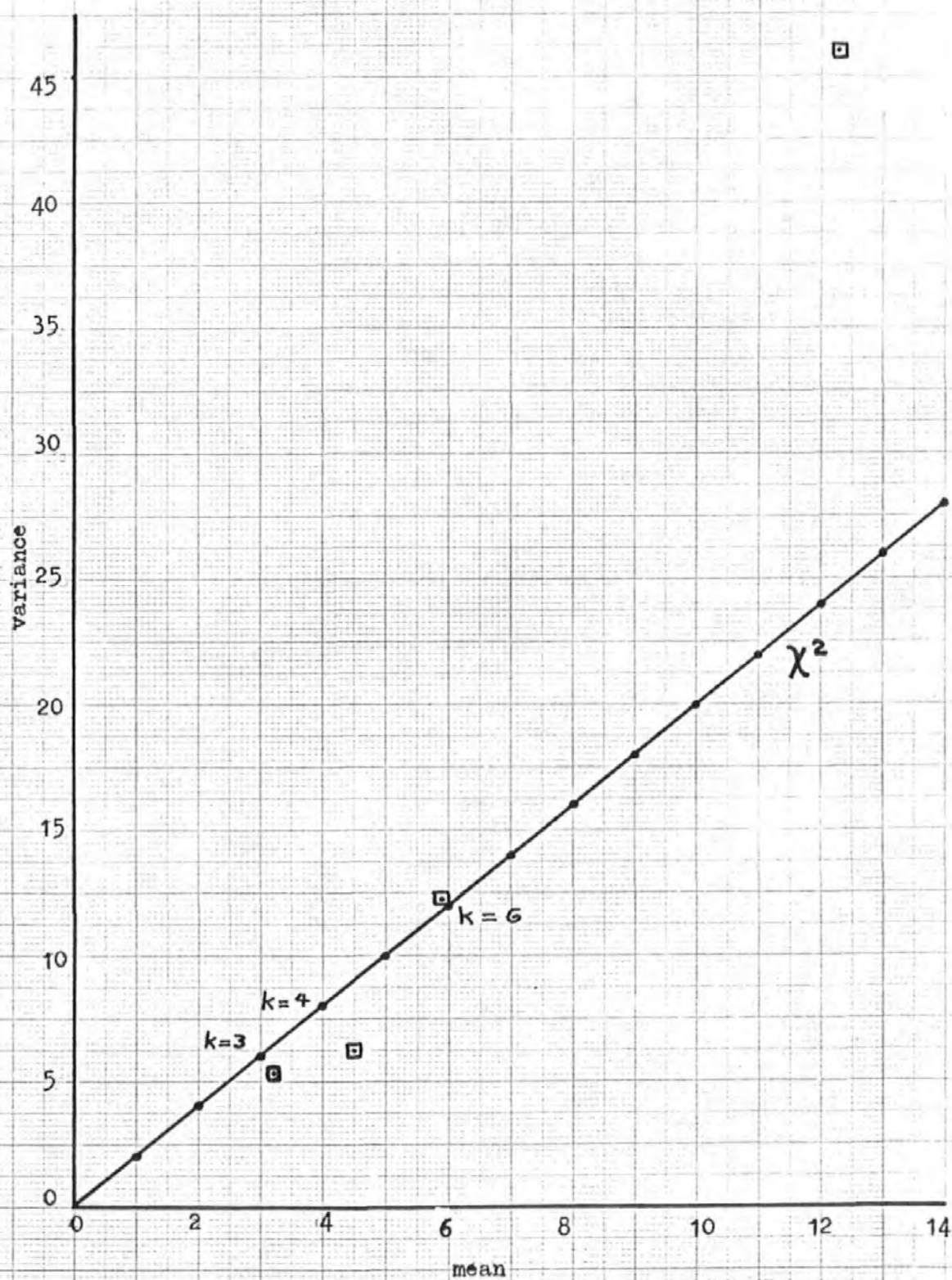
where the  $z_i$  are independent standardized random normal variables  $N(0,1)$ . The p.d.f. of  $|g_d|$  will be recognised as the chi-square distribution i.e.

$$P|g_d| \simeq p(\chi^2) = [2^{k/2} \Gamma(k/2)]^{-1} (\chi^2)^{k/2-1} \cdot e^{-\chi^2/2}, \chi^2 \geq 0$$

and a rough test for a fit is to compare the ratio of variance to mean for the two functions. For  $\chi^2$

$$\frac{V(\chi^2)}{E(\chi^2)} = \frac{2k}{k}$$

Fig. 7.1: mean and variance of  $|g_d|$  in Figs. 6.13 - 6.16  
compared with that for  $\chi^2$



and this is shown in Fig. 7.1 along with the corresponding values for  $|\varepsilon_d|$  obtained from Fig. 6.17. Clearly the  $\chi^2$  distribution is not a particularly good fit since it cannot account for a finite mean at zero variance but on the other hand Figs. 6.14(b) and 6.16 correspond reasonably well with distributions  $\chi^2(6)$  and  $\chi^2(3)$  respectively. Using the  $\chi^2(6)$  distribution the chance of a codec falling within the 6% limit is about 57.6% compared with an estimate of 58% from the histogram and using the  $\chi^2(3)$  distribution gives an 88.5% chance compared with 86% from the histogram.

The fit is considered close enough to enable an estimate of the effect of white noise at the codec input to be made and we start by considering the reduction in differential gain achieved by lowering the unweighted input SNR to, say, 45dB. According to Fig. 6.23(b) the reduction that might be expected when each encoder error source has a random  $q/2$  error is approximately 2% and we might tentatively assume that the mean in Fig. 6.14(b) is likewise improved by 2% since the same order of random error is used in each case. This would reduce the mean in Fig. 6.14(b) to about 4% and using the  $\chi^2(4)$  distribution we find that the probability of a differential gain measurement lying within the 6% limit is now about 80%. This is a very significant improvement upon the figure of 58% without noise, although it is traded for an increase in the random noise at the codec output. Turning to Fig. 6.16, we might reasonably hope for a 1% improvement in mean differential gain by adding white noise and this would reduce the mean to about 2.2%. Using the  $\chi^2(2)$  distribution the chance of a differential gain measurement being within the 6% limit is found to be approximately 95% and this corresponds to an improvement of 8 or 9% over the case without dither.

This analysis is not exhaustive and it is based upon a number of assumptions but nevertheless it is considered sufficiently detailed to enable the following recommendation for the design of a PWM video encoder to be formulated. Quite briefly, it is recommended that the (maximum) voltage error

generated by each encoder error source should have a high probability (95%) of being  $< q/2$  and in practical terms this means for example that any deviation from linearity in each ramp must invariably be  $< 5.8\text{mV}$  and should typically be only a few mV (assuming a 3V quantizing range). Exactly how the error arises need not be rigidly defined; for purposes of assigning a probability law it has been assumed to be due to small alignment errors or finite component tolerance but clearly the effects of temperature and component ageing should also be subject to the above criterion. Subject to the assumptions of the analysis, an encoder designed to the above recommendation would have an 85 - 90% chance of falling within the current differential phase and gain specification for analog video equipment<sup>3</sup> and if simple dither is used this probability may increase to about 95%.

## 7.1 IMPROVEMENTS TO THE PWM VIDEO ENCODER

### 7.1.0 CIRCUIT ASPECTS

The ideal solution would be to integrate all aspects of the encoder and use a bucket-brigade or similar device for the 1 sample period delay. The analog comparator and 4-bit decoder in particular would both benefit from integration since this would reduce drift with temperature variations. On the other hand, if a discrete component comparator is retained, then it is not recommended that the interrogation pulses be applied to the differential amplifier circuit of the comparator. This approach was initially adopted following the work of JOHANNESSEN<sup>26</sup> but it does have the disadvantage that the amplifier is subjected to an extremely high slew-rate, typically  $2\text{kv}/\mu\text{s}$ . In addition, the parasitic capacitance at the comparator input varies as the ramp sweeps the quantizing range and this has an adverse effect upon the interrogation pulse amplitude (see Fig. 3.19). Probably a better approach is to apply the

pulses direct to the tunnel-diode latch as in SCHINDLER's<sup>41</sup> comparator.

It is also recommended that the relative phasing of the interrogation pulses w.r.t. the clock pulses be made adjustable so that the optimal timing of the comparator transition w.r.t. the clock pulses at each AND gate can be achieved. In fact, pre-set adjustments can be inserted into all SRD networks to ease timing alignment.

### 7.1.1 AUTOMATIC ERROR CORRECTION

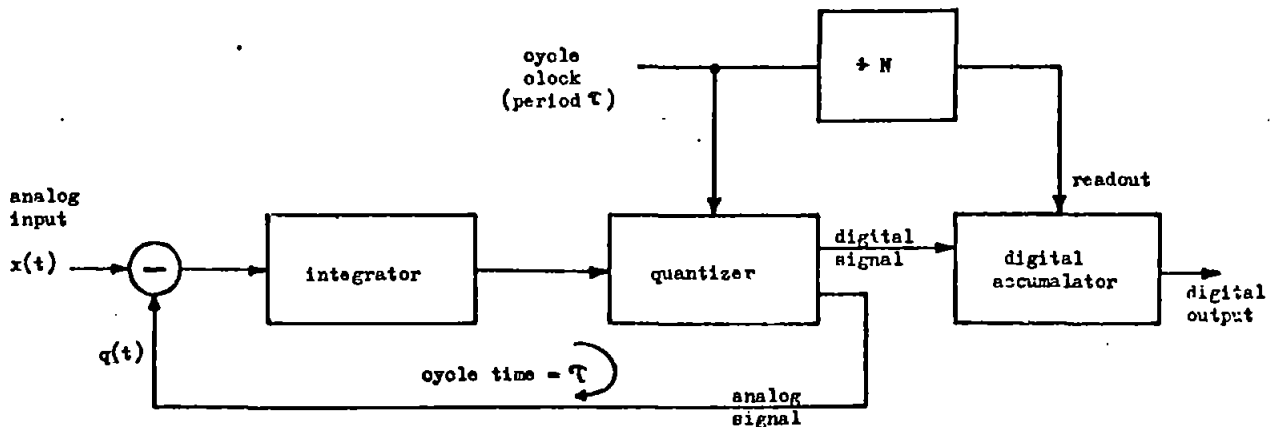


Fig. 7.2: principle of a robust PCM encoder (CANDY<sup>97</sup>)

The error analysis has shown that precision instrumentation is required to realise a broadcast quality PWM video encoder, but less precise instrumentation could be used if some form of automatic error correction is employed. The philosophy is to trade circuit speed and/or complexity for reduced instrumental precision and hence reduced cost.

CANDY<sup>97</sup> has described a low precision 8-bit 'Picturephone' encoder and the principle is illustrated in Fig. 7.2. The basic loop equation is

$$\frac{1}{N} \sum_{n=0}^N q(nT) = \frac{1}{NT} \int_0^{NT} x(t) dt + \frac{e_q(NT)}{N}$$

where  $e_q(NT)$  is the quantizing error associated with the quantizer and it shows that after  $N$  cycles round the feedback loop the average of the quantized



Fig. 7.3:  $v_1$  incorrectly coded as 1101, and appropriate correction.

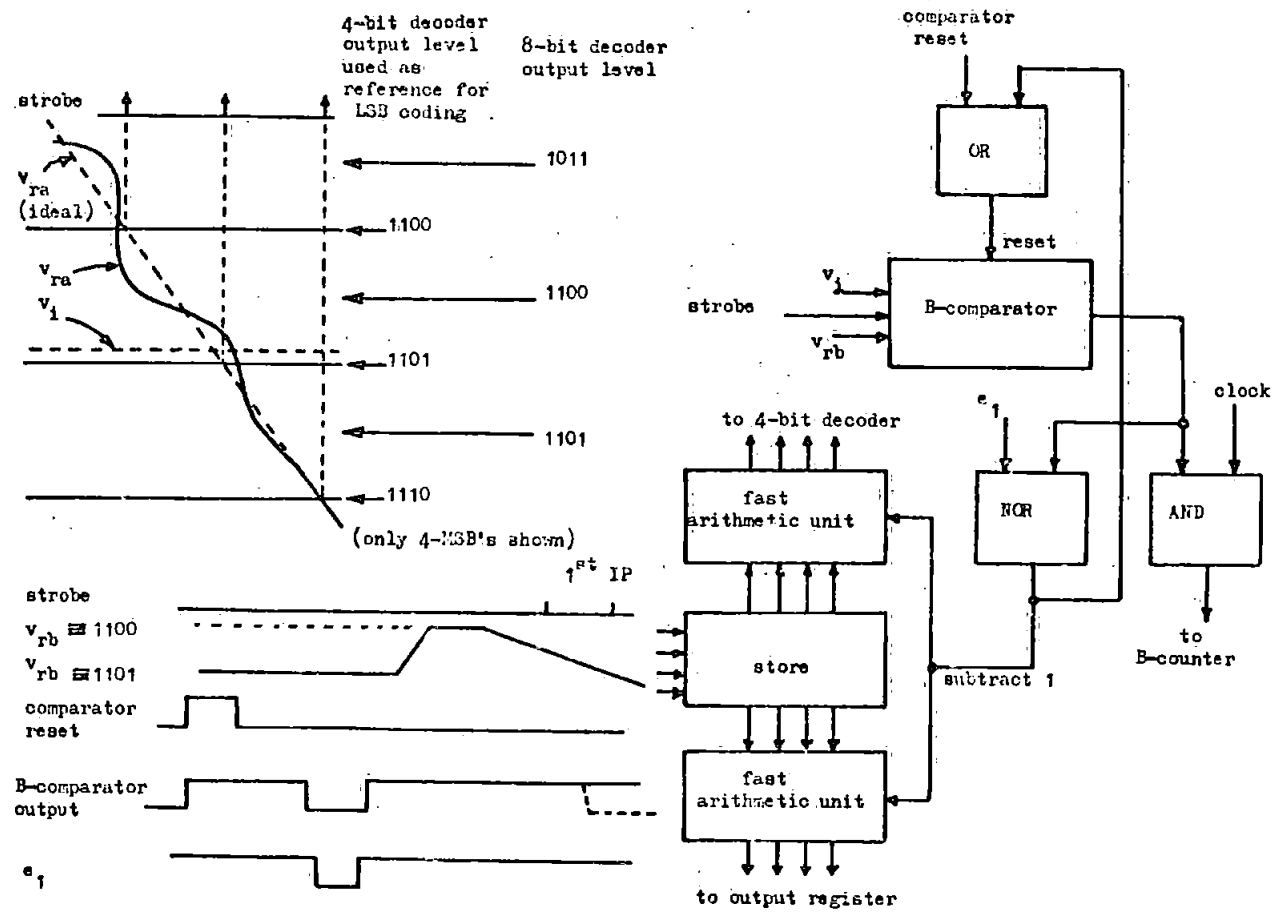
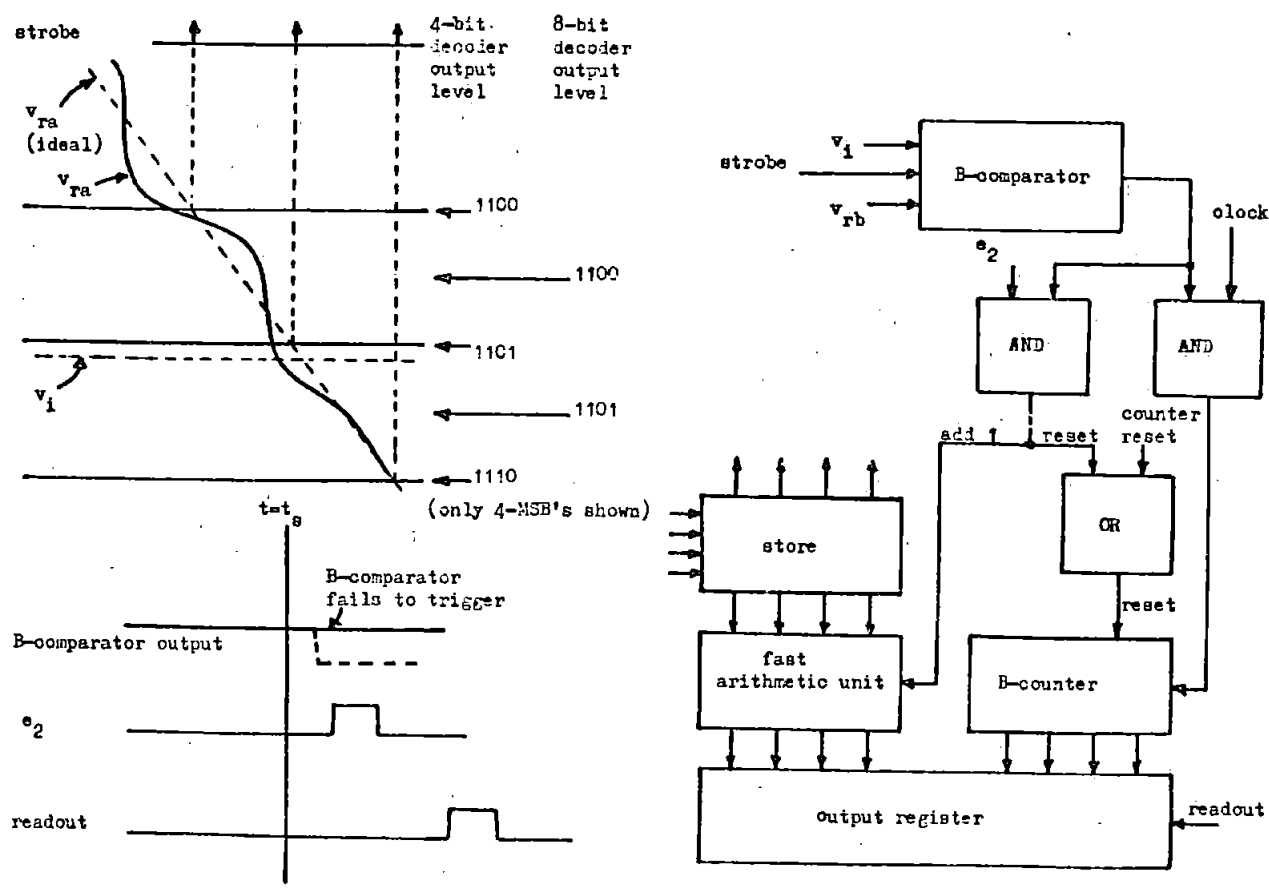


Fig. 7.4:  $v_1$  incorrectly coded as 1100, and appropriate correction.



signals approximates to the average analog input. It follows that the quantizing error from a 4-bit quantizer will be reduced to that of an 8-bit quantizer providing  $N = 16$  and CANDY shows that if the quantizer threshold levels are non-uniformly spaced, due to relaxed precision, the effect is to change a usually sharp discontinuity in the static transfer characteristic (e.g. missed codes) into a 'smoothed' nonlinearity. Instrumental errors are therefore automatically corrected, or at least smoothed, but the technique is probably unsatisfactory for PAL or NTSC signals since chrominance nonlinearity is still retained. In any case, the circuit speed requirements show that implementation is beyond the state of the art since, for a sample rate of 13.3MHz and a 4-bit quantizer, the cycle time must be  $< 5\text{ns}$  to achieve 8-bit resolution.

FLETCHER<sup>101</sup> describes a more realistic error correction technique for broadcast quality codecs in which coding error generated during the generation of the first 4 MSB's is detected and then corrected using fast digital arithmetic. A similar technique can be incorporated into the PWM video encoder as follows.

An analog sample  $v_1$  near a quantizer (comparator) threshold may be coded incorrectly due to noise or an incorrectly set threshold. For the PWM encoder we will assume an incorrect threshold occurs due to a transient on the A-ramp. Considering Fig. 7.3, assume that this local nonlinearity in the A-ramp results in  $v_1$  being coded as 1101 rather than the true value of 1100, so that the quantizing error is  $> q/2$ . The 4-bit decoder will give a reference level such that  $v_{rb} < v_1$  (even before the first interrogation pulse) and this will prematurely trigger the B-comparator as indicated. An error detect pulse  $e_1$  detects this error and the store output is corrected by fast digital arithmetic. Providing the B-comparator is reset it will then be possible to correctly encode  $v_1$  to 8-bits despite the local error in the A-ramp. On the other hand, if  $v_1$  is encoded as 1100 instead of its true value of 1101 (Fig. 7.4) then the

4-bit decoder output level will be too high and the B-comparator will never trigger i.e.  $v_{rb} > v_1$ , always. A second error detect pulse  $e_2$  is used to prematurely zero all 4 LSB's and add 1 to the 4 MSB's before readout in order to give a correction capability of 1 LSB.

Further work along these lines could incorporate both error correction algorithms into the codec model in order to evaluate a new (relaxed) encoder design and alignment criterion. To incorporate both algorithms into a practical encoder we need to relax the timing system shown in Fig. 3.3 and possibilities in this direction are discussed in section 7.1.2.

#### 7.1.2 RELAXING THE TIMING SYSTEM

Broadly speaking, the timing system (Fig. 3.3) comprises a 15ns data transfer period and a 60ns coding period and the main timing problems are associated with the relatively critical transfer, readout, resetting, decoding and sample acquisition processes taking place during the 15ns period. It is therefore of interest to extend this period and this can be achieved, without increasing the encoder complexity, if we reduce the sampling frequency. A factor 2 would give a very significant improvement.

BROWN and KING<sup>34</sup> have shown that for system I PAL signals the sampling frequency could be reduced to 11.9MHz at the expense of more complex pre and post sampling filters, whilst the sampling frequency for an NTSC colour signal sampled at three times subcarrier frequency would be only 10.7MHz, approximately. Also, DEVEREUX and PHILLIPS<sup>102</sup> have extended the work of GOLDING<sup>14</sup> to the sub-Nyquist sampling of PAL signals and they concluded that, in either straight PCM or in DPCM, good picture quality can be maintained for  $f_s = 2f_{so}$  provided pre and post sampling comb filters are used. Table 7.1 shows how these reductions in sampling frequency result in very significant increases in the data transfer period (assuming that the clock frequency is maintained at

approximately 266MHz). Alternatively, for the same 15ns data transfer period, the clock frequency can be reduced as indicated.

TABLE 7.1

| sampling frequency          | data transfer period | clock frequency for 15ns |
|-----------------------------|----------------------|--------------------------|
|                             | for 266MHz clock     | data transfer period     |
| MHZ                         | ns                   | MHZ                      |
| 13.3 (3f <sub>so</sub> PAL) | 15                   | 266                      |
| 11.9 (PAL, system I)        | 24                   | 231                      |
| 10.7 (NTSC)                 | 33                   | 204                      |
| 8.86 (2f <sub>so</sub> PAL) | 53                   | 163                      |

If the sampling frequency is maintained at 13.3MHz, the clock frequency can still be very significantly reduced by using the modified PWM video encoder shown in Fig. 7.5. The coding principle is illustrated in Fig. 7.6 for 8-bits, a constant analog input of +2.280V and a fullscale analog input of +3V. Initially, comparator  $C_1$  decides that the sample is in the upper half of the code raster so a 1 is assigned to the appropriate store data input. Simultaneously the A-ramp is set to start from a nominal voltage reference of  $V_{FS}/2$  (the exact value depends upon the ramp starting time). Comparator  $C_2$  then triggers on the 5<sup>th</sup> strobe pulse and all 4 bits are transferred to the store at the end of the sample period. During the following sample period the input to  $C_4$  is a residue lying between 0 and  $V_{FS}/16$ ; it is 30mV in this case so  $C_3$  assigns a 0 to the appropriate input of the output register and the B-ramp is set to start from nominally 0V. Comparator  $C_4$  triggers on the third strobe pulse so the sample is eventually coded as 11000010.

Clearly, by predetermining the MSB for each set of 4-bits only 7 clock pulses are required per sample period and the clock frequency is approximately halved. A suggested timing system for a 133MHz clock frequency (30th harmonic



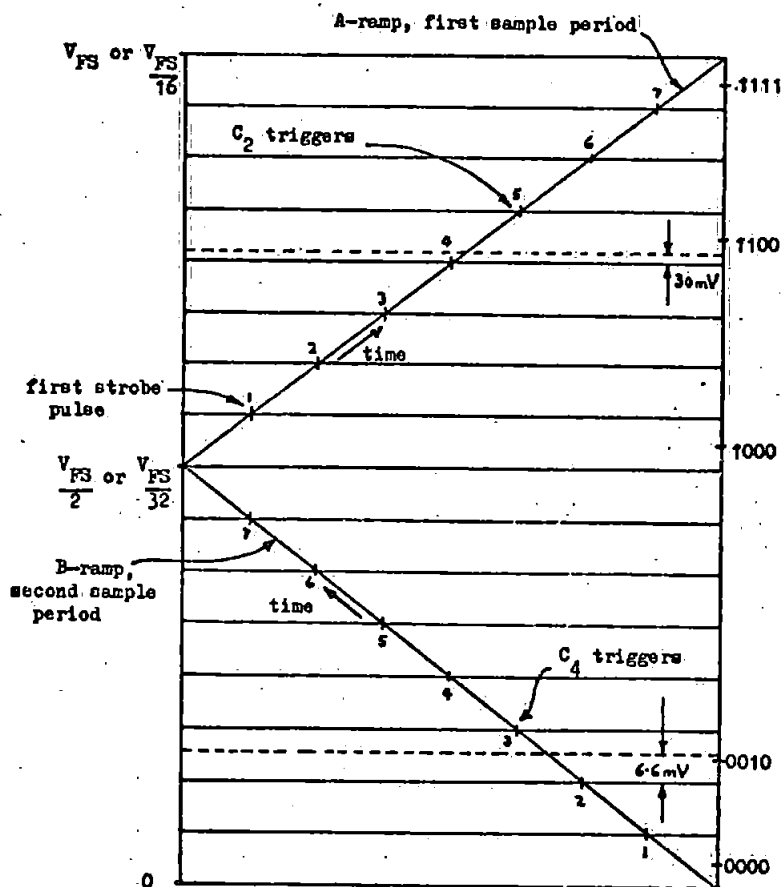


Fig. 7.6: coding example for the modified P.W.M. video encoder  
 (  $v_i = +2.280V$ ,  $V_{FS} = +3V$  )

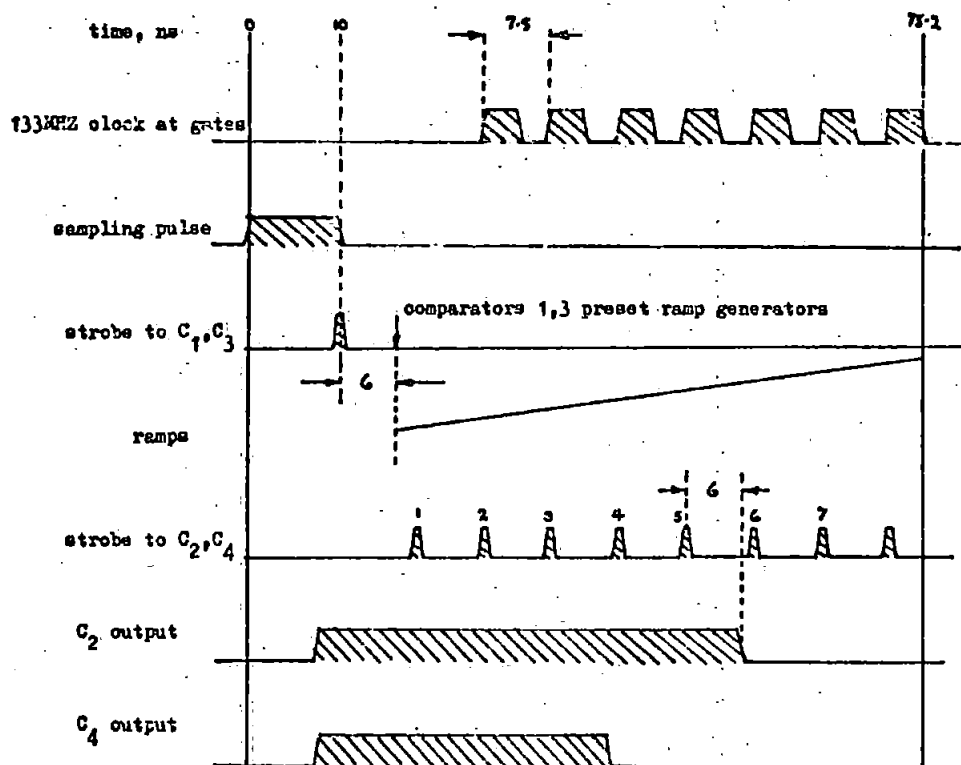


Fig. 7.7: suggested timing system for the modified P.W.M. video encoder  
 ( comparator triggering corresponds to  $v_i = +2.280V$  )

operations is

$$N = c + 2 \sum_{i=1}^{2^k-1} (d_i) = 24 \text{ } \mu\text{o} \quad (k=3)$$

Similarly, the complexity can be written as

$$E = 2(g + b + 2f + 2c + q/2) = 32 \text{ } \mu\text{c}$$

Referring to Fig. 2.9 it will be seen that the modified PWM video encoder (system  $E_2$ ) has about the same complexity as the prototype encoder (system  $E_1$ ) whilst on average the logic speed requirements are relaxed by a factor 2. As previously indicated, this has important practical implications in that advanced IC comparators could probably be incorporated, together with an integrated VCO.

In conclusion, given the problem of simplifying straight PCM video encoders as much as possible, it is evident that systems  $D_2$   $D_3$   $E_1$   $E_2$  and F all have about the same complexity although they differ significantly in speed of operation. System F is considered impractical for broadcast quality video applications, although it could be improved by using a 2-step production line technique - assuming 8-bits per sample this would result in a system located near 32 $\mu\text{o}$ , 40 $\mu\text{o}$ . Systems  $D_2$  and  $D_3$  are probably more viable, particularly system  $D_2$  and both these systems have the advantage that the circuits are repetitive. However, neither of these systems is as digital in nature as systems  $E_1$  and  $E_2$  and in the writer's opinion the latter systems are to be preferred. It has been shown that system  $E_1$  could probably be developed into a broadcast quality encoder although implementation involves state of the art techniques and precision instrumentation. On average system  $E_2$  (Fig. 7.5) has a less critical timing system and if the sampling frequency can be reduced to permit an extended data transfer period (Table 7.1) then automatic error correction methods (section 7.1.1) can be incorporated to realize a more robust PWM video encoder.



## APPENDIX 1

### SWITCHING TIME OF A CURRENT MODE SWITCH

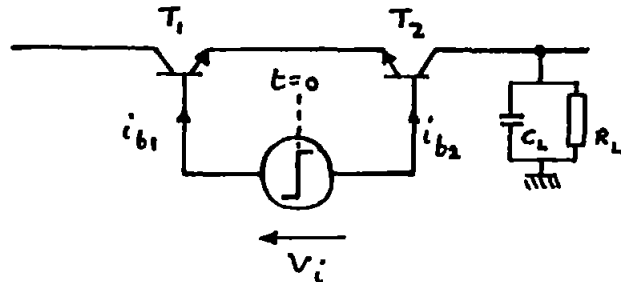


Fig. 1

Neglecting the current required to charge the collector transition capacitance the continuity equation for the instantaneous minority carrier base charge  $q_B$  of a bipolar device is

$$i_b = \frac{dq_B}{dt} + \frac{q_B}{\tau_b}$$

$$= \tau_c \frac{di_c}{dt}$$

- assuming negligible base  
recombination

Charge control theory also shows that  $\tau_c = \omega_T^{-1}$ . Considering Fig. 1, if a step input  $v_i$  is just sufficient to interchange states then during the active region we have

$$\frac{v_i}{s} - V_{be1}(s) + V_{be2}(s) = 0$$

$$\frac{v_i}{s} - 2r i_{b1}(s) = 0$$

where  $r$  is the small signal base-emitter impedance and at high frequencies is approximately given by  $r_{bb}(\omega)$ . Substituting for  $i_{b1}$

$$v_i - \frac{2r \cdot s^2}{\omega_T} \cdot i_{c1}(s) = 0 \quad (i_{c1}(0-) = 0)$$

therefore

$$i_{c1}(t) = \left( \frac{\omega_T v_i}{2r} \right) t$$

If the switched current is  $I_o$  then the 10% - 90% rise time of  $T_1$  collector current is

$$t_r = \frac{1.6 r I_o}{\omega_T v_i}$$

If now  $v_i$  has a finite rise time  $t_{ri}$ , the voltage rise time at  $T_2$  collector is approximately

$$t_r = \left[ t_{ri}^2 + \left( \frac{1.6 r I_o}{\omega_T v_i} \right)^2 + \left( 2.2 C_L R_L \right)^2 \right]^{1/2}$$

SUBCARRIER PHASE AND GAIN ERRORS ARISING FROM QUANTIZATION

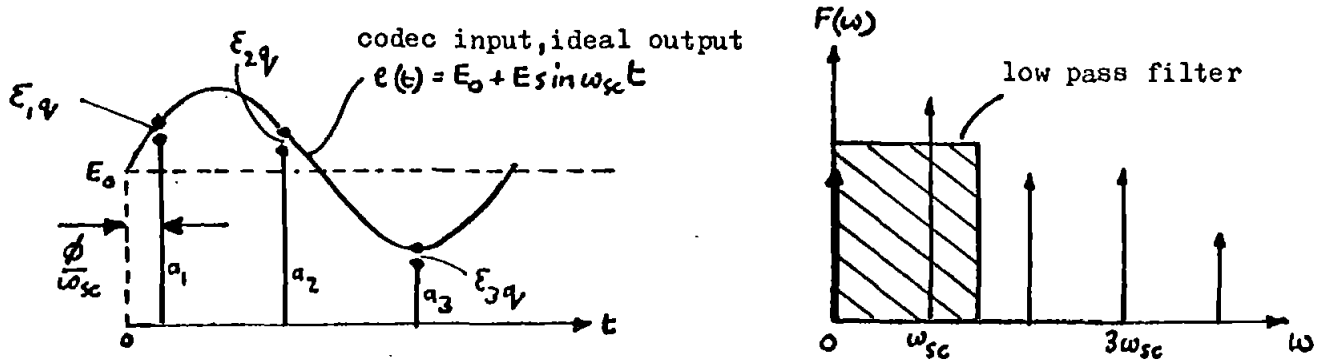


Fig.1: sampled and quantized subcarrier, time and frequency domain

Assume that sampling is at  $3f_{so}$  and that the sampling phase is  $\phi$ . Let  $a_1 a_2 a_3$  be the quantized impulse samples from a codec and  $\epsilon_{1q} \epsilon_{2q} \epsilon_{3q}$  be the corresponding quantizing errors ( $-\frac{1}{2} \leq \epsilon \leq \frac{1}{2}$ ). Using an interpolation filter of cut-off frequency  $3\omega_{so}/2$  the filtered codec output can be written as

$$\sum_{k=1}^{\infty} a_k \text{Sa}[3\omega_{sc}(t - kt_s)/2] = \Delta E_0 + \Delta E \cos(\omega_{sc}t + \theta) + e(t) \quad (1)$$

$\Delta E_0$  is a spurious dc component and  $\Delta E$  is the amplitude of an error wave and both arise from folded subcarrier harmonics generated by quantizing and sampling. Since eqn.(1) represents a sum of orthogonal sampling functions then the peak of each  $a_k$  lies on the output subcarrier and the amplitude of the output subcarrier can be expressed as

$$E' = \frac{1}{3} \left[ (2a_2 - a_1 - a_3)^2 + 3(a_3 - a_1)^2 \right]^{\frac{1}{2}} \quad (2)$$

where

$$a_k = E_0 + E \sin \left[ \phi + \frac{2\pi}{3}(k-1) \right] + \epsilon_k q \quad k=1,2,3$$

For a sampling phase  $\phi = 0^\circ$  then

Eqn. (2) reduces to

$$E' = \frac{1}{3} \left[ \left( \frac{3E\sqrt{3}}{2} + 2\varepsilon_2 q - \varepsilon_1 q - \varepsilon_3 q \right)^2 + 3 \left( \varepsilon_3 q - \varepsilon_1 q - \frac{\sqrt{3}}{2} E \right)^2 \right]^{\frac{1}{2}}$$

which is of the form

$$E' = \frac{1}{3} \left[ (\alpha + f_1(\varepsilon))^2 + (\beta + f_2(\varepsilon))^2 \right]^{\frac{1}{2}} \quad (3)$$

Considering eqn. (3) as the addition of two vectors,  $\vec{\alpha} + \vec{\beta}$  corresponding to the ideal subcarrier output, and  $\vec{f_1(\varepsilon)} + \vec{f_2(\varepsilon)}$  corresponding to the error wave we have

$$\begin{aligned} \Delta E &= \frac{1}{3} \left[ f_1^2(\varepsilon) + f_2^2(\varepsilon) \right]^{\frac{1}{2}} \\ &= \frac{q}{3} \left[ (2\varepsilon_2 - \varepsilon_1 - \varepsilon_3)^2 + 3(\varepsilon_3 - \varepsilon_1)^2 \right]^{\frac{1}{2}} \\ &= \frac{2q}{3} \left[ \varepsilon_1^2 + \varepsilon_2^2 + \varepsilon_3^2 - \varepsilon_1 \varepsilon_3 - \varepsilon_1 \varepsilon_2 - \varepsilon_2 \varepsilon_3 \right]^{\frac{1}{2}} \end{aligned}$$

$\Delta E$  is a maximum when  $\varepsilon = \pm \frac{1}{2}$  for one sample and  $\mp \frac{1}{2}$  for the other two samples so that

$$\Delta E_{\max} = 2q/3$$

The maximum phase and gain errors measured relative to the ideal subcarrier output can be found by considering the vector sum  $\vec{E} + \vec{2q/3}$ . For a full scale codec input  $V_{FS}$  and  $n$  bits per sample the phase and gain errors are respectively

$$\begin{aligned} \rho_e &\leq \pm \sin^{-1} \left( \frac{2V_{FS}}{3 \cdot 2^n E} \right) && \text{deg} \\ g_e &\leq \pm \left( \frac{200}{3 \cdot 2^n} \right) \frac{V_{FS}}{E} && \% \end{aligned}$$

These relations are summarised below for  $E = 70\text{mV}$  and  $V_{FS} = 1.234\text{V}$  (corresponding to 100/0/100/0 colour bars).

| n | max. gain error % | max. phase error, $\pm$ deg |
|---|-------------------|-----------------------------|
| 7 | 9.18              | 5°16'                       |
| 8 | 4.59              | 2°38'                       |
| 9 | 2.295             | 1°19'                       |

It is well known that the harmonic amplitudes for a quantized sinusoid can vary abruptly for very small changes in mean level or wave amplitude and both the amplitude and phase of the filtered subcarrier are expected to behave similarly. To illustrate this effect the values of  $p_e$  and  $g_e$  were computed and plotted as a function of luminance level, Fig. 2. The mathematical model of the codec was made ideal so that the phase and gain errors arise entirely from 8-bit quantization (i.e. they are measured relative to an unquantized codec output,  $n \rightarrow \infty$ ). The sampling phase, subcarrier amplitude and full scale codec input all correspond to the values used in the Monte Carlo and crosscorrelation investigations (Figs. 6.17 and 6.21 respectively).

Fig. 2 shows the abrupt changes with luminance level (neglecting plotter interpolation errors between 0.2mV luminance increments) and clearly shows how the differential phase and gain errors in Figs. 6.17 and 6.21 relate to the more fundamental concept of 'quantizing phase and gain errors'. Variation of the sampling phase gives different patterns although the errors are always within the theoretical bounds. According to the bounds for  $n = 8$ , it is just possible for the differential phase and gain to be about 5° and 9% respectively but these extreme values are of little practical consequence since the PAL system is relatively tolerant of such errors and anyway the errors tend to be eliminated by dither.

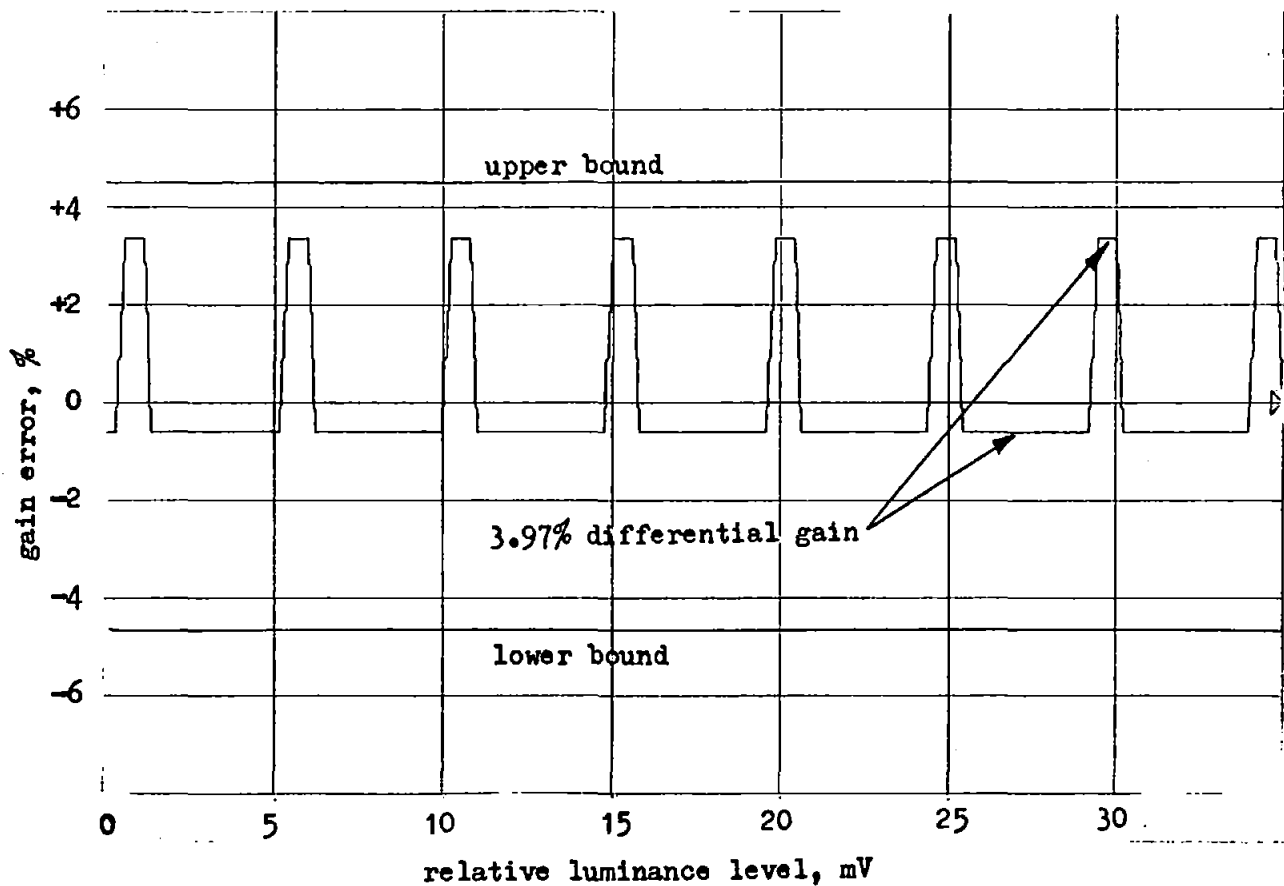
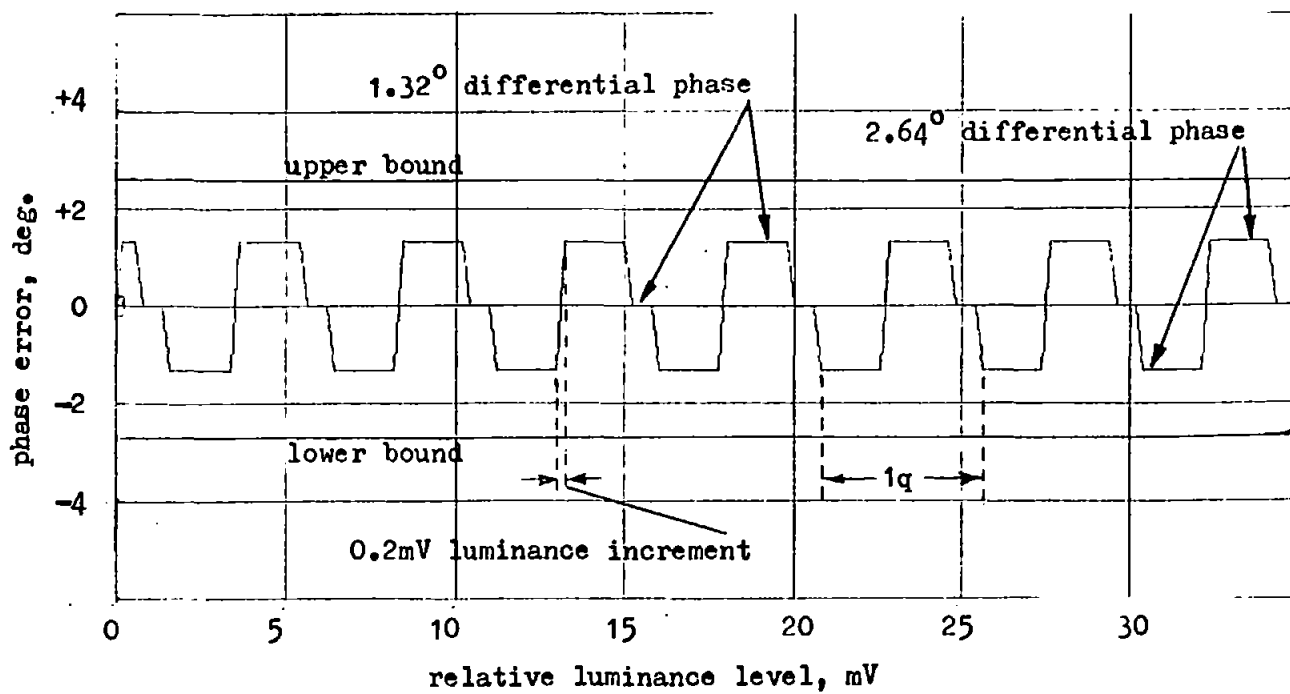


Fig. 2: computed subcarrier phase and gain error arising from quantization as a function of luminance level ( $E = 70\text{mV}$ ,  $V_{FS} = 1234\text{mV}$ ,  $n = 8$ ,  $1q = 4.82\text{mV}$ , sampling phase =  $0^\circ$ ).

### APPENDIX 3

#### FOURIER ANALYSIS OF THE NOISE-FREE CODEC OUTPUT

If the codec output is noise-free then the subcarrier and its subharmonic can be filtered from the codec output using Fourier analysis. The output updates virtually instantaneously so that it will have the general form shown in Fig. 1.

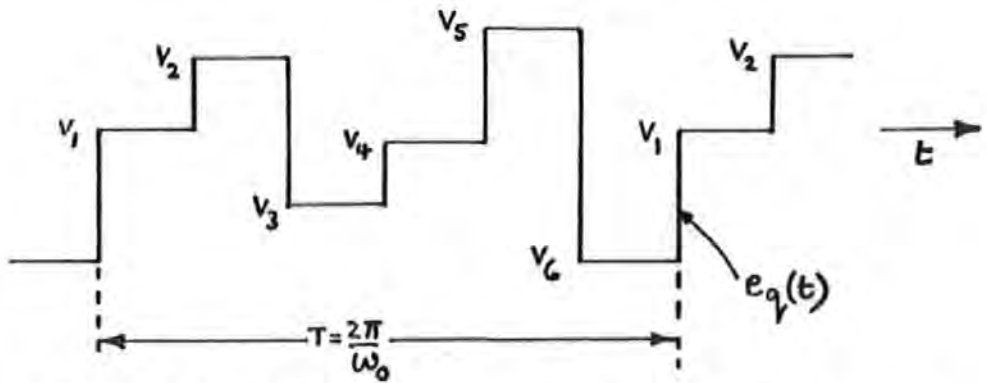


Fig. 1: Generalised codec output for subcarrier input

$e_q(t)$  has a fundamental component  $\omega_{sc}/2$ , designated  $\omega_0$

$$\begin{aligned} \therefore e_q(t) &= \sum_{k=-\infty}^{\infty} F_k e^{jk\omega_0 t} \\ &= F_0 + 2 \sum_{k=1}^{\infty} |F_k| \cos(k\omega_0 t - \phi_k), \quad 0 < t < T \end{aligned}$$

where 
$$F_k = \frac{1}{T} \int_0^T e_q(t) e^{-jk\omega_0 t} dt$$

$$\phi_k = \tan^{-1}(-R_k/I_k)$$

and  $I_k$  and  $R_k$  are the real and imaginary components of  $2\pi F_k$ . The required components are

$$e_1 = 2|F_1| \cos(\omega_0 t - \phi_1)$$

$$e_2 = 2|F_2| \cos(2\omega_0 t - \phi_2)$$



$$\begin{aligned}
 \therefore F_k &= \frac{V_1}{T} \int_0^{T/6} e^{-jk\omega_0 t} dt + \frac{V_2}{T} \int_{T/6}^{T/3} e^{-jk\omega_0 t} dt + \frac{V_3}{T} \int_{T/3}^{T/2} e^{-jk\omega_0 t} dt \\
 &\quad + \frac{V_4}{T} \int_{T/2}^{2T/3} e^{-jk\omega_0 t} dt + \frac{V_5}{T} \int_{2T/3}^{5T/6} e^{-jk\omega_0 t} dt + \frac{V_6}{T} \int_{5T/6}^T e^{-jk\omega_0 t} dt \\
 &= \frac{j}{2k\pi} \left[ (V_1 - V_2) e^{-jk\omega_0 T/6} + (V_2 - V_3) e^{-jk\omega_0 T/3} + (V_3 - V_4) e^{-jk\omega_0 T/2} \right. \\
 &\quad \left. + (V_4 - V_5) e^{-jk\omega_0 2T/3} + (V_5 - V_6) e^{-jk\omega_0 5T/6} + (V_6 - V_1) \right]
 \end{aligned}$$

letting  $k = 1$

$$\begin{aligned}
 F_1 &= \frac{j}{2\pi} \left[ (V_1 - V_2) e^{-j\pi/3} + (V_2 - V_3) e^{-j2\pi/3} + (V_3 - V_4) e^{-j\pi} \right. \\
 &\quad \left. + (V_4 - V_5) e^{-j4\pi/3} + (V_5 - V_6) e^{-j5\pi/3} + (V_6 - V_1) \right]
 \end{aligned}$$

which can be expressed in the form

$$F_1 = \frac{1}{2\pi} (I_1 + jR_1)$$

$$\text{where } I_1 = \frac{\sqrt{3}}{2} (V_1 + V_6 - V_4 - V_3)$$

$$R_1 = V_5 - V_2 + \frac{1}{2} (V_6 + V_4 - V_1 - V_3)$$

Similarly, for  $k = 2$

$$\begin{aligned}
 F_2 &= \frac{j}{4\pi} \left[ (V_1 - V_2) e^{-j2\pi/3} + (V_2 - V_3) e^{-j4\pi/3} + (V_3 - V_4) e^{-j2\pi} \right. \\
 &\quad \left. + (V_4 - V_5) e^{-j8\pi/3} + (V_5 - V_6) e^{-j10\pi/3} + (V_6 - V_1) \right]
 \end{aligned}$$

$$\therefore F_2 = \frac{1}{4\pi} (I_2 + jR_2)$$

$$\text{where } I_2 = \frac{\sqrt{3}}{2} (V_1 - 2V_2 + V_3 + V_4 - 2V_5 + V_6)$$

$$R_2 = V_6 + V_3 - V_4 - V_1 - \frac{1}{2} (V_1 + V_4 - V_3 - V_6)$$

# MATHEMATICAL MODEL OF CODEC

```

SUBROUTINE CODEX(G,GBX,GBY,VCX,VCY,VOA,VOB,VIP,AMPA,AMPB,OSCA,
60SCB,FR,GQ,RE,E1,E2,E3,E4)
INTEGER D1,D2,D3,D4,D5,D6,D7,D8,BITNO
COMMON VI(6),I,TC,TS,W,WM,BITNO,NUM,DA,GDEC
GOTO(106,105,106,105,106,105),I
105 VIC = VCY-G*GBY*VI(I)
GOTO 108
106 VIC = VCX-G*GBX*VI(I)
108 IF (VIC-3) 110,120,120
110 NUM= NUM+1
120 D1=0
D2=0
D3=0
D4=0
D5=0
D6=0
D7=0
D8=0
DO 160 K=1,16
IF (K-3) 125,125,126
125 RAMPE=RE*(K**0.5)
GOTO 128
126 RAMPE=1.732*RE*(1.-(K-3.)/13.)
128 TL=K*TC
VRA=VOA-VIP-K*AMPA*0.0625+OSCA*SIN(W*TL)*EXP(-TL/(4*TC))
6+RAMPE*AMPA
IF (VRA-VIC) 131,150,150
C ABOVE STATEMENT SIMULATES A-COMPARATOR, MSB CODING FOLLOWS
131 GOTO (200,132,133,134,135,136,137,138,139,140,141,142,143,144,
6145,146),K
132 D4=1
GOTO 200
133 D3=1
GOTO 200
134 D3=1
D4=1
GOTO 200
135 D2=1
GOTO 200
136 D2=1
D4=1
GOTO 200
137 D2=1

```

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D3=1
GOTO 200
138 D2=1
D3=1
D4=1
GOTO 200
139 D1=1
GOTO 200
140 D1=1
D4=1
GOTO 200
141 D1=1
D3=1
GOTO 200
142 D1=1
D3=1
D4=1
GOTO 200
143 D1=1
D2=1
GOTO 200
144 D1=1
D2=1
D4=1
GOTO 200
145 D1=1
D2=1
D3=1
GOTO 200
146 D1=1
D2=1
D3=1
D4=1
GOTO 200
150 IF (K-16) 160,170,160
160 CONTINUE
170 D1=1
D2=1
D3=1
D4=1
200 IF (BITNO - 4) 300,300,210
210 VB=GQ*(F1*D1*0.5+E2*D2*0.25+E3*D3*0.125+E4*D4*0.0625)
C SETTING E1=1.001 SIMULATES -0.1( ERROR IN CURRENT SOURCE
DO 260 L=1,16
IF (L-3) 220,220,222
220 RAMPE=RE*(L**0.5)
GOTO 225
222 RAMPE=1.732*RE*(1.-(L-3.)/13.)
225 TL=L*TC
VRB=VOB-VIP-VB-L*AMPB*0.0625+OSCB*SIN(W*TL)*EXP(-TL/(4*TC))
6+RAMPE*AMPB
IF (VRB-VIC) 231,250,250
C ABOVE STATEMENT SIMULATES B-COMPARATOR, LSB CODING FOLLOWS
231 GOTO (300,232,233,234,235,236,237,238,239,240,241,242,243,244,
6245,246),L
232 D8=1
GOTO 300
233 D7=1

```

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GOTO 300
234 D7=1
    D8=1
    GOTO 300
235 D6 = 1
    GOTO 300
236 D6=1
    D8=1
    GOTO 300
237 D6=1
    D7=1
    GOTO 300
238 D6=1
    D7=1
    D8=1
    GOTO 300
239 D5=1
    GOTO 300
240 D5=1
    D8=1
    GOTO 300
241 D5=1
    D7=1
    GOTO 300
242 D5=1
    D7=1
    D8=1
    GOTO 300
243 D5=1
    D6=1
    GOTO 300
244 D5=1
    D6=1
    D8=1
    GOTO 300
245 D5=1
    D6=1
    D7=1
    GOTO 300
246 D5=1
    D6=1
    D7=1
    D8=1
    GOTO 300
250 IF (L-16) 260,270,260
260 CONTINUE
270 D5=1
    D6 =1
    D7 =1
    D8 =1
300 GOTO (301,302,303,400,305,306,307,400),BITNO
301 D2 = 0
    D3 = 0
    D4 = 0
    GOTO 400
302 D3 = 0
    D4 = 0
    GOTO 400

```

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303 D4 = 0
    GOTO 400
305 D6 = 0
    D7 = 0
    D8 = 0
    GOTO 400
306 D7 = 0
    D8 = 0
    GOTO 400
307 D8 = 0
400 DA=GDEC*(D1*0.5+D2*0.25+D3*0.125+D4*0.0625+D5/32.+D6/64.+D7/128.
    6+D8/256.)
    RETURN
    END

```

```

C   THIS PROGRAM DETERMINES THE EFFECT OF ENCODER ERRORS UPON A
C   CODED AND DECODED 625 LINE COMPOSITE RAMP
      INTEGER BITNO,DB
      6, PROG
      COMMON V1(853),VDA(853),TC,W,BITNO
      6, PROG
      READ (2,5) GAIN,GBX,GBY,VCX,VCY,VOA,VOB,VIP,AMPA,AMPB,OSCA,
      6 OSCB,FR,GQ,RE,E1,E2,E3,E4
      5   FORMAT (8F10.4)
      READ (2,6) BITNO,DB,IX
      C   IX IS AN ODD POSITIVE INTEGER LESS THAN 32,768
      6   FORMAT (5I10)
      PROG=2
      RMSNZ = 0.7/(10**((DB/20.0)))
      PI=3.14159265
      TS=1/(3*4.433619*.1E7)
      TC=0.05*TS
      WSC=2*PI*4.433619*.1E7
      WM=3*PI*4.433619*.1E7
      W=2*PI*FR*.1E7
      DO 10 N1=1,19
      N=N1
      10  VI(N)=0.3
      VI(20)=0.225
      VI(21)=0.150
      VI(22)=0.075
      DO 20 N2=1,59
      N=22+N2
      20  VI(N)=0
      VI(82)=0.075
      VI(83)=0.150
      VI(84)=0.225
      DO 30 N3=1,77
      N=84+N3
      30  VI(N)=0.3
      DO 40 N4 =1,692
      N=161+N4
      40  VI(N)=0.3 + 0.7*N4/692
      IF (DB-100) 11,15,11
      11  DO 14 I=1,853
      CALL GAUSS(IX,RMSNZ,VI(I),V)
      C   IX IS USED AS AN INPUT AND OUTPUT PARAMETER
      14  VI(I) = V
      C   VI(I) NOW HAS A RANDOM GAUSSIAN NOISE COMPONENT
      15  CALL CODEC(GAIN,GBX,GBY,VCX,VCY,VOA,VOB,VIP,AMPA,AMPB,OSCA,
      6 OSCB,FR,GQ,RE,E1,E2,E3,E4)
      C   EACH SAMPLE,N, HAS BEEN CODED AND DECODED
      WRITE (3,560)
      560  FORMAT (//,' CODEC VIDEO OUTPUT AVAILABLE')
      CALL SCFOR(1,7.,7.,0.,0.)
      CALL SCFOR(3,0.,70.,7.,0.)
      CALL SCFOR(4,0.,1.4,7.,0.)
      CALL FPLLOT(-2,0.,0.)
      DO 900 N=1,853
      T= (N-1)*TS*.1E7
      900  CALL FPLLOT (0,T,VDA(N))
      CALL FPLLOT(1,0.,0.)
      CALL FPLLOT(0,120.,0.)
      WRITE(3,1003)
      1003  FORMAT('1INPUT DATA')
      WRITE(3,1005) BITNO,DB
      1005  FORMAT(//,' BITNO= ',I1,10X,'DB= ',I3)
      WRITE(3,1007) GAIN,GBX,GBY,VCX,VCY,VOA,VOB,VIP
      1007  FORMAT(//,' GAIN= ',F5.3,5X,'GBX= ',F5.3,5X,'GBY= ',F5.3,5X,
      6 'VCX= ',F5.3,5X,'VCY= ',F5.3,5X,'VOA= ',F5.3,5X,'VOB= ',
      6 'F5.3,5X,'VIP= ',F5.3)
      WRITE(3,1009) AMPA,AMPB,OSCA,OSCB,FR,GQ,RE
      1009  FORMAT(//,'AMPA= ',F5.3,5X,'AMPB= ',F6.4,5X,'OSCA= ',F5.3,5X,
      6 'OSCB= ',F5.3,5X,'FR= ',F6.1,5X,'GQ= ',F5.3,5X,'RE= ',F5.3)
      WRITE(3,1011) E1,E2,E3,E4
      1011  FORMAT(//,' E1= ',F5.3,5X,'E2= ',F5.3,5X,'E3= ',F5.3,5X,'E4= ',F
      65.3)
      CALL EXIT
      END

```

```

C THIS PROGRAM ESTIMATES THE MEAN DIFF. PHASE AND GAIN AND THE
C MEAN SUBHARMONIC THAT MIGHT BE MEASURED ON CODECS SELECTED FROM
C A PRODUCTION LINE. DIFFERENT CODECS ARE SIMULATED BY MONTE
C CARLO SAMPLING OF CODEC ERRORS.
REAL I1,I2
INTEGER BITNO,SIZE,PHI,HISTP(72),HISTG(72)
DIMENSION VDA(6),AMP2(6),PHASE(6),DIFPE(1000),DIFGE(1000)
6,RMAX(1000),R(6),AMP1(6)
COMMON VI(6),I,TC,TS,W,WM,BITNO,NUM,DA,GDEC
READ(2,4) S1,S2,S3,S4,S5,S6,S7,S8,S9,S10,S11,S12,S13,S14
4 FORMAT(8F10.4)
READ(2,6) BITNO,PHI,SIZE,IX
6 FORMAT(4I10)
C SIZE IS SAMPLE SIZE,IX ANY ODD INTEGER LESS THAN 32,768
GAIN=3./((1.234*0.95)
FR=300.
PI=3.14159265
TS=1/(3*4.433619*.1E7)
TC=0.05*TS
WSC=2*PI*4.433619*.1E7
WM=3*PI*4.433619*.1E7
W=2*PI*FR*.1E7
GDEC = 1.234
VPK=0.07
RAD=PHI*PI/180.
SUMR=0.
SUMPE=0.
SUMGE=0.
DEVPE=0.
DEVGE=0.
NUM=0
OSCB=0.
VIP=1.5
DO 8 K=1,36
8 HISTP(K)=0
E3=1.0
E4=1.0
WRITE(3,10)
10 FORMAT('DIFF PHASE',5X,'DIFF GAIN')
DO 1000 N=1,SIZE
RMAX(N)=0.
C ASSIGN RANDOM VALUE TO EACH CODER VARIABLE
CALL GAUSS(IX,S14,0.95,GBX)
CALL GAUSS(IX,S1,GBX,GBY)
CALL GAUSS(IX,S2,6.0,VCX)
CALL GAUSS(IX,S3,VCX,VCY)
CALL GAUSS(IX,S4,7.5,VOA)
CALL GAUSS(IX,S5,7.5,VOB)
CALL GAUSS(IX,S6,3.0,AMPA)
CALL GAUSS(IX,S7,0.1875,AMPB)
CALL GAUSS(IX,S8,0.0,OSCA)
CALL GAUSS(IX,S9,0.0,RE)
CALL GAUSS(IX,S10,3.0,GQ)
CALL GAUSS(IX,S11,0.,DET)
CALL GAUSS(IX,S12,1.0,E1)
CALL GAUSS(IX,S13,1.0,E2)
DO 40 LL=1,6
PED= (LL-2)*0.14
VI(1)=VPK*SIN(RAD)+ 0.44+ PED
VI(2)=VPK*SIN(RAD+2*PI/3.+WSC*DET/.1E10)+0.44+PED
VI(3)=VPK*SIN(RAD+4*PI/3.)+0.44+PED
VI(4)=VPK*SIN(RAD+WSC*DET/.1E10)+0.44+PED
VI(5)=VPK*SIN(RAD+2*PI/3.)+0.44+PED
VI(6)=VPK*SIN(RAD+4*PI/3.+WSC*DET/.1E10)+0.44+PE)
DO 30 I=1,6
CALL CODEX(GAIN,GBX,GBY,VCX,VCY,VOA,VOB,VIP,AMPA,AMPB,OSCA,
6OSCB,FR,GQ,RE,E1,E2,E3,E4)
30 VDA(I)=DA
C SIX OUTPUTS FOUND FOR SPECIFIED LUMINANCE STEP
I2=SQRT(3.)*(VDA(1)-2*VDA(2)+VDA(3)+VDA(4)+VDA(6)-2*VDA(5))/2.
R2= VDA(6)+VDA(3)-VDA(4)-VDA(1)-(VDA(1)+VDA(4)-VDA(3)-VDA(6))/2.
AMP2(LL)= (SQRT(I2*I2+R2*R2))/(2.*PI)
I1=SQRT(3.)*(VDA(1)+VDA(6)-VDA(4)-VDA(3))/2.
R1=VDA(5)-VDA(2)+(VDA(6)+VDA(4)-VDA(1)-VDA(3))/2.
AMP1(LL)=(SQRT(I1*I1+R1*R1))/PI
R(LL)=AMP1(LL)/AMP2(LL)
IF (R(LL)-RMAX(N)) 32,32,31
31 RMAX(N) = R(LL)
32 IF (I2) 34,33,34
33 PHASE(LL) = 90.
GOTO 40

```

```

34 PHASE(LL) = ABS((ATAN(-P2/I2))*180./PI)
40 CONTINUE
C PHASE AND AMP OF SUBCARRIER OUTPUT FOUND FOR EACH LUMINANCE STEP
C AND MAX SUBHARMONIC/SUBCARRIER RATIO FOUND FOR NTH RANDOM SET
DIFPE(N) = ABS(PHASE(2) - PHASE(1))
DIFGE(N) = ABS(AMP2(2) - AMP2(1))*100./AMP2(1)
DO 75 KK=3,6
A = ABS(PHASE(KK)-PHASE(1))
IF (A-DIFPE(N)) 65,65,60
60 DIFPE(N) = A
65 B = ABS(AMP2(KK) - AMP2(1))*100./AMP2(1)
IF (B-DIFGE(N)) 75,75,70
70 DIFGE(N) = B
75 CONTINUE
DO 78 II=1,36
IF (DIFPE(N)-II*0.5) 77,77,78
77 HISTP(II)=HISTP(II)+1
GOTO 80
78 CONTINUE
80 DO 85 MM=1,36
IF (DIFGE(N)-MM*0.5) 82,82,85
82 HISTG(MM)=HISTG(MM)+1
GOTO 90
85 CONTINUE
90 SUMPE=SUMPE+DIFPE(N)
SUMGE = SUMGE +DIFGE(N)
WRITE(3,800) DIFPE(N), DIFGE(N)
800 FORMAT(/,2X,F7.2,9X,F7.2)
SUMR=SUMR+RMAX(N)
1000 CONTINUE
C ESTIMATE EXPECTED DIFF PHASE(GAIN)
AVPE = SUMPE/SIZE
AVGE = SUMGE/SIZE
DO 1050 N=1,SIZE
DEVPE = DEVPE +(DIFPE(N)-AVPE)**2
1050 DEVGE = DEVGE +(DIFGE(N)-AVGE)**2
C ESTIMATE POPULATION STD. DEVIATIONS
STDPE=SQRT(DEVPE/(SIZE-1))
STDGE=SQRT(DEVGE/(SIZE-1))
WRITE(3,1080) NUM
1080 FORMAT(/,' OVERLOAD COUNT = ',110)
WRITE(3,1085)
1085 FORMAT(/,' PHASE HISTOGRAM',10X,'GAIN HISTOGRAM')
DO 1090 NN=1,36
1090 WRITE(3,1095) HISTP(NN),HISTG(NN)
1095 FORMAT(/,5X,14,20X,14)
IF (SUMR) 1097,1097,1096
1096 EXPDB= 20*(ALOG(SUMR/N)/ALOG(10.))
GOTO 1098
1097 EXPDB=-100.
1098 WRITE(3,1099) EXPDB
1099 FORMAT(/,' EXPECTED MAX SUBHARMONIC-SUBCARRIER RATIO= ',F6.1,'DB')
WRITE(3,1100) AVPE
1100 FORMAT(/,' EXPECTED DIFF PHASE ERROR=',F6.1,' DEGREES')
WRITE(3,1110) AVGE
1110 FORMAT(/,' EXPECTED DIFFERENTIAL GAIN ERROR=',F6.1,' PERCENT')
WRITE(3,1130) STDPE
1130 FORMAT(/,' DIFFERENTIAL PHASE STANDARD DEVIATION=',F6.1)
WRITE(3,1140) STDGE
1140 FORMAT(/,' DIFFERENTIAL GAIN STANDARD DEVIATION=',F6.1)
WRITE(3,1154)
1154 FORMAT(/,' INPUT DATA')
WRITE(3,1156) BITNO,SIZE,PHI
1156 FORMAT(/,' BITNO=',11,5X,'SAMPLE SIZE=',14,
65X,'SAMPLING PHASE = ',13)
WRITE(3,1158) S1,S2,S3,S4,S5,S6,S14
1158 FORMAT(/,' S1=',F6.4,5X,'S2=',F6.4,5X,'S3=',F6.4,5X,'S4=',F6.4,
65X,'S5=',F6.4,5X,'S6=',F6.4,5X,'S14=',F6.4)
WRITE(3,1159) S7,S8,S9,S10,S11,S12,S13
1159 FORMAT(/,' S7=',F6.4,5X,'S8=',F6.4,5X,'S9=',F6.4,5X,'S10=',F6.4,
65X,'S11=',F6.4,5X,'S12=',F6.4,5X,'S13=',F6.4)
CALL EXIT
END

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C   COMPUTES CODER DIFFERENTIAL PHASE AND GAIN ERROR IN
C   PRESENCE OF INPUT NOISE AND SPECIFIED STATIC CODER ERRORS.
C   OUTPUT IS FILTERED (TO OBTAIN ONLY SUBCARRIER COMPONENT) BY
C   CROSS CORRELATION.
C   INTEGER BITNO,DB,WINDO,PATH
C   DIMENSION VIO(6),VO(3000),PHIPK(6),PEAK(6),PE(6),GE(6)
C   ,DBO(6)
C   COMMON VI(6),I,TC,TS,W,WM,BITNO,NUM,DA,GDEC
C   READ(2,6) BITNO,IX,PATH
6   FORMAT(3I10)
C   READ(2,5) GAIN,GBX,GBY,VCX,VCY,VOA,VOB,VIP,AMPA,AMPB,OSCA,
6   OSCB,FR,GQ,RE,E1,E2,E3,E4,PHI,DET
5   FORMAT(8F10.4)
C   PI=3.14159265
C   TS=1/(3*4.433619*.1E7)
C   TC=0.05*TS
C   WSC=2*PI*4.433619*.1E7
C   WM=3*PI*4.433619*.1E7
C   W=2*PI*FR*.1E7
C   GDEC = 1.234
C   VPK=0.07
C   RAD=PHI*PI/180.
C   WRITE(3,3003)
3003  FORMAT('INPUT DATA')
C   WRITE(3,3005) BITNO
3005  FORMAT('/',BITNO=' ',I1)
C   WRITE(3,3007) GAIN,GBX,GBY,VCX,VCY,VOA,VOB,VIP
3007  FORMAT('/',GAIN=' ',F5.3,5X,GBX=' ',F5.3,5X,GBY=' ',F5.3,5X,
6   'VCX=' ',F5.3,5X,VCY=' ',F5.3,5X,VOA=' ',F5.3,5X,VOB=' ',
6   'F5.3,5X,VIP=' ',F5.3)
C   WRITE(3,3009) AMPA,AMPB,OSCA,OSCB,FR,GQ,RE
3009  FORMAT('/',AMPA=' ',F5.3,5X,AMPB=' ',F6.4,5X,OSCA=' ',F5.3,5X,
6   'OSCB=' ',F5.3,5X,FR=' ',F6.1,5X,GQ=' ',F5.3,5X,RE=' ',F5.3)
C   WRITE(3,3011) E1,E2,E3,E4
3011  FORMAT('/',E1=' ',F5.3,5X,E2=' ',F5.3,5X,E3=' ',F5.3,5X,E4=' ',
6   'F5.3)
C   WRITE(3,1020) PHI,DET
1020  FORMAT('/',SAMPLING PHASE = ',F5.1,5X,SAMPLING TIME ERROR(NS)
6   '= ',F6.2)
C   DO 3000 J=1,6
C   NUM=0
C   READ(2,600) DB,WINDO
600   FORMAT(2I10)
C   MAX1=6*WINDO-2
C   MAX2=6*WINDO-5
C   IF (DB) 3001,3001,700
700   WRITE(3,800) DB,WINDO
800   FORMAT('/',DB=' ',I3,5X,WINDO=' ',I4)
C   RMSNZ=0.7/(10*((DB/20.)))
C   DO 2000 L=1,6
C   M=0
C   PED = (L-1)*0.14
C   VIO(1)=VPK*SIN(RAD)+0.3+PED
C   VIO(2)=VPK*SIN(RAD+2*PI/3.+WSC*DET/.1E10)+0.3+PED
C   VIO(3)=VPK*SIN(RAD+4*PI/3.)+0.3+PED
C   VIO(4)=VPK*SIN(RAD+WSC*DET/.1E10)+0.3+PED
C   VIO(5)=VPK*SIN(RAD+2*PI/3.)+0.3+PED
C   VIO(6)=VPK*SIN(RAD+4*PI/3.+WSC*DET/.1E10)+0.3+PED
C   LUMINANCE STEP SELECTED
C   DO 1500 K=1,WINDO
C   DO 1000 I=1,6
C   M=M+1
C   TEMP1=VIO(I)
C   CALL GAUSS(IX,RMSNZ,TEMP1,TEMP2)
C   VI(I)=TEMP2
C   RANDOM NOISE ADDED TO VIO(I)
C   CALL CODEX(GAIN,GBX,GBY,VCX,VCY,VOA,VOB,VIP,AMPA,AMPB,OSCA,
6   OSCB,FR,GQ,RE,E1,E2,E3,E4)
1000  VO(M)=DA
1500  CONTINUE
C   TIME SAMPLE IS OVER (2.WINDO) CYCLES,SAMPLES STORED IN VO(M)
C   NOW CROSS-CORRELATE
C   RXY1=.1E7
C   RXY2=.1E8
C   DO 1600 N=1,76
C   PHIN= (N-1)*5.*PI/180.
C   SUM=0.
C   IF (PATH-1) 1525,1525,1553

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```

1525 DO 1550 K=1,MAX1,3
C SUM ELEMENTARY PRODUCTS OVER TIME WINDO
K2=K+1
K3=K+2
1550 SUM=SUM+SIN(PHIN)*VO(K)+SIN(PHIN+2*PI/3.)*VO(K2)+SIN(PHIN+4*PI/3.)*
6*VO(K3)
GOTO 1558
1553 DO 1555 K=1,MAX2,6
C SUM CROSS PRODUCTS
K2=K+1
K3=K+2
K4=K+3
K5=K+4
K6=K+5
1555 SUM=SUM+SIN(PHIN)*VO(K)+SIN(PHIN+PI/3.)*VO(K2)+SIN(PHIN+2*PI/3.)*
60(K3)+SIN(PHIN+PI)*VO(K4)+SIN(PHIN+4*PI/3.)*VO(K5)+SIN(PHIN+5*PI/
6.)*VO(K6)
1558 RXY3=RXY2
RXY2=RXY1
RXY1=SUM/(6*WINDO)
IF (RXY2-RXY1) 1600,1560,1560
1560 IF (RXY2-RXY3) 1600,1600,1650
1600 CONTINUE
1650 RXY1=.1E7
RXY2=.1E8
PHIO = PHIN - PI/18.
DO 1800 I=1,110
PHIM = PHIO + I*PI/1800.
SUM=0.
C PHIM INCREMENTS IN 0.1 DEGREE STEPS
IF (PATH-1) 1675,1675,1710
1675 DO 1700 K=1,MAX1,3
K2=K+1
K3=K+2
1700 SUM=SUM+SIN(PHIM)*VO(K)+SIN(PHIM+2*PI/3.)*VO(K2)
6+SIN(PHIM+4*PI/3.)*VO(K3)
GOTO 1720
1710 DO 1715 K=1,MAX2,6
K2=K+1
K3=K+2
K4=K+3
K5=K+4
K6=K+5
1715 SUM=SUM+SIN(PHIN)*VO(K)+SIN(PHIN+PI/3.)*VO(K2)+SIN(PHIN+2*PI/3.)*
60(K3)+SIN(PHIN+PI)*VO(K4)+SIN(PHIN+4*PI/3.)*VO(K5)+SIN(PHIN+5*PI/
6.)*VO(K6)
1720 RXY3=RXY2
RXY2 = RXY1
RXY1 = SUM/(6*WINDO)
IF (RXY2 - RXY1) 1800,1750,1750
1750 IF (RXY2 - RXY3) 1800,1800,1850
1800 CONTINUE
1850 PHIPK(L) = (PHIM-PI/1800.)*180./PI
C PHASE OF PEAK RESOLVED TO 0.05 DEGREE OR BETTER
PEAK(L)=2000*RXY2
IF (RXY2) 1900,1900,1950
1900 DBO(L)=-100.
GOTO 2000
1950 DBO(L)=20*ALOG(PEAK(L)/57.89)/ALOG(10.)
C SUBHARMONIC GIVEN RELATIVE TO IDEAL SUBCARRIER OUTPUT AFTER
C SINX/X ATTENUATION
2000 CONTINUE
IF (PATH-1) 2050,2050,2350
2050 DO 2300 K=2,6
PE(K)=ABS(PHIPK(K)-PHIPK(1))
IF (PE(K)-180.) 2070,2070,2060
2060 PE(K)=ABS(360.-PE(K))
2070 GE(K)=100.*ABS(PEAK(K)-PEAK(1))/PEAK(1)
WRITE(3,2100) PE(K),GE(K)
2100 FORMAT(/,' PE( DEG)= ',F6.2,5X,' GE(PERCENT)= ',F6.2)
2300 CONTINUE
GOTO 2500
2350 DO 2400 K=1,6
2400 WRITE(3,2450) K,DBO(K)
2450 FORMAT(/,' SUBHARMONIC, STEP',I2,'= ',F6.1,' DB')
2500 WRITE(3,2200) NUM
2200 FORMAT(/,' OVERLOAD COUNT= ',I10)
3000 CONTINUE

3001 CALL EXIT
END

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## REFERENCES

1. CCIR XII<sup>th</sup> Plenary Assembly, New Delhi 1970, vol.5, part 2, Report No. 405-1.
2. JOHNSON and LEONE, 'Statistics and Experimental Design in Engineering and the Physical Sciences', vol.1, Wiley, 1964.
3. IBA Technical Review No.2, 'Technical Reference Book'.
4. ROBERTS, L.G., 'Picture Coding Using Pseudo-Random Noise', IRE Trans. on Information Theory, vol.IT-8, part 2, pp.145-154, Feb. 1962.
5. HAMMING, R.W., 'Numerical Methods for Scientists and Engineers', 2nd. ed., McGraw-Hill, 1973.
6. SCHREIBER, W.F., 'Picture coding', Proc. IEEE, vol.55, No.3, pp.320-330, 1967.
7. MICRO CONSULTANTS LTD. (Engineering Note MCP310/8/73) Interface House, Croydon Road, Caterham, Surrey.
8. DEVEREUX, V.G., (B.B.C. Research Dept.), private communication.
9. REEVES, A.H., 'Electrical Signaling System', Int. Standard Electric Corp., U.S. Patent No.2,272,070, Feb. 1942.
10. BENNETT, W.R., 'Spectra of Quantized Signals', B.S.T.J., vol.27, No.3, pp.446-472, July 1948.
11. SHANNON, C.E. et al, 'The philosophy of PCM', Proc. IRE, vol.36, pp.1324-1331, Nov. 1948.
12. GOODALL, W.M., 'Television by pulse code modulation', B.S.T.J., vol.30, Jan. 1951.
13. BLACK, H.S., and EDSON, J.O., 'Pulse Code Modulation', AIEE, vol.66, pp.895-899, 1947.
14. GOLDING, L.S., 'DITEC, a digital communications system for satellite links', Proc. 2nd Int. Conf. on Digital Satellite Comm., Paris, Nov.1972.

15. BORODICH, S.V., 'Interference Suppression Properties of Pulse Code Modulation Systems', Radiotekhnika, vol.4, pp.13-27, 1949.
16. KRETZMER, E.R., 'Statistics of Television Signals', B.S.T.J., vol.31, pp.751-763, July 1952.
17. O'NEAL, J.B., 'Predictive Quantizing Systems (Differential Pulse Code Modulation) for the Transmission of Television Signals', B.S.T.J., pp.689-721, May-June 1966.
18. CUTLER, C.C., 'Differential Quantization of Communication Signals', Patent No. 2,605,361, July 29, 1952.
19. SCHREIBER, W.F., 'The measurement of third order probability distribution of television signals', IRE Trans. on Information Theory, vol.IT-2, pp.94-105, Sept. 1956.
20. DEVEREUX, V.G. and ROUT, E.R., 'The use of PCM in television networks', IEE Colloquium on Pulse Code Modulation, pp.18/1-18/6, 1968.
21. EDSON, J.O. and HENNING, H.H., 'Broadband Codecs for an Experimental 224 Mb/s PCM Terminal', B.S.T.J., pp.1887-1940, Nov. 1965.
22. BROWN, D.W., 'The conversion of television signals into digital form', M.Sc. Thesis, Imperial College, London, 1962.
23. TEESDALE, R.R. and WESTON, J.D., 'The Encoding of Broadband Signals', Systems and Communications, pp.18-22, Feb. 1967.
24. B.B.C. Research Dept. Report No.E1-14, Serial No.1968/6, 'Experimental equipment for converting television signals into digital signals and vice versa'.
25. B.B.C. Research Report No. 1970/25, 'Pulse code modulation of video signals: 8-bit coder and decoder'.
26. JOHANNESSEN, F.G., 'Successive approximation and feedback p.c.m. encoder for television', Proc. IEE, vol.117, No.4, pp.671-680, April 1970.

27. MILLARD, J.B. and MAUNSELL, H.I., 'Digital Encoding of the Video Signal', (the Picturephone System), B.S.T.J., pp.459-479, Feb. 1971.
28. OLIVER, B.M., 'Efficient Coding', B.S.T.J., 31, No.4, pp.724-750, July 1952.
29. HARRISON, C.W., 'Experiments with Linear Prediction in Television', B.S.T.J., 31, No.4, pp.764-783, July 1952.
30. GRAHAM, R.E., 'Subjective Experiments in Visual Communication', IRE National Convention Rec., vol.6, pt.4, pp.100-106, 1958.
31. B.B.C. Research Dept. Report No. 1971/40, 'Pulse code modulation of video signals: subjective study of coding parameters'.
32. GOLDING, L.S. and GARLOW, R.K., 'Frequency interleaved sampling of a Colour Television Signal', IEEE Trans. on Comm. Technology, vol.COM-19, No. 6, pp.972-979, Dec. 1971.
33. THOMPSON, J.E., 'Differential Coding for Digital Transmission of PAL Colour Television Signals', International Broadcasting Convention, 1972, and, 'An experimental differential p.c.m. encoder-decoder for Viewphone signals', The Radio and Electronic Engineer, vol. 43, pp.201-208, March 1973.
34. B.B.C. Research Dept. Report No. 1972/36, 'DIGITAL VIDEO: reduction of sampling frequency to 11.9MHZ'.
35. B.B.C. Research Dept. Report No. 1973/21, 'Digital Transmission codes: preliminary investigation of HDB3 and related ternary codes for broadcast signal distribution'.
36. PARKER, F.G., 'The impact of digital techniques on studio equipment', International Broadcasting Convention, 1972.
37. HOESCHELE, D.F., 'Analog-to-Digital/Digital-to-Analog Conversion Techniques', Wiley, 1968.

38. CCIR XII<sup>th</sup> Plenary Assembly, New Delhi, 1970, Rec. 451-1.
39. STEVEN, S.S., 'Handbook of Experimental Psychology', New York, Wiley, 1951.
40. LIMB, J.O., 'Design of Dither Waveforms for Quantized Visual Signals', B.S.T.J., pp.2555-2582, Sept. 1969.
41. SCHINDLER, H.R., 'UHF Analog-Digital Converter', Int. Solid-State Circuits Conf. of Technical Papers, Feb. 1963.
42. GRAY, J.R. and KITSOPOULOS, S.C., 'A Precision Sample and Hold Circuit with Subnanosecond Switching', IEEE Trans. on Circuit Theory, pp.389-396, Sept. 1964.
43. GARDNER, F.M., 'Phaselock Techniques', Wiley.
44. POMEROY, P., 'Designing a Television line Flywheel Generator using a Phase-locked Loop IC', The Radio and Electronic Engineer, vol.42, no.11, pp.479-488, Nov. 1972.
45. MOTOROLA handbook on Integrated Circuits, 1971.
46. KAUPP, H.R., 'Characteristics of Microstrip Transmission Line', IEEE Trans. on Computers, vol. EC16, No. 2, April 1967.
47. SPRINGFIELD, W.K., 'Designing transmission lines into multilayer boards', Electronics No.1, 1965.
48. MILLMAN and TAUB, 'Pulse, Digital and Switching Waveforms', McGraw-Hill, 1965.
49. LATHI, B.P., 'Communication Systems', Wiley, 1968.
50. JARVIS, D.B., 'The effects of interconnections on high-speed logic circuits', IEEE Trans. on Electronic Computers, pp.476-487, Oct. 1963.
51. CATTERMOLE, K.W., 'Principles of PCM', Iliffe, 1969.
52. DORWARD, R.M., 'Aspect of the Quantization noise associated with the digital coding of colour-television signals', Electronics Lett., vol.6, No.1, pp.5-7, Jan. 1970.



53. VERHOVEN, L., 'More aspects of quantization noise associated with digital coding of colour-television signals', Electronics Lett., vol.9, No.3, pp.69-70, Feb. 1973.
54. BALDWIN, J.L.E., 'The digital future of television studio centres', International Broadcasting Convention, 1972.
55. NEU, W., 'Some techniques of Pulse Code Modulation', Bulletin S.E.V., pp.8-17, 8th. Oct. 1960.
56. SMITH, B.D., 'An unusual analog-digital conversion method', Trans. IRE Instrumentation, pp.155-160, June 1956.
57. WALDHAUR, F.D., U.S. Patent 3,187,325, 1965.
58. EULER, K., 'Pulse code modulation for wide frequency bands with encoding time adaptation', IEE Conf. on Transmission Aspects of Comm. Networks, London, 1964.
59. PEARCE, T.H. and MAYS, L., 'Pulse code modulation for wideband signals', The Marconi Review, 4th. Quarter, pp.286-313, 1971.
60. JOHANNESSEN, F.G., 'PCM encoder for wideband signals', D.I.C. thesis, Imperial College, London, June 1969.
61. BOUTMY, P., 'Decodeur-extenseur pour système de modulation par impulsions codées', Cables and Trans., 17, pp.264-270, Oct. 1963.
62. INGRAM, D.G.W., 'Non-linear coder and decoder for a PCM system', IEE conf. on Transmission Aspects of Comm. Networks, London, 1964.
63. McNEILLY, J.H., B.P. application 43586/65.
64. REEVES, A.H., French patent 852,183, 1938 and B.P. 535,860, 1939.
65. THOMPSON, J.E., 'Reduction of perceptual redundancy for Data compression of Television signals', Ph.D. thesis, Imperial College, Univ. London, May 1968.

66. WADE, J.G., 'Crosscorrelation method for analysing phase and gain errors in PCM systems for colour television', Proc. IEE, vol.122, No.4, pp.367-368, April 1975.
67. BRAINARD, R.C. and CANDY, J.C., 'Direct-Feedback Coders: Design and performance with television signals', Proc. IEEE, vol.57, No.5, May 1969.
68. ROBINSON, A.H. and CHERRY, C., 'Results of a Prototype Television Bandwidth Compression Scheme', Proc. IEEE, vol.55, No.3, March 1967.
69. CCITT Special Study Group D, 'Digital Encoding of Television Programme Signals', (Question 10/D), source: COMSAT.
70. CHANG, H. and COOPER, A., 'Bubble Domain Analog-to-Digital Converter', IBM Tech. Disclosure, Bulletin, vol.14, No. 7, Dec. 1971.
71. DEVEREUX, V.G., 'Digital video: differential coding of PAL signals based on differences between samples one subcarrier period apart', B.B.C. Research Dept., Report No. 1973/7.
72. THOMPSON, J.E., UK Patent Application 40309/71, Aug. 27, 1971.
73. THOMPSON, J.E., 'Differential Encoding of Composite Colour Television Signals using Chrominance-Corrected Prediction', IEEE Trans. on Comm., vol.COM-22, No.8, Aug. 1974.
74. PRATT, W.K., KANE, J., and ANDREWS, H.C., 'Hadamard transform image coding', Proc. IEEE, vol.57, No.1, pp.58-68, 1969.
75. WINTZ, P.A., 'Transform picture coding', Proc. IEEE, Vol.60, No.7, pp.809-820, 1972.
76. OHIRA, T., HAYAKANA, M., MATUMOTO, K., and SHIBATA, K., 'Picture quality of Hadamard transform coding using non-linear quantizing of colour television pictures', symp. on Appl. of Walsh Functions, Washington D.C., April 16-18, 1973.



77. WALKER, R., 'Hadamard Transformation: a real-time transformer for broadcast standard pom television', B.B.C. Research Dept. Report, No. 1974/7.
78. WALKER, R., and CLARKE, C.K.P., 'Walsh-Hadamard transformation of television pictures', B.B.C. Research Dept. Report No. 1974/13.
79. BALDWIN, J.L.E., (Head Video Section, Experimental and Development Dept., IBA), private communications.
80. CHOWANIEC, A., 'Charge Transfer Device Analogue Delay Lines', Electronics and Power, pp.1122-1126, 12 Dec., 1974.
81. KRETZMER, E.R., 'Reduced Alphabet Representation of Television Signals', IRE Conv. Record, Part 4, 1956.
82. GOODYEAR, C.C., 'Signals and Information', BUTTERWORTHS, 1971, (appendix 4).
83. SHANNON, C. E., 'Proc. Inst. Radio Engrs.', Vol.37, pp.10-21, 1949.
84. BARR, P., 'Influence of aperture-time and conversion rate on the sampling accuracy of A-D converters', Data Systems Engineering, pp.30-34, May 1964.
85. Engineering Notes: COMPUTER LABS., 1109 South Chapman St., Greensboro, N. Carolina 27403; MICRO CONSULTANTS LTD., Interface House, Croydon Rd., Caterham, Surrey; DATEL SYSTEMS, INC., 1020 Turnpike St., Canton, Mass. 02021.
86. EARLY, J.M., 'Speed, power and component density in multielement high speed logic systems', Proc. Int. Solid State Circuits Conf., Philadelphia, Pa., p.78, 1960.
87. KHANTEL, A.D., 'Normalization of errors in the coding of random signals', Measurement Techniques (USA), vol.16, No.1, pp.36-40, Jan. 1973.

88. TARNAY, K., 'Computer simulation of an amplitude-digital conversion', *Meres es Automatika (Hungary)*, vol.18, No.10, pp.368-373, 1970.
89. CALLAS, L., 'Evaluating analog-to-digital converters', *Simulation*, pp.81-86, March 1975.
90. SHEINGOLD, D.H., editor 'Analog-Digital Conversion Handbook', Analog Devices, Inc. Norwood, Mass (USA), June 1972.
91. LANCASTER, J.F. et al, 'Analog-to-Digital Converter Technology', Preliminary Investigation and Proposal, U.S. Army Missile Command Technical Report RE-73-25, Aug. 1973.
92. GORDON, B.M., 'Effects of noise on analog to digital conversion accuracy; a tutorial', 1973 Electronics Meeting on A/D and D/A Conversion, Lausanne, Switzerland, pp.186-221, 16-18 Oct. 1973.
93. SMITH, B.F., 'High speed A/D and D/A converters: their effect on video signal fidelity', 1973 Electronics Meeting on A/D and D/A Conversion, Lausanne, Switzerland, pp.413-438, 16-18 Oct. 1973.
94. HARTLEY, M.G., et al, 'Digital simulation methods', IEE Monograph series 15, Peregrinus, 1975.
95. EYKHOFF, P., 'System Identification, Parameter and State Estimation', Wiley, 1974, (p.67).
96. CONNOLLY, J.J., 'Critical design parameters and test methods for ultra high speed analog-to-digital conversion', 1973 Electronics Meeting on A/D and D/A Conversion, Lausanne, Switzerland, pp.374-411, 16-18 Oct. 1973.
97. CANDY, J.C., 'A use of Limit Cycle Oscillations to obtain Robust Analog-to-Digital Converters', *IEEE Trans. on Comm.*, vol.COM-22, No.3, pp.298-305, March 1974.
98. KNUTH, D.E., 'Seminumerical Algorithms Vol.2: the art of computer programming', Addison-Wesley, 1969, (p.82).

99. COOLEY, J.W., and TUKEY, J.W., 'An algorithm for the machine calculation of complex Fourier series', Math. of Computation, vol.19, April 1965.
100. DI ROCCO, J.V., 'A/D and D/A converters in System Design', 1973 Electronics Meeting on A/D and D/A Conversion, Lausanne, Switzerland, pp.497-515, 16-18 Oct. 1973.
101. FLETCHER, R.E., 'A video analogue to digital converter', International Broadcasting Convention, pp.47-57, 1974.
102. DEVEREUX, V.G., and PHILLIPS, G.J., 'Bit-rate reduction of digital video signals using differential PCM techniques', International Broadcasting Convention, pp.83-89, 1974.
103. PINEL, J.F., and ROBERTS, K.A., 'Tolerance Assignment in Linear Networks Using Nonlinear Programming', IEE Trans. Circuit Theory, pp.475-479, 1972.

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