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ON CODING AND DETECTION TECHNIQUES FOR TWO-DIMENSIONAL MAGNETIC RECORDING

by

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Abstract

The areal density growth of magnetic recording systems is fast approaching the superparamagnetic limit for conventional magnetic disks. This is due to the increasing demand for high data storage capacity. Two-dimensional Magnetic Recording (TDMR) is a new technology aimed at increasing the areal density of magnetic recording systems beyond the limit of current disk technology using conventional disk media. However, it relies on advanced coding and signal processing techniques to achieve areal density gains. Current state of the art signal processing for TDMR channel employed iterative decoding with Low Density Parity Check (LDPC) codes, coupled with 2D equalisers and full 2D Maximum Likelihood (ML) detectors. The shortcoming of these algorithms is their computation complexity especially with regards to the ML detectors which is exponential with respect to the number of bits involved. Therefore, robust low-complexity coding, equalisation and detection algorithms are crucial for successful future deployment of the TDMR scheme.

This present work is aimed at finding efficient and low-complexity coding, equalisation, detection and decoding techniques for improving the performance of TDMR channel and magnetic recording channel in general. A forward error correction (FEC) scheme of two concatenated single parity bit systems along track separated by an interleaver has been presented for channel with perpendicular magnetic recording (PMR) media. Joint detection decoding algorithm using constrained MAP detector for simultaneous detection and decoding of data with single parity bit system has been proposed. It is shown that using the proposed FEC scheme with the constrained MAP detector/decoder can achieve a gain of up to 3dB over un-coded MAP decoder for 1D interference channel. A further gain of 1.5 dB was achieved by concatenating two interleavers with extra parity bit when data density along track is high. The use of single bit parity code as a run length limited code as well as an error correction code is demonstrated to simplify detection complexity and improve system performance.

A low-complexity 2D detection technique for TDMR system with Shingled Magnetic Recording Media (SMR) was also proposed. The technique used the concatenation of 2D MAP detector along track with regular MAP detector across tracks to reduce the complexity order of using full 2D detection from exponential to linear. It is shown that using this technique can improve track density with limited complexity. Two methods of FEC for TDMR channel using two single parity bit systems have been discussed. One using two concatenated single parity bits along track only, separated by a Dithered Relative Prime (DRP) interleaver and the other use the single parity bits in both directions without the DRP interleaver. Consequent to the FEC coding on the channel, a 2D multi-track MAP joint detector decoder has been proposed for simultaneous detection and decoding of the coded single parity bit data. A gain of up to 5dB was achieved using the FEC scheme with the 2D multi-track MAP joint detector decoder over un-coded 2D multi-track MAP detector in TDMR channel. In a situation with high density in both directions, it is shown that FEC coding using two concatenated single parity bits along track separated by DRP interleaver performed better than when the single parity bits are used in both directions without the DRP interleaver.

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Glossary

ACSU	Add Compare and Select Unit
AP	A-Priori Probability
APP	A-Posteriori Probability
ATE	Adjacent Track Erasure
AWGN	Additive White Gaussian Noise
BCJR	Balh Cocke Jevelink Raviv
BER	Bit Error Rate
BMU	Branch Metric Unit
BPMR	Bit Patterned Media Recording
CD	Compact Disk
DDNP	Data-dependent Noise Prediction
DPR	Dithered Relative Prime
EAMR	Energy Assisted Magnetic Recording
ECC	Error Correction Codes
EPR-4	Extended Partial Response 4
FEC	Forward Error Correction
FER	Frame Error Rate
FG	Factor Graph
GA	Gaussian Approximation
GFP	Grain Flipping Probability
GMR	Giant Magneto Resistive

GPR	Generalized Partial Response
HAMR	Heat Assisted Magnetic Recording
HDD	Hard Disk Drive
IDC	International Data Corporation
IRCSDFA	Iterative-Row-Column Soft Decision Feedback Algorithm
ISI	Inter-Symbol Interference
ITI	Inter-Track Interference
LDPC	Low Density Parity Check
LMR	Longitudinal Magnetic Recording
LLR	Log Likelihood Ratio
LUT	Look-Up Table
LTI	Linear Time-Invariant
MAMR	Micro-Wave Assisted Magnetic Recording
MAP	Maximum-A-Posteriori Probability
MIMO	Multiple Input Multiple Output
ML	Maximum Likelihood
MLSD	Maximum Likelihood Sequence Detection
MMSE	Minimum Mean Square Error
MSE	Mean Square Error
MR	Magneto Resistive
MTR	Maximum Transition Run
NP	Non-Deterministic Polynomial-Time
NPML	Noise Predictive Maximum Likelihood
NRZ-L	Non-Return to Zero-Level
NRZ-I	Non-Return to Zero-Inverted
PDNP	Pattern-dependent Noise Prediction
PMR	Perpendicular Magnetic Recording

PR	Partial Response
PRML	Partial Response Maximum likelihood
RAMAC	Random Access Method of Accounting and Control
RLL	Run Length Limited
RS	Reed-Solomon
SMR	Shingled Write-Magnetic Recording
SNR	Signal-to-Noise Ratio
SOP	Sum of Products
SOVA	Soft Output Viterbi Algorithm
SPA	Sum-Product Algorithm
SSD	Solid State Drive
SUL	Soft Magnetic Under-Layer
TMR	Transvers Magnetic Recording
TDMR	Two-dimensional Magnetic Recording
TBU	Trace-Back Unit
VA	Viterbi Algorithm
1D	One-dimensional
2D	Two-dimensional

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Author's Declaration

At no time during the registration for the degree of Doctor of Philosophy has the author been registered for any other University award without prior agreement of the Doctoral College Quality Sub-Committee.

Work submitted for this research degree at the University of Plymouth has not formed part of any other degree either at the University of Plymouth or at another establishment.

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The author has presented a paper in the following peer-reviewed international conferences:

1. 2016 Asia-Pacific Magnetic Recording Conference (APMRC 2016), Seoul, Korea, 13 - 15 July 2016;

2. 30th Annual IEEE Canadian Conference on Electrical and Computer Engineering (CCECE' 2017), Windsor, Canada, 30 April - 3 May 2017; and

3. 40th International Conference on Telecommunications and Signal Processing (TSP' 2017), Barcelona, Spain, 5 - 7 July 2017.

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Signed: _____

Mohammed Dikko Almustapha

Date: _____

Dedication

This thesis work is dedicated to my late father Engr. Muhammad Almustapha.

Chapter 1

Introduction to Magnetic Recording

1.1 Introduction

The advent of modern digital technology has revolutionized the way in which we create and manage information. Information data in digital form can easily be handled, processed, and transferred to different locations from the location where the data was first created, or accessed at a later time different from when the information was created. This facilitates the continuous rapid growth of user data and the demand for data from various applications and devices, ranging from personal computers (PCs), Internet, smartphones, datacentres, entertainments, corporate businesses etc.

Depending upon the device or application that create the information or is intended for, or whether the information is to be accessed at a different location or at a later time, there always exist a form of storage system that hold the data either permanently or temporarily. Temporary mode of storage has lower storage capacity and hold information for a short period of time until the data is processed. While permanent mode of storage provides higher storage capacity and access to the information at any later time. Over time, different kinds of storage system technologies have evolved for supporting wide range of commercial enterprise and consumer storage demand. These storage systems are categorised depending on their storage medium

type, information capacity and data access method. Among the storage technologies includes: magnetic tapes, optical disk, magnetic hard disk drive (HDD), and solid-state drive (SSD).

The demand for data storage capacity across all media types is poised to keep on increasing exponentially, driven by the widespread dissemination of the Internet, online streaming services, big data application, and cloud computing. Recently, the International Data Corporation (IDC) forecast predicted the amount of data to be generated globally by the year 2025 to reach about 163 zettabytes (zettabyte is trillion gigabytes), which is almost tenfold of the amount created in 2016 (Reinsel, Gantz and Rydning, 2017). To keep up with this data age demand, more storage capacity is needed to be shipped across all media types with the bulk of the shipment capacity emanating from the magnetic HDD industry.

Magnetic HDDs have been the dominant and most important storage devices over time and up till today due to their reliability and low storage cost per gigabytes of data. They provide a much easier, faster, denser, affordable and more portable means of data storage. Today they are the most common recording medium used in millions of PCs, servers, and workstations found in our homes, offices and enterprise centres.

IBM pioneered the development of the HDD industry with the release of the first commercial HDD in 1956. The “IBM model 350” was developed around the “IBM RAMAC 305 system” which enabled random access to data stored on a memory device. It had a storage capacity of about 3.75 MB and weighed 500lb (Vasic and Kurtas, 2005). Today’s HDDs are much cheaper and faster than the IBM 350 with reduced size (less than 3.5 to 2.5 inches) and higher storage capacity (6Terabytes to 12Terabytes) (Goodwins, 2015) (Reinsel, Gantz and Rydning, 2017). This was possible due to innovations in recording technologies, primarily on magnetic heads and recording media that resulted in significant improvements in recording densities.

The implementation of partial response maximum likelihood (PRML) techniques (Cocker et al, 1991) on HDD in the early 1990's marks a major turning point in the development of HDD system. From 1956 up to 1989, the main signal detection method used on the HDD was peak detection. The adoption of PRML detection saw a significant increase in linear recording densities of magnetic HDD as more bits are packed closely together and the interaction between adjacent bits was no longer a concern. In 1997, Giant magneto resistive (GMR) heads appeared in the HDD industry prompting an exponential rise in linear densities of magnetic storage devices. Recording densities improved by 100% annually (Hattori, Suzuki and Sugaya, 2011) thanks to the new GMR head structure. However, this figure dropped to 30% annually in 2001 (Hattori, Suzuki and Sugaya, 2011) due to media limitation of longitudinal magnetic recording reaching its superparamagnetic limit of 150Gbit/in^2 (Chen et al., 2003) (Leonhardt et al., 2001). But this trend was reversed with the deployment of Perpendicular magnetic recording (PMR) technology to HDD in 2005. Since then, the growth in capacity of HDD continued to grow more than double every year in accordance with the Kryder's law (Walter, 2005)) projection that is similar to Moore's law. But increasing demand for higher storage capacity has approached a limit imposed by the superparamagnetic limit beyond which the conventional PMR media is no longer scalable. To continue the areal density growth beyond the current 1 Tb/in^2 limit (Shiroishi, 2009) for conventional recording media, new technologies have to be developed.

1.2 Evolution of Magnetic Hard Disk Storage

The magnetic hard disk storage system has undergone various evolutional and developmental stages throughout the decades since the invention of the first commercial HDD. Some of the major historic events that happed in the development of the magnetic hard disk including the signal processing aspects that had yielded tremendous gain in storage capacity are highlighted below:

1956 IBM RAMAC 305- The first commercial computer disk storage to appear on market was released. The IBM 305 RAMAC (Random Access Method of Accounting and Control) allow random access to the data stored on it and has a capacity of 3.75 MB (Vasic and Kurtas, 2005).

1962 IBM model 1301 was released. The disk drive has a storage capacity of 56 MB and featured a dedicated clock track for timing and recovery in the data channel (Vasic and Kurtas, 2005).

1967 Forney applies trellis decoding to simplify the decoding of convolutional codes given more insight into the concept of Viterbi algorithm (Forney, 1967).

1970 Extension of the PRML techniques application to magnetic recording channels was proposed (Kobayashi and Tang, 1970).

1971 Magneto resistive head was discovered by Hunt (Hunt, 1971).

1974 The BCJR algorithm was introduced as a Maximum A-posteriori Probability (MAP) decoding algorithm for minimizing symbol or bit error rate (Bahl et al., 1974).

1979 First disk drive with run-length-limited (RLL) coding scheme was introduced by IBM. The IBM 3370 employed thin-film inductive heads and (2, 7) RLL code to improve performance (Vasic and Kurtas, 2005).

1984 Constrained coding for PRML channel was proposed by Barian Marcus and Paul H. Siegel (Marcus and Siegel, 1984).

1989 First disk drive to use PRML channel IBM 0681was shipped. The disk drive has an areal density of One-gigabit-per-square-inch and is 3.5 inch in size.

1992 (Marcellin and Weber, 1992) proposed Two-dimensional modulation codes based on RLL constraints applied on multiple tracks to improve performance. Similarly, (Swanson and Wolf, 1992) introduced new class of Two-dimensional RLL recording codes that imposed an additional constraint across each track.

1992 Magneto resistive heads made their first appearance on a commercial hard drive IBM Rochester (Vasic and Kurtas, 2005).

1997 GMR heads were first employed on hard drives by IBM which opened the gateway toward achieving 100% improvement in recording density

2005 Toshiba announced the deployment of the first HDD to use the PMR technology.

2007 Hitachi Global Storage Technologies announced the release of its first 1 Terabyte HDD using PMR technology. Also, this same year Fujitsu achieved a significant breakthrough in patterned media technology.

2009 Wood suggested the possibility of achieving magnetic recording at 10 Terabits per square inch on conventional recording media (Wood et al., 2009).

2013 Western Digital released the first 6 TB Helium field HDD into market (Anthony, 2013).

2014 First HDD deploying shingled write magnetic recording media was introduced into the market by Seagate (Pinola, 2015).

2015 Hitachi Global Storage Technologies delivered the world first 10 TB capacity HDD. The ultra-star archive Ha^{10} is based on field-proven HelioSeal platform with shingled magnetic recording technology (Harris, 2015).

2018 Western Digital introduced a 14 TB capacity HDD using conventional perpendicular magnetic recording with two-dimensional magnetic recording read heads (Coughlin 2018).

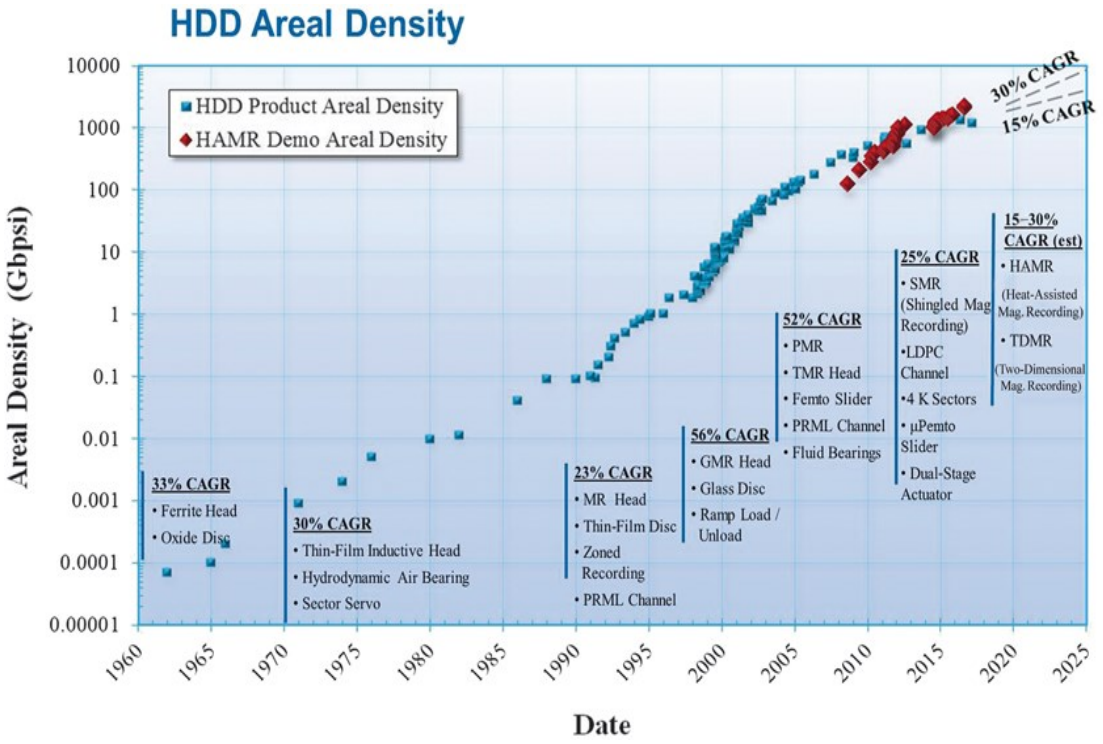


Figure 1.1: Evolution of HDD technology with areal density growth projection source: (Kautzky and Blaber, 2018).

Over five decades of progression, the storage capacity of HDD has grown tremendously by continuous increase in areal density growth of the data stored on the media. This is driven by the progression in technological and materials innovation. The areal density growth has increased over past decades with a compounded annual growth rate (CAGR) of 30% (Kautzky and Blaber, 2018). Figure 1.1 shows the evolution of HDD technology and the areal density progression /growth projections triggered by the new technological and materials innovation.

Similarly, Figure 1.2 shows the future HDD technology roadmap issued by the Advanced Storage Technology Consortium (ASTC), and how the technology has moved on from conventional

perpendicular magnetic recording (PMR) to heat-doted magnetic recording (HDMR) with the expected data storage demand/requirement to be fulfilled by the new upcoming technologies.

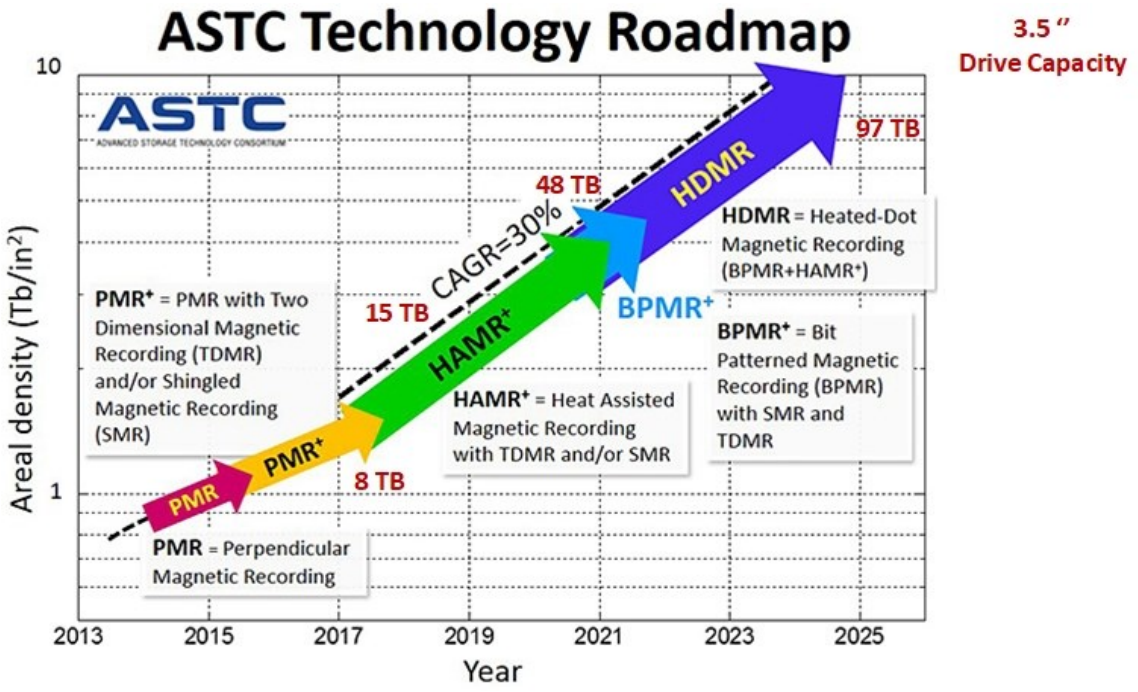


Figure 1.2: Roadmap for HDD technology areal density projection with expected data storage requirement/demand for 3.5'' drive disk. Source: (Bala, Landers and McArthur, 2018).

1.3 Basic Hard Disk Drive Components

Magnetic hard drives are very important devices found in computers and server machines. They form the backbone of the storage system and are the primary means of permanent data storage for those machines. They stored *non-volatile* data, meaning the data stored is retained on the hard drive even when the computer is switched off, except when the data is deliberately erased or overwritten. Because of the data retention capability, crucial software programmes and important data are stored on the hard drive. The basic components that made up the HDD are shown as depicted by the Figure 1.3.

Figure 1.3: Hard disk drive components (Craig, 2007).

The main component on the HDD where the data are recorded on is the platter. *Platters* are circular rigid disk which cannot be bent or flexed, hence the name hard disk. They are traditionally made from an aluminium/magnesium alloy, but modern platters are now made of glass-ceramic composite material to increase rigidity and reduce weight (Hard Disk Drives). A HDD can have one or more platters depending on the desired capacity with each having a separate read/write head. The surface of the platters is covered on both sides with a thin magnetic layer to form the medium on which magnetic information is stored. Iron oxide medium and Thin-film medium are the most commonly used media on hard disk platters. Disk platters are mounted on a spindle around which they revolve. A *Spindle motor* is connected directly to the spindle and is the main motor that spins the hard drive platters at a very high speed.

The *Read/Write heads* are HDD components used in reading and writing data on the magnetic media. Data is written on the media by passing a write current through the write head that magnetizes the magnetic medium is opposite directions representing either 1 or 0. Similarly, data is read out of the media by the Read head sensing the magnetic flux of the medium which

then converts into voltages. The heads are connected or ganged on a single moving mechanism that moves them across the disk platters. This mechanical system that moves the heads and positioned them accurately towards the disk is known as the *Head Actuator Mechanisms*. Head actuator mechanisms are broadly classified into two forms: stepper motor actuators and voice coil actuators. Most modern HDDs employed the voice coil actuator mechanism because of their advantage of performance and reliability compared to the former (Craig, 2007).

Other components found on the hard drive are the *Logic board*, *Cables and connectors*, and also *Configuration items*. The logic board is an intelligent circuit board that contains electronic components for controlling the various sections of the HDD and also provide an interface between the computer and HDD. Cables carry power supply from the computer to the hard drive to supply the motors and actuators, while interface connectors carry data and command signals between the computer and the hard drive.

1.4 Introduction to Digital Magnetic Recording

Digital magnetic recording is the act of storing and retrieving of binary information on magnetic media. Binary information/data are recorded on magnetic medium in time with the intention of retrieving or reading the data at a later time. It can be viewed as synonymous to a communications system transmitting data in time from “now” to “later”. Therefore, the whole digital magnetic recording system can be modelled as a linear time-invariant (LTI) system with the readback signal distorted due to various channel effects. Error correction codes (ECC) and other signal processing techniques are employed to successfully recover the stored data.

Two main processes characterized the entire magnetic recording process: namely, the “writing” process and the “reading” process. The data to be recorded on the disk are modulated into a write current and passed on to the magnetic medium through the write head. The write head

creates regions of magnetisation flux on the medium which changes the magnetisation of the medium depending on the change in the direction of the magnetic field applied. During the readback process, the magnetisation patterns in the form magnetic flux created on the media are sensed by the Read head which are converted into voltages to generate the readback waveform.

1.4.1 Data Writing

The magnetic medium has essentially two saturation states with the modulated signal current being bipolar. Data is written on the magnetic medium by changing the direction of magnetisation on the medium in two opposite directions. Two directions of magnetic field created by the write current are therefore needed to represent the data bits either 0s or 1s. This form of recording is known as the two-level magnetic recording (Vasic and Kurtas, 2005). It is the most popular and stable form of data recording with less susceptibility towards noise and other distortions. This is because going beyond two-level (multi-level recording) results in more distortions beyond the gain in capacity or an exponential increase in complexity (Shah eat al., 2005).

Data bits are recorded on the disk in concentric tracks written spatially as a sequence of small magnetic domains, one after the other in the direction of the moving write head. A track is a circular path on the disk that provide a physical means of dividing data on the disk. A track is subdivided into a group of sectors. Data sector or cluster contains contiguous group of physical sector(s) on the disk. Figure 1.4 shows a simplified structure of a disk (Ace Data Recovery). In conventional HDD, guard bands are placed in between tracks and sectors to provide separation between tracks or sectors in order to avoid over-writing data on adjacent track during the write process or interference from adjacent track data during the read process.

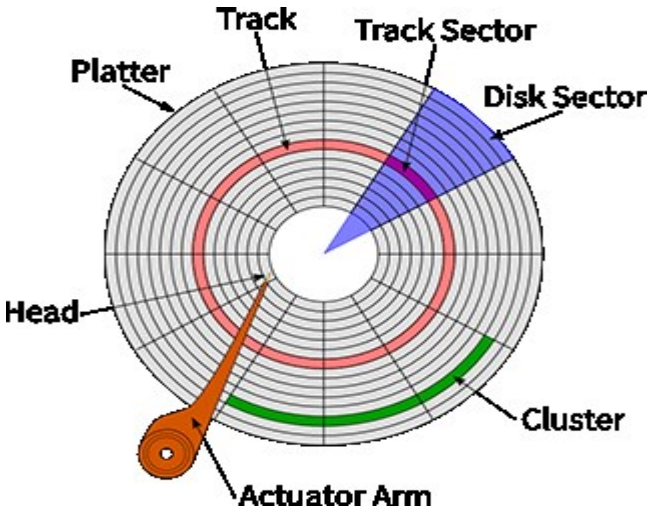


Figure 1.4: Disk structure (Ace Data Recovery).

1.4.2 Data Format

For the recorded data to be suitably and successfully read by the Read head during the reading process, the data to be written on the magnetic medium needed to be given a certain format that best matches the characteristics of the recording medium. These include requirements for synchronisation and timing of the readback waveform (Vasic and Kurtas, 2005).

The two most popular formats of written data for two-level bit system used on digital magnetic recording medium are namely: Non-Return to Zero-Level (NRZ-L) and Non-Return to Zero-Inverted (NRZ-I) (Immink, 1991).

In the NRZ-L format, two opposite directions of magnetisation field created by the positive and negative amplitude of the write current are used to represent the digital data {1, 0}. That is to say, bit 1 is represented by the positive or (upward) direction of the magnetisation field while bit 0 is represented by the negative or (downward) direction of the magnetisation field. This is the simplest format for representing data in magnetic recording channels especially when magneto resistive head is used for reading data. However, NRZ-L format has the disadvantage

of error propagation when a bit is misread during the read process. To prevent errors propagating within the user data sequence, NRZ-I is used to provide a form of precoding.

Using the NRZ-I format; a change in the direction of the magnetic field is used to represent data rather than the actual direction of the magnetic field. The presence of a transition (low to high or high to low) denotes a binary 1, while no transition denotes a binary 0. The process of converting the user data to NRZ-I format is termed precoding (Kobayashi and Tang, 1970). Precoding prevents an error that occurs in detection of a single bit to spread across the entire data sequence to be read ahead (Siegel, 1985). Figure 1.5 shows the signal format and magnetisation pattern representation of bits 01001100011.

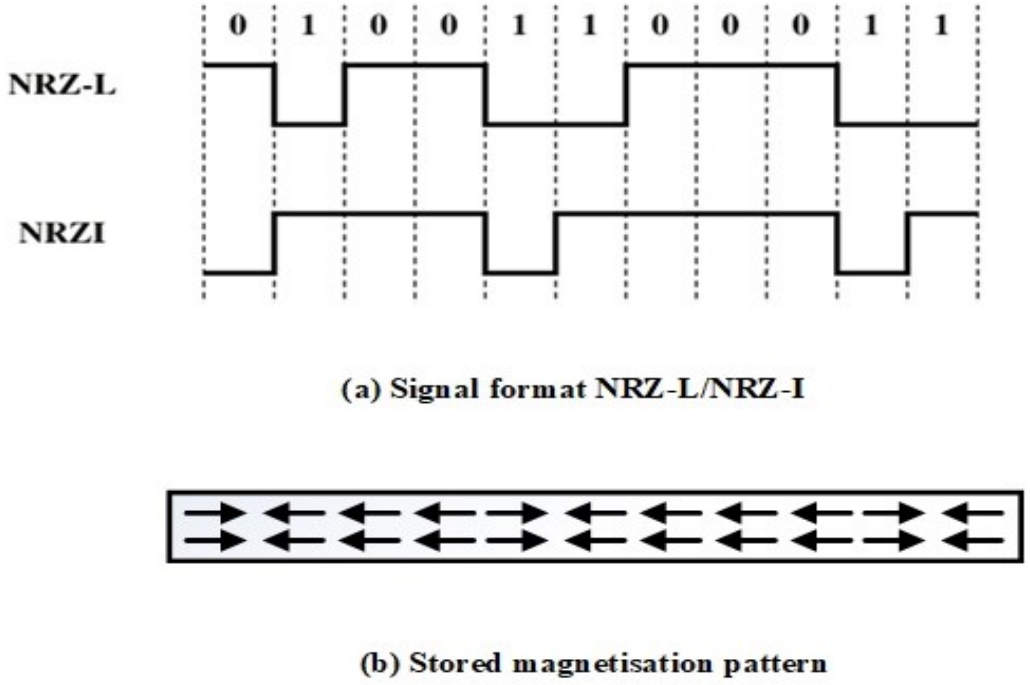


Figure 1.5: Signal format and stored magnetisation pattern for 01001100011

1.4.3 Data Reading

The recorded data are stored on the magnetic disk in form of magnetisation flux. During the reading process, the Read head fly over the disk surface at a steady clearance of 5 nm (Zhu,

2003) and picks up the magnetisation flux to generate the readback waveform that drive the data and the data clock. An effective magnetic Read head is therefore critical to the success of any magnetic recording scheme. The popularly known Read head used in magnetic recording are the inductive read heads “inductive heads” for short, and the Magneto Resistive (MR) read heads.

Prior to 1990, inductive heads were the dominant head technology found in most hard drive systems. The same head is used for both inductive writing (time-varying current producing a time-varying magnetic field) when driven by a write current (representing the data) and inductive reading (changing magnetic flux due to the motion of the medium past the head resulting in an induced voltage or current) (Mcfadyen, Fullerton and Carey, 2006) when flown across the surface of the disk. Inductive head detects the magnetisation on the disk medium through the induced EMF according to Faraday’s law of induction (Harrington, 2003).

An inductive head responds to the time rate of change of the magnetic flux (changes in magnetic transitions). It senses the change in magnetic flux flowing through the head core as it flies along the surface of the HDD medium thereby differentiating the flux on the medium. The output voltage is proportional to the change in magnetisation of the medium over which the head is flown and also dependent upon the head-to-medium velocity (Taratorin, 1996). However, as areal density increases, continuous scaling of the media to support capacity results in weaker magnetic flux produced by smaller bits and smaller disk with lower linear velocities. The readback signal from the inductive head becomes very weak to provide adequate signal-to-noise required to detect the recorded data. Thus, inductive heads becomes less attractive for high density magnetic recording application.

The switch from inductive heads to MR read heads by the early 1990s mark a turning point in the history of magnetic recording. Tremendous amount in increase in areal density was achieved

using the MR read head technology. Unlike inductive heads assembly, MR heads assembly consist of two separate heads: an inductive write head for writing the data, and a MR read head for reading data all on a single assembly. The MR heads operates based on the anisotropic MR principle, in which change in resistance occurs due to changes in magnetisation field (Vopsaroiu, Blackburn and Cain, 2007). MR heads are more sensitive than inductive heads (since they detect only the magnetic flux flowing through the head) and produced large signal amplitude during readback. Another advantage of MR heads is that the output voltage from the Read head is independent of the head-medium velocity. This makes it suitable for reading smaller disk with lower linear velocity. Also, the fact that the Read head is completely independent of the wider write head which writes on wider tracks, interference from adjacent tracks can be reduced during the readback process due to narrow Read head (Kryder, 2005).

MR read heads are relatively smaller in size compared to inductive heads and are therefore suitable for high density recording since media scalability is no more a concern. Because of their smaller size, they are usually placed in between shields that protect them from the effect of magnetic fields emanating from the inductive element of the write head.

A more powerful form of MR read heads is the Giant magneto resistive (GMR) Read head introduced into HDD industry in 1997. The GMR effect or spin-valve ((Mcfadyen, Fullerton and Carey, 2006) is based on the principles whereby the magnetisation between two adjacent magnetic layers is used to control the current flowing through a device. The word “giant” is used to qualify the magneto resistance effect in comparison to the MR heads. Data is readback from the disk by measuring the stray fields originating from the transitions between regions of opposite magnetisation. The output voltage from the GMR heads is significantly larger than the output from MR heads. Thus, about more than 100% improvement in areal density can be achieved with GMR heads (Hattori, Suzuki and Sugaya, 2011). A more recent Read head

technology introduced is the tunnel magneto resistance heads although it is still undergoing improvements.

1.5 Magnetic Media Recording Technologies

In magnetic recording systems, the recording mode is categorised based on the direction of magnetic field magnetisation in relation to the direction of head motion or the plane of the disk media. Depending on the mode in which the recording medium is saturated, three modes of recording data can be identified. These are Longitudinal, Transverse and Perpendicular magnetic recording (Hoagland and Monson, 1991).

Using the Longitudinal magnetic recording (LMR) mode, data are stored in such a way that the direction of the magnetic field is parallel to the plane of the medium and to the direction of head motion relative to the media. This is to say, the magnetic bits representing the data are aligned horizontally along the medium plane. For over 50 years, LMR technology was the dominant recording technique used in commercial HDD up to the year 2005. However, due increasing demand for higher areal densities, it quickly reached the maximum areal density it can support ($140GB/in^2$) (Chen et al., 2003) and became unstable thus, approaching the superparamagnetic limit (Leonhardt et al., 2001).

In Transverse magnetic recording (TMR) mode, the direction of the magnetic field is along the plane of the media surface but perpendicular to the direction of motion of the head relative to the media surface. This recording mode was not adopted because it does not present any significant improvement over LMR technology (Hoagland and Monson, 1991). This why it was very unpopular compared to the other recording technologies.

As the quest for higher capacity HDDs and high areal density recording kept on increasing beyond the limit in which the traditional LMR media can support, PMR was re-introduced as

an alternative that provides more stability and support for higher areal densities. The technology was first proposed by (Iwasaki, 1980) as a method of increasing recording density. In this method, a change is made in the orientation of the magnetic bits and the geometry of the writing process. The direction of the magnetic field is normal to the direction of the medium motion. Magnetic bits are stored on the medium pointing upward or downward perpendicular to plane of the HDD plate. This arrangement allows shrinking of the writing area and aligned the bits closer together due the attractive force between opposite charges, thus improving thermal stability of the bits and recording density. With the soft magnetic underlayer (SUL) beneath the recording medium, the monopole write head produces a strong stringing write field in the short gap between the pole and the SUL. This field generated is almost twice as strong as the field generated by LMR head for the same material. Thus, materials with higher coercivity can be used for greater media stability. Also, the presence of the SUL improves the readback signal strength and reduces the interference due to neighbouring tracks (HGST, 2007).

However, PMR and LMR modes can be used interchangeably to complement each in the HDD industry, LMR mode is employed mostly when dealing with analog signals, while PMR mode is more suited for digital signals (Iwasaki, 1980) (Awad, 2013). More also, the detection process is similar for both signals only that in LMR, bits transitions are sensed by the Read head, while in PMR the head sensed the bits not the bit transitions (Leonhardt et al., 2001). Figure 1.6 shows an illustration of LMR and PMR recording methods.

The following are some of the advantages of perpendicular magnetic recording over longitudinal magnetic recording:

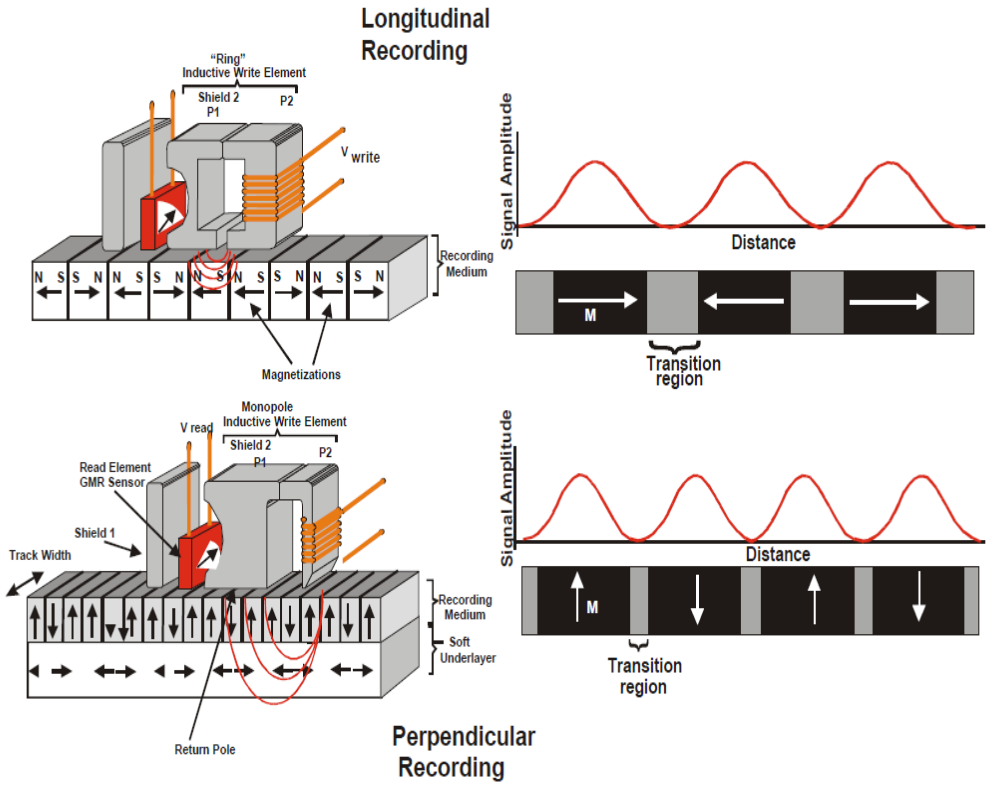


Figure 1.6: Longitudinal Magnetic Recording (LMR) Technology and Perpendicular Magnetic Recording (PMR) Technology (Hitachi, 2000).

I. The magnetic field generated by the write head in perpendicular recording is twice as that generated in longitudinal recording (Victoria, Senanan and Xue, 2002) hence improving writing efficiency and increase in areal densities.

II. The orientation of bits in the perpendicular magnetic recording allows for attractive force to exist between adjacent bits thereby ensuring high stability at high-density recording.

III. The demagnetization field vanishes at the centre of the transition in perpendicular recording resulting to narrower transitions (Cain et al., 1996). This translates to higher areal densities.

IV. Giant magneto-resistive head employed for longitudinal recording can also be applied to perpendicular magnetic recording (Leonhardt et al., 2001).

Due to the numerous advantages offered by the perpendicular magnetic recording especially thermal stability and the potentials for higher density recording, PMR has been adopted as standard for hard drives industry up to today.

However, the main obstacle towards achieving higher areal densities beyond the conventional limit with the PMR system is the instability of the medium as the magnetised area keep shrinking and the superparamagnetic limitations.

1.6 Media Trilemma and the Superparamagnetic Limit

Increasing the areal density of magnetic HDDs in order to support the continuous demand for high capacity data storage requires continuous scaling of all the relevant physical dimensions making up the magnetic HDDs system. These include; the bit size, the media grain size, the write head dimension, media thickness and the Read head geometry. However, continued scaling of the current conventional magnetic recording (PMR) media has some limitations which preclude the continuous areal density growth. One of such limiting factor is the size of the write head, which mechanically is larger than the MR read heads.

But the major challenge has to do with the physical magnetic anisotropic properties of the thin film magnetic recording layer. If the write head size is reduced, smaller write heads will produce a weaker magnetisation field which effectively confined the writing field to affect only a small writing region. This becomes more difficult for the magnetic field produced to flip the grains changing the magnetisation of the region. This problem is termed as the **write-ability constraint**. But the write-ability issue can be tackled by lowering the coercivity of the magnetic media using a low coercive HDD material. However, this affects the thermal stability of the

magnetic grains of the medium as small vibrations due to thermal fluctuations even at ambient temperature will destroy the magnetisation of the grains or flip the grains position. This problem is coined the **thermal stability constraint**. These two problems can be resolved by either using a HDD medium with very high coercivity or finding a means of increasing the strength of the magnetic field generated by the write head. But strong writing field means the field effect will spread a large distance from the actual bit position. Hence, this creates a significant amount of interferences between adjacent bits thereby reducing the Signal to Noise Ratio (SNR). This problem is called the **SNR constraint**. These three compelling constraints are coined the **media trilemma** (Chan et al., 2010) of the magnetic recording media. The media trilemma imposes a limit known as the **superparamagnetic limit** (a point where the media grains becomes highly unstable even at temperature below the Curie temperature) which precludes the continuous scaling of conventional magnetic HDD technology to higher areal densities.

Beside the media trilemma, another important key parameter that is at the heart of all limits towards ultrahigh density recording is the grain size of the magnetic material. Magnetic grains are the tiny contiguous irregular sized portion of the disk platter that forms the magnetic media. A bit of data (either 1 or 0) is stored by flipping (changing the magnetisation state) a grain within magnetic medium. Therefore, a grain can be regarded as the smallest unit of the magnetic particle that can be magnetised with a unique magnetic field generated by a write current. This means, at least a minimum of one or more grain particles are needed for an information bit (1 or 0) to be recorded on the magnetic media. Ultrahigh density recording requires grain size reduction through refinement of the magnetic materials to increase areal density. An average grain size of about 10 nm (Abdulrazaq, 2017) was achieved through material refinement. Consequently, putting all the odds together (grain size and the media trilemma), the highest

areal density that can be achieved with the current conventional HDD technology is estimated to be 1Tb/in^2 (Wood, 2000).

1.7 Future HDD Recording Options

The superparamagnetic limit has technically stalled the areal density growth of the current magnetic recording media and puts a barrier towards achieving high capacity expansion for ultrahigh density recording. In order to break this barrier and to continue the areal density growth beyond the superparamagnetic limit, either a new recording technology option has to be introduced, or a way of redefining the use of the current technology has to be found.

Among the candidate's technologies proposed for extending the areal density growth of the magnetic HDD beyond the current limit and continued capacity expansion of HDD capacity are, Energy Assisted Magnetic Recording (EAMR), Bit Patterned Media Recording, Shingled Magnetic Recording (SMR) and Two Dimensional Magnetic Recording (TDMR) (Shiroishi et al., 2009). Each of these four technologies approaches the media trilemma issues and circumvents the superparamagnetic limits from different individual perspective.

1.7.1 Energy Assisted Magnetic Recording

EAMR in the form of heat assisted magnetic recording (HAMR) (Kryder et al., 2008), or microwave assisted magnetic recording (MAMR) (Zhu, Zhu and Tang, 2008) addressed the write-ability/thermal stability problem of the media trilemma. By using a heat source in the form of laser or microwave energy, heat is injected onto the recording media to soften the magnetic medium when writing the data. The heat raised the temperature of the magnetic medium above the Curie temperature where the coercivity of the medium is below the magnetic field applied by the write head. After writing the data, the media is instantly cooled off back to

its initial state. This means that the coercivity of the medium need not to be reduced because the weak magnetic field from the write head is compensated by the heat injected onto the media to aid the writing process. Also, the thermal stability of the medium is kept intact as the media cooled off after the writing process. An estimated areal density of 100Tb/in^2 is projected to be achieved in the near future when the technology of the HAMR materials fully materialised (Kryder et al., 2008).

However, this new recording technology has some drawbacks. One of the drawbacks is the development of new media with appropriate thermal and magnetic properties that can withstand fairly high temperatures produced by laser or microwave heating. This requires enormous amount of resources and time. There is the requirement of extra energy for the writing process. This raised the energy consumption of storage systems especially large-scale storage systems used for enterprise applications thus, increasing the cost of operations. Another drawback is the need for write head redesign to accommodate the heat source and to withstand high temperature during the writing process. There is also the need for thermal heat confinement management and new type of lubricant capable of withstanding high temperature (Shiroishi et al, 2009), (Wood et al., 2009).

1.7.2 Bit Patterned Media Recording

BPMR approaches the media trilemma issue by addressing the SNR problem through redesign of the media such that data bits are recorded on a well-defined isolated magnetic island. Each bit magnetisation is stored on a single isolated magnetic island so that bit positions are made isolated from each other. This allows more bits to be placed on the media thereby increasing the media areal density. The non-magnetic material placed in between the magnetic islands provides adequate separation of the bits magnetisation position. This reduced the interference

between neighbouring bits (Wu, Armand and Cruz, 2014) thereby improving the SNR of the medium and allow continues scaling of the medium grain size.

The BPMR technology faces some challenges which make it very difficult to implement on a larger scale. One of such challenge has to do with the problem of write synchronization which can introduce written-in error (Wu, Armand and Cruz, 2014) into the system whenever there is a loss in head timing. This is due to the fact that, the head must be aligned to locate the precise position of the island to which the data is to be written onto or read from during the write and read processes. Any deviation of the head from the island position due to movement of the device, or variation of island positions due to manufacturing error can cause fatal errors which degrade the performance of the whole system. The other challenge is finding a way for the mass production of tiny well defined patterned isolated magnetic islands on the media cheaply (Shiroishi et al., 2009), (Chan et al., 2010), given that the whole media stage need to be completely redesign in order to accommodate this new technology.

1.7.3 Shingled Magnetic Recording

An alternative to HAMR and BPM towards achieving higher density recording is the SMR. SMR has the advantage of retaining the conventional media structure of PMR system without the media redesign, thus being easy to implement and more desirable to manufacturers. Only small modifications in the writing process and signal processing aspect is needed. SMR approaches the media trilemma by addressing the write-ability and stability constraints while finding a way to deal with the SNR problem. The idea behind SMR is to eliminate the guard bands between the data tracks (shrink the channel bit cell) by overlapping data so that the tracks are placed closer together in order to increase the recording density. The overlapping tracks results in a much narrower track width compared with the originally written width. A

conventional Read head could then be easily employed for readback although with reduced signal energy (Wood et al., 2009) due interference between tracks.

However, due to change in the writing operation mode of the media, one of the major drawbacks of the SMR technology is the lack of update-in-place operation on the written information (Shiroishi et al., 2009). This is because any change made on a single track will affect the neighbouring tracks and the bit that are packed closely together.

Moreover, as the recording density is increased, the shingling becomes more aggressive and the interference across the tracks becomes much more severe. The readback signal is degraded as conventional one-dimensional codes and detectors cannot handle the interferences across the tracks direction (Chan et al., 2010).

1.7.4 Two Dimensional Magnetic Recording

A more robust technology towards higher density recording other than SMR was the TDMR proposed by (Wood et al., 2009). TDMR achieves higher areal density by utilizing both SMR and 2D readback signal processing. The guard bands between the data tracks are eliminated by squeezing the tracks. This result in a significant interference across tracks referred to as crosstalk (Srinivasa, Chen and Dahandah, 2014). Using smaller Read head avoids crosstalk, but at the expense of less signal energy (reduced SNR) captured from the Read head. A wide Read head is employed to maximize the SNR by capturing signals from multiple tracks. Advanced 2D coding and signal processing algorithms are used to recover the signal (Wood et al., 2009).

The 2D read back signal processing algorithms uses the inter-track interference (ITI) and Inter-symbol interference (ISI) to make a final decision about the overall signal (Shiroishi et al., 2009). This enables higher areal density to be attained with improved performance in signal

detection. This however results in reasonable complexity in decoder/detector design. Figure 1.7 shows the illustration of the four technology alternatives for future magnetic recording systems.

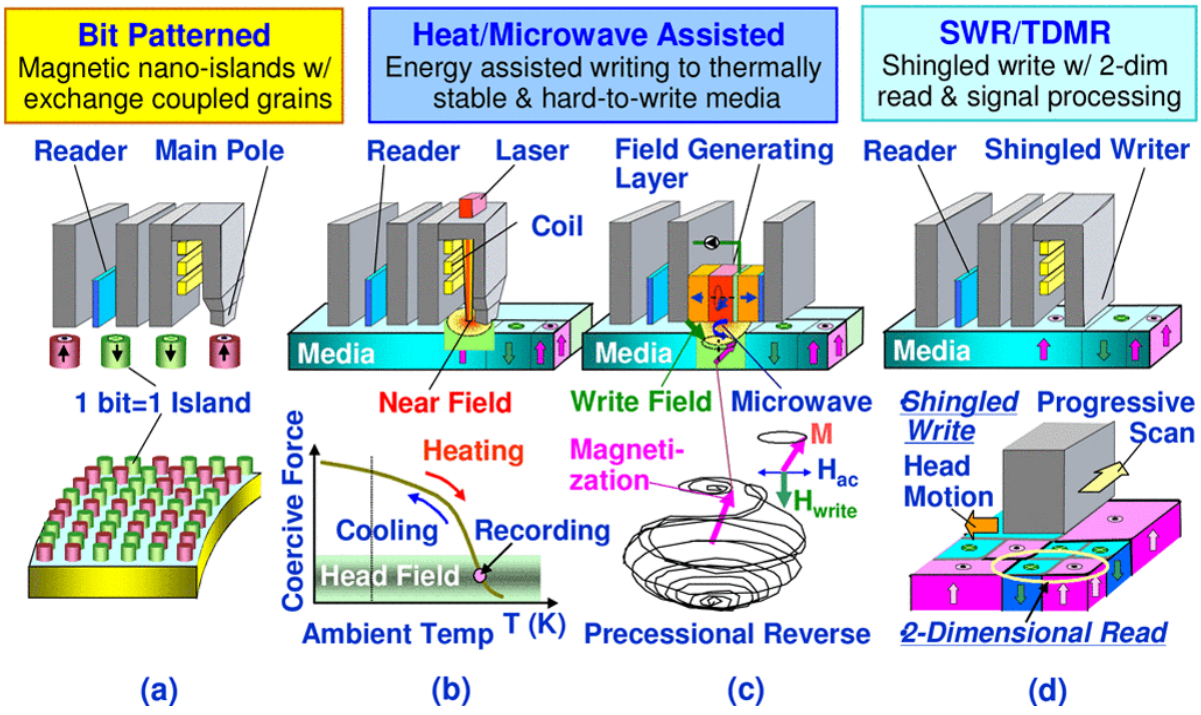


Figure 1.7: Candidate technology options for future magnetic recording system (Shiroishi et al. 2009).

1.8 Codes for Magnetic HDD

The magnetic recording channel suffers from various channel impairments and distortions similar to any digital transmission system. These channel impairments such as electronic noise, media noise and other channel distortions introduce errors and detection failures into the system which significantly affects the integrity and reliability of the recorded data. Therefore, to ensure that the recorded information is recovered from the media with no or less errors, channel coding is employed to improve the efficiency and reliability of the recording channel. Codes are used for timing synchronisation purposes, interference reduction, error correction, and other purposes. They generally add an overhead to the user data sequence and introduce a redundancy into the coded stream. This systematically affects the raw capacity of the HDD due to the fact

that there are always gains or losses in capacity due to application of coding. There are two forms of codes used for HDD application. These two forms of codes are explained below.

1.8.1 Modulation codes

In order to read data out of the magnetic disk correctly, the read data must be perfectly synchronised with the written data to achieve such objective. The clocking system is responsible for providing adequate timing in order to achieve a perfect synchronisation. Clocking from the data require adequate transitions to occur frequently from one bit to another, to make sure there is sufficient energy for the timing circuit to provide regular clocking update. This is because if there is a long run of a single bit, the timing will be lost and the system may deviate from the write timing.

Modulation codes or recording codes as they are sometimes referred to are used in magnetic HDD system to avoid detection failures, and to combat timing and synchronisation errors caused due to timing instability where an insertion or deletion of a symbol may occur (Ahmed, 2003), (Levenshtein, 1966), (Bertram, 1994). Modulation codes bring structure into the data stream by imposing a constraint on the user data which best fits the characteristics of the recording channel. A constraint imposes a restriction on the set of data sequences that are permissible to be transmitted on recording channel. A popular modulation code used in the magnetic media for many years is the Run Length Limited (RLL) code.

RLL code is used to ensure that magnetic transition changes at least once within a certain number of channel bits, and also to constrain the minimum separation between transitions during the recording process. This reduces interference between transitions and allows more data to be compress on the disk (Abdulrazaq, 2017), (Immink, 1990). The RLL code limits the runs of zeros in the user data sequence and also specified the minimum number of zeros in

certain data sequence. RLL codes are constructed or defined by the parameters as RLL (*d, k, m, n, r*) or RLL (d, k) for short, where:

d = minimum number of consecutive zeros allowed (plus clock).

k = maximum number of consecutive zeros allowed (plus clock).

m = minimum number of data bits to be encoded.

n = number of code bits (plus clock) for each of the m data bits.

r = number of different word lengths in a variable length code [40].

RLL code with parameter RLL (1, 7, 2, 3, 1) or RLL (1, 7) is a very popular code used in the magnetic storage media. This code has a rate 2/3 meaning that it takes in two user data bits and coverts them into a three codeword sequence. Table 1.1 shows the mapping of user data bits into a RLL (1, 7) code.

Table 1.1: RLL (1, 7) mapping Table (McLoughlin, 2011).

Data nibble	RLL (1, 7) code	Data nibble	RLL (1, 7) code
00	101	00 00	101 000
01	100	00 01	100 000
10	001	10 00	001 000
11	010	10 01	010 000

When encoding set of bits using the RLL (1, 7) encoding scheme, the encoder looks at the set of bits ahead to see if it can be found on the first column on the right-hand side of the table. If it exists, it will use it or else it uses left side of the table to map the first two bits. The RLL (1, 7) code has density ratio of 1.33, which allows more compression of data thereby increasing

the recording density by a factor of 1.33. However, the disk capacity is reduced by a two-third factor due to the coding rate.

1.8.2 Error Correction Codes

Errors are inevitable in any kind of digital transmission system despite all the necessary measures and precautions taken to avoid them. In magnetic storage systems, errors occur due to electronic noise, media noise, and also due to interferences. These errors degrade the quality of the recorded data. For magnetic recording system, due to the enormous amount of writing and reading of data done on the disk, the error rate requirement for the recovered data has to be kept very low (10^{-12} to 10^{-15}), compared to other digital communications system such as wireless communications with error rate requirement of 10^{-6} (Wu, 2009), (Wang, 2014). Therefore, a mechanism is put in place to make sure that user data are coded in such a way that errors is the system are easily detected, identified and possibly corrected. This mechanism is called Forward Error Correction (FEC), and the codes involved are referred to as Error Correction Codes (EEC).

The aim of ECC is to introduce a redundancy into the original message symbols, so that the receiver can exploit the redundant symbols and their relationship with the information symbols in order to correct errors that may occur during transmission or storage. The addition of the redundant symbols with the information message formed what is referred to as a coded sequence or codeword (Morelos-Zaragoza, 2006). The redundant symbols are usually appended at the rightmost part of the codeword if systematic mode of encoding is used. However, the leftmost part of the codeword is occupied by the k information symbols as illustrated in Figure 1.8.

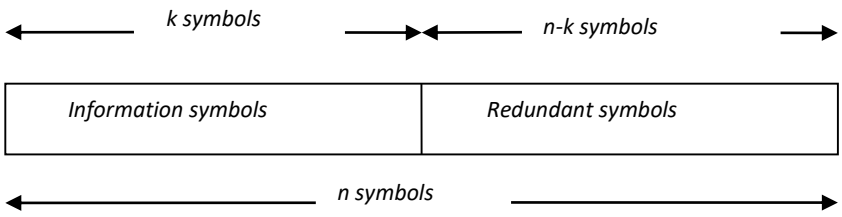


Fig. 1.8: Systematic block encoding of ECC

Error correction codes are classified according to the manner in which the redundant symbols are added. They include block codes and convolutional codes.

In the early days of magnetic recording, Reed-Solomon (RS) codes were the most popular forms of ECC used as FEC mechanism in the storage media. This is because of their ability to detect and correct random and burst errors introduced into the recording system (Immink, 1990). RS codes are block codes that groups the data bits into blocks and encode them using algebraic equations. At the receiving end, these equations are checked to detect any error in the blocks. If an error occurs within the blocks during transmission, the equations will not be satisfied. Correction is done by implementing an algorithm that chooses a codeword that is closest to the received code satisfying the algebraic equation. With hard decision decoding, RS codes are very well defined and simple to implement.

Nowadays, Low Density Parity Check (LDPC) codes are on their rise as they gain more popularity in the field of magnetic recording. They are gradually replacing RS codes as ECC for magnetic HDDs due their near-capacity approaching performance (Wu, 2009), (Soriaga, 2005). Encoding is done through the interconnection of many simple sparse parity check equations. These are then decoded iteratively using message passing algorithm. LDPC codes are easy to decode and can be parallelised easily for fast processing (Abdulrazaq, 2017). However, LDPC codes have some drawbacks. One drawback is due to the iterative decoding, as its performance is sub-optimal because of the dependency on the number of iterations

performed. Another drawback is of complex encoding for normally good performing codes (Han, 2008).

As the same case with modulation codes, FEC generally reduce the raw capacity of the HDD due to additional bits required to form the parity check equations. However, it makes the storage system more resilient to noise and interferences and gives room for more data to be compressed.

1.9 Methodology

A numerical approach has been undertaken for analysis of the work presented in this thesis. The main channels of interest are the conventional PMR and SMR readback channels. Various numerical models have been developed and simulated using the C/C++ programming language under GNU C compiler. Perpendicular magnetic recording channel has been simulated using the *tanh* transition response approximation and was modelled using the jitter noise channel model. Shingled based perpendicular magnetic recording channel has been modelled and simulated using the same convention PMR media with modifications to the write and readback processes.

Various blocks were developed under C/C++ language and were put together to create a full conventional perpendicular/shingled based perpendicular magnetic recording channel. A generic simulation model block adopted for this thesis is shown in Figure 1.9. Each block shown in the generic model performs a specific operation that constitute part of the entire readback process.

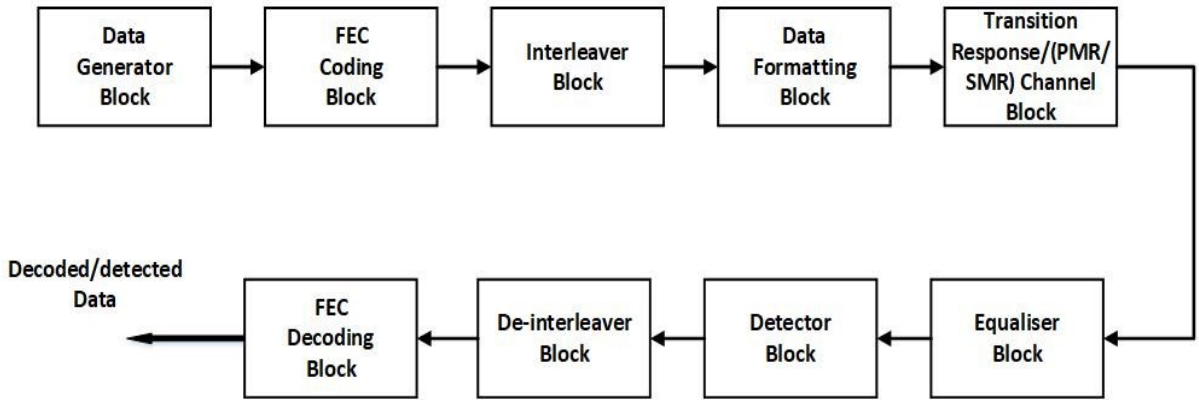


Figure 1.9: Generic Simulation Model Block

The blocks shown in Figure 1.9 are explained as below:

1. Data Generator Block: Generates random Data (0, 1) of length 4096 per track for 8 tracks as information to be recorded on the magnetic media.

2. FEC Coding Block: encode information bits using single parity check constraint. Even and Odd parity check constraint are implemented using this block to serve as error correcting and modulation codes.

3. Interleaver Block: Dithered relative prime (DRP) or Matrix/Square interleaver is implemented in this block.

4. Data Formatting Block: This block converts data into suitable format NRZ-L/NRZ-I data for transition.

5. Transition Response/Channel Block: This block provides the transition response approximation of simulated channel and modelled the channel into the form of conventional PMR with jitter noise and ISI or 2D SMR with jitter noise and 2D interference noise (ISI and ITI). Electronic white noise is also included in this block.

6. Equaliser Block: Depending upon the simulated channel, the equaliser would be 1D PR or 2D GPR equaliser.

7. Detector Block: This block creates the trellis which is used for the application MLSD/MAP detection algorithms. 1D MAP joint detector-decoder or 2D MAP joint detector-decoder is implemented in this block depending upon the simulated channel.

8. De-interleaver Block: The de-interleaving algorithm is generated in this block to reverse the arrangement of the bits position depending upon which interleaver is implemented.

9. FEC Decoding Block: This block provides decoding of single parity code.

1.10 Thesis Outline

This thesis covers various topics of interest in conventional PMR and SMR/TDMR systems. It includes equalisation, application of error correcting codes for both PMR and SMR channels, GPR target selection for PMR media, joint detection-decoding, improvement in detection techniques for PMR and TDMR systems and 2D TDMR detection-decoding using parity along and across track. The aim and objectives of this thesis are as below:

1.10.1 Overall Aim

The aim of this thesis is to study the detection and decoding techniques implemented in *conventional PMR and SMR media* in order to achieve near perfect readback from the magnetised media and use parity coding to improve the performance of magnetic recording.

1.10.2 Objectives

The main objectives set towards achieving the stated aim of this work are discussed as below:

1. Investigation and implementation of PRML readback system on conventional PMR media as a mechanism for extracting data from the magnetic media. This is divided into the following:

- Design and simulation of PMR channel with 1D interference (ISI along track), jitter noise and AWGN representing electronic noise and other important noise in the channel

- Implementation of PR equalisation using a PR equaliser to reshape the readback data into the desired target response.

- Development and implementation of PRML detectors based on Viterbi algorithm and Balh Cocke Jelinel Raviv (BCJR) algorithm for the detection of data on the PMR channel.

- To search for best equaliser target response and equaliser length with optimal Bit Error Rata (BER)/Frame Error Rate (FER) performances at different data density for the PRML detectors.

2. Investigation and implementation of SMR/TDMR system as a candidate technology for future high density magnetic recording using conventional PMR media platform with modifications to the writing and readback process.

3. Application of single parity-based coding approach to conventional PMR and SMR/TDMR channels as a form of error correction coding and modulation code.

4. Investigation and implementation of low-complexity 2D detection scheme for multi-track TDMR system in order to reduce the detection complexity of full 2D ML detector from exponential to linear order with number of tracks involved.

5. Development and implementation of joint detection-decoding on conventional PMR media and 2D TDMR joint detection-decoding using parity along and across track.

This thesis report is organised into seven (7) chapters. The remainder of the thesis is divided into the following chapters;

Chapter 2 presents reviews of literatures on channel models for TDMR/SMR channel modelling and the magnetic medium in general, an introduction to TDMR/SMR technology architecture and challenges of implementing the technology. It is also present an overview of signal processing techniques for magnetic recording channel and reviews of literatures on coding, equalisations, detections and decoding algorithms implemented in this research work.

Chapter 3 presents modelling and implementation of partial response maximum likelihood (PRML) read channel system on PMR media as a mechanism for data recovery from the magnetic medium. As part of the data recovery system, PR equaliser design and implementation, coupled with PRML detectors based on Viterbi and BCJR algorithm Implementation are also presented. The performance analysis of the PRML detectors based on VA and BCJR algorithm for the PMR channel is also given in this chapter.

Chapter 4 presents a FEC coding system with a novel joint detection decoding scheme based on single parity coding and constrained MAP detector for a magnetic recording channel with PMR media. Design and implementation of single parity bit encoders and interleavers with 1D MAP decoder is also presented in this chapter. Performance evaluation of Generalized Partial Response (GPR) target length 4 for different data densities along track is presented and the best target is selected for the proposed FEC coding and joint detection decoding scheme. The performance of the FEC coding system with the joint detector decoder for 1D PMR channel is analysed with different interleaver configuration when decoding of first parity bits is designed based on either MAP or MLSD criterion.

Chapter 5 gives the modelling and implementation of TDMR system with shingled write based PMR media for two-track channel interference and target length 4. Modelling of inter-track interference, jitter noise, Inter-symbol interference and AWGN representing electronic noise and other noise sources is also presented. The design and implementation of 2D equaliser and 2D multi-bits detector for joint track detection of the TDMR Channel using 2D MAP detector along track and regular MAP detector across track is also presented in this chapter. Performance evaluation of the design and computational complexity of the detection technique is analysed with comparison made to other detection techniques is given in this chapter.

Chapter 6 describes the application and implementation of FEC coding using single parity check codes for TDMR channel. Two single parity check coding systems for FEC implementation are presented. The first implementation utilises the addition of two single parity codes along track separated by DRP interleaver, while in the second implementation, the single parity codes are used both along track and across track without DRP interleaver. A novel 2D multi-track MAP joint detector decoder for simultaneous detection and decoding of parity bits on the same trellis is also presented. The 2D joint detector decoder reduced the detection complexity while at the same improves system performance.

Finally, chapter 7 provides thesis summary, conclusion and recommendations for future work.

1.11 Contributions to Knowledge

This thesis covered many aspects of coding, detection and decoding techniques for both conventional PMR media and TDMR with shingled write-magnetic recording media. The work done by the author has led to the following major contributions to knowledge.

1. A new FEC scheme using concatenated interleaved constrained single parity bit systems for improving the performance of perpendicular magnetic recording channel was introduced and published.
2. A joint detection-decoding scheme utilising BCJR algorithm on a trellis was introduced for simultaneous detection and decoding of data with concatenated interleaved constrained single parity bit systems.
3. 2D detection scheme by concatenating multi-level 2D MAP detector along track with regular MAP detector across tracks was introduced aimed at reducing the complexity of full 2D detection of TDMR system with SMR media.
4. Two coding approaches for FEC scheme utilising two single parity bit systems for improving the performance of TDMR channel were introduced and presented. These approaches exploit the simplicity of decoding single parity bit to achieve a remarkable coding gain with reasonable complexity.
5. A novel 2D multi-track MAP joint detection decoding scheme for simultaneous detection and decoding of data for TDMR channel on the same trellis structure was presented. The scheme evades the needed for a postprocessor stage or iterative detection decoding process, thereby reducing computational costs, and data processing delays.

A chapter-wise expansion of the above mentioned main contributions is outlined below:

Chapter 3

- The effect of equaliser taps on the performance of MAP detector in conventional PMR channel is presented and it is shown that, at lower ISI, equaliser with 9 taps is sufficient for to give a good performance. However, higher ISI, equaliser with taps 11 and above are needed for good detection performance.

- Symmetric GPR targets of length 3 performed better than their un-symmetric counter parts for the conventional PMR media. It is shown that, suitable targets for detection are found to be [4, 5, 4] for $T_{50} \leq 1.5$, while for larger values of T_{50} target [1, 2, 1] performs better.
- It is seen that the MAP detector outperformed the VA detector in terms of BER performance under same channel condition with a gain of around 3 dB.

Chapter 4

- The merit of combining interleaved single parity check coding and joint detection-decoding in conventional PMR media channel is highlighted. It is shown that a gain of about 3 dB was achieved at BER point 10^{-6}.
- The use of single odd parity bit system as a RLL (0, 6) modulation code and at the same time as error correction code is demonstrated. This helps to simplify the detection process and reduce decoding errors.
- For FEC using interleaved single parity bit systems, concatenating more than one interleaver with additional parity bits resulted in performance improvement only at higher data densities. It is not beneficial to concatenate more interleaves with additional parity bits at low data densities.

Chapter 5

- For an 8 track SMR/TDMR system with target length 4 and ITI of two tracks, the problem of full 2D joint-track detection of multiple tracks can be broken down into detecting smaller number of tracks together jointly using 2D MAP detector along track to remove ISI, then followed by regular MAP detector across track to remove ITI. This reduces the complexity order of joint-track full 2D detection from 2^{32} to $8 * 2^8$ for an 8-track system.

- It is seen that the performance of the detector using 2D MAP along track and regular MAP across track is best when the ITI from the side track is 100% for all ISI conditions.
- ITI target [1.0, 1.0] outperformed all other ITI targets at high data density along track because it has the highest minimum separation distance compared with rest of the targets.

Chapter 6

- The use of simple FEC scheme with single parity bit systems for TDMR is demonstrated and yielded good results. Reasonable gains (about 4.5 dB) in performances are recorded at situations where there is high ITI and ISI at the same time in the channel.
- It is shown that depending on the channel situation in relation to the amount of data densities or track densities considered, the single parity bit systems can be applied either along track with interleaver or in both directions without interleaver.
- In situations where there is low ITI, it is better to use FEC coding with single parity bit system applied along track and across track without the DRP interleaver.
- When high ITI is required (75% and above), where more data is compressed across tracks, it better to use FEC coding with two concatenated single parity bit systems along track separated by DRP interleaver.
- In situations where the channel interferences are high in both directions (high ISI and ITI), it is beneficial to use FEC coding with two concatenated single parity bit systems separated by DRP interleaver.
- The use of 2D multi-track MAP joint detector-decoder for combine signal detection and parity bit decoding in TDMR system is demonstrated to reduce detection complexity by selecting only the valid transition paths on the trellis.

Chapter 2

Magnetic Recording Channel and Signal Processing

This chapter presents a review of channel models developed in literatures for modelling of SMR/TDMR and the magnetic recording medium in general. An introduction to SMR and TDMR as alternative technologies for future magnetic recording systems is given in this chapter. This is followed by a detailed description of the SMR and TDMR system architecture and the challenges around the implementation of the technology. Following an overview of signal processing method for recording channels, the review of literature based on equalisation, coding and detection algorithms implemented in this research is presented. Finally, review of some similar works related to magnetic recording, SMR/TDMR systems, equalisation, 2D detection and coding is undertaken in this chapter.

2.1 Introduction

The magnetic layer of a HDD consists of small areas made of magnetic materials where information is being stored and retrieved on the disk. These small areas of magnetic materials consist of smaller magnetic grain particles that store data in form of magnetic bits. The magnetic

grains are magnetised either positively or negatively (North or South Pole), facing upward or downward direction to represent data bit 0 or 1.

In an ideal situation, the magnetic grains are supposed to be of regular size and of predefined shape. This is almost true in the case of low areal density magnetic recording, where the magnetic grains are assumed to have a desired regular shape and size. But at a very high areal density recording like in the TDMR system, where the media grain size is comparable to the channel bit, the magnetic grains have random irregular shapes and size and have significant effect on the quality of information stored on the media (Krishnan et al., 2009). Therefore, the nature of the magnetic grain particles has to be put into consideration for successful modelling of the read channel, writing and reading processes, equaliser and detector design, error correction coding and other signal processing aspects.

2.2 TDMR Channel Models

The magnetic grain is the smallest unit of the magnetic medium that is magnetised by a unique magnetic field to represent a given data bit. The TDMR system is aimed at storing one data bit per grain or even more in order to achieve areal density above 1Tb/in^2. Hence, it is implied that the channel bit area is of comparable size with the grain size. Also, since it was proposed that the TDMR is to retain the conventional media structure of the PMR system, then at areal density above 1Tb/in^2, the grain boundaries are randomly irregular and constitute the primary source of noise in the recording channel (Krishnan et al., 2009). Consequently, at high areal densities, the grains are randomly distributed across the recording medium causing significant interference from along track and across tracks direction. In this scenario, the Micro-track model proposed in (Caroselli and Wolf, 1996) is inaccurate and not reliable for TDMR studies.

Therefore, the need for the development of new channel models suitable for designing signal processing algorithms for the TDMR system.

In (Wood, 2000), two recording channel models were presented. The first model envisioned a recording medium grains that have finite number of predefined shapes. The second model however, viewed the recording media as a collection of randomly distributed irregular grains taking different forms of shapes and sizes to reflect a real medium representation. While the first model simplifies the channel modelling process and was suited for system capacity analysis, its lacks accuracy. The second model is a more accurate representation of the system, but its complexity rendered it difficult for performance analysis of detectors and coding schemes. Hence, a more elaborate channel model for TDMR systems that can provide a trade-of between accuracy and design complexity is needed. A variety of channel models for the TDMR system, each with degree of varying complexity and accuracy was proposed by (Krishnan et al., 2009). Figure 2.1 shows a spectrum span of TDMR channel model with varying degree of complexity and accuracy.

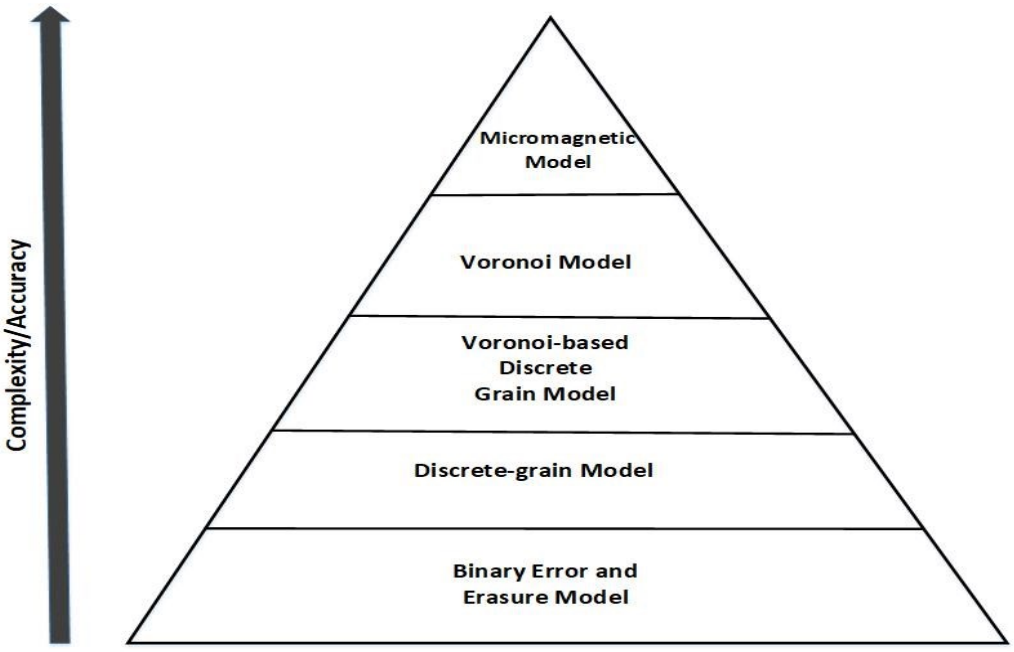


Figure 2.1: Spectrum span of the TDMR read-channel model (Krishnan et al., 2009).

The task of developing a model for the magnetic medium is divided into three distinct parts; first is the modelling of the magnetic medium grains, then modelling the writing process and finally modelling the readback process. Each of these processes is executed with varying degrees of accuracy and complexity. The next section will discuss how each of these processes applies to the Voronoi model (Caroselli and Wolf, 1996), (Todd et al., 2012) and its variants such as the Four Grain Rectangular Model (Krishnan, Radhakrishnan and Vasic, 2009) and the Grain Flipping Probability Model (Chan et al., 2009).

2.2.1 Four Grain Rectangular Model

The four-grain rectangular model is the simplest form of the Voronoi model that is less complex and very easy to implement. Because of its simplicity, it is well suited for capacity analysis of the TDMR channel. In this model, the magnetic grains are assumed to be not of the same size but have only four possible sizes, 1x1, 1x2, 2x1, and 2x2. Each of these possible sizes or shapes has a probability of occurrence defined to it. The magnetic grains are distributed randomly over the medium according to their probabilities of occurrence. This models the magnetic recording medium such that every portion of the disk is covered by a grain or part of a grain. Figure 2.2 depicts the grains size structures involved for the four-grain rectangular model.

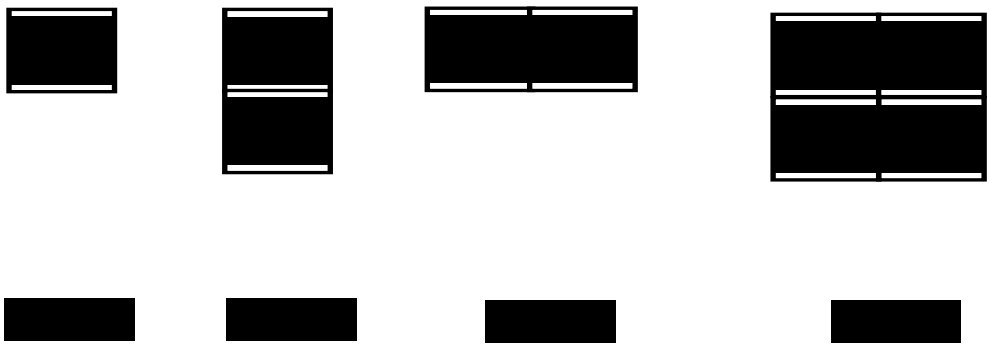


Figure 2.2: The possible shapes and sizes of the four-grain rectangular model.

The writing process is actualised through a raster scan head sweeping in a row-by-row fashion starting from the top-left cell of the medium, moving rightwards, and ends downwards at the bottom-rightmost cell (Krishnan et al., 2009), (Chan et al., 2009). In this scenario, a grain may be written once or more than once as grains spans more than one cell. The final magnetisation of the medium is taken from the last bit magnetised within the cell region. The depiction of ideal medium writing compared with the writing on a Four Grain Rectangular medium model is given by Figure 2.3.

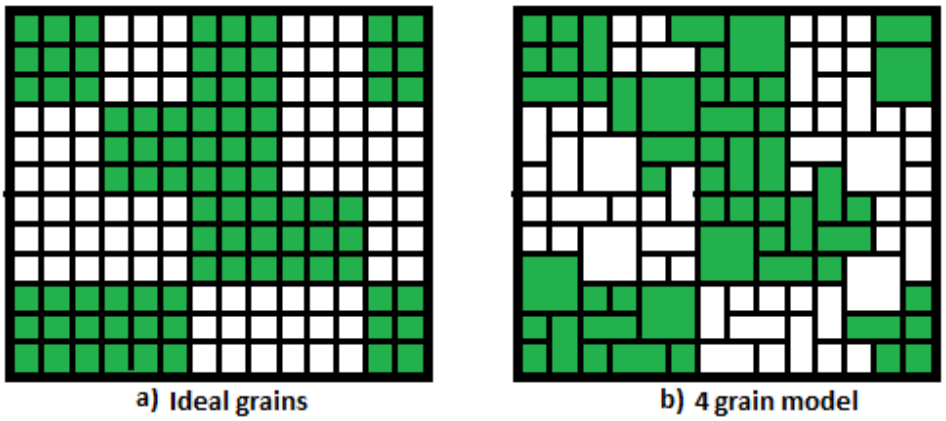


Figure 2.3: Magnetisation of an ideal grains vs four grain rectangular model, from (Abdulrazaq, 2017).

2.2.2 Voronoi Model

The Voronoi model provides a balance between complexity and accuracy of the recording medium. It is therefore used as a platform for the design of detectors and codes performance evaluation on the TDMR systems. In the Voronoi model, the recording medium is modelled as a collection of grains represented by random Voronoi regions of irregular shapes and size. There are many approaches on how to create the Voronoi media model proposed in literature. One approach adopted in (Krishnan, Radhakrishnan and Vasic, 2009) is to mark certain number of points on the medium randomly and then generate the Voronoi regions corresponding to each

point. The recording medium would now have as many grains as the number of points with large variations in grain sizes. To reduce the correlation in grain shapes and positions close to a realistic model, larger grains are divided, and the smaller ones are combined (Wood et al., 2009), (Chan et al., 2009). Although the method had a simple approach that presents a realistic medium model, it does not fully give an insight into the effect of noise due to irregular grain boundaries.

In (Krishnan et al., 2009) the recording medium is modelled by shifting the grain centres randomly from the cell centres to mimic the randomness in shape, size and position of the magnetic grains. By allowing the shift of the grain centres from their ideal position to have a Gaussian distribution, the grain centres are allowed to cross their corresponding bit-boundaries. This captured the noise characterisation observed in TDMR channel due to irregular grain boundaries.

A more elaborate approach on Voronoi based channel modelling for SMR media was proposed by (Todd et al., 2009). The Voronoi based model developed takes into account effects such as finite grain size, imperfections in the write process and interferences (both ISI and ITI). Initially, a random distribution of grain nuclei is created throughout the medium, with a specified average grain area (A) and a certain standard deviation (σ_A) of the area. The grains created (Voronoi regions) have large variation in grain size with σ_A greater than the desired value for the medium. To tune the σ_A of the grain area to the desired medium value, an iterative process is performed as follows:

1. The grain nuclei are replaced with the grain centroid so as to smoothen out the irregularities in the grain size distribution.

2. Grains with smaller area less than $A - 2\sigma_A$ are eliminated.

3. Grains with larger area more than $A + 2\sigma_A$ are split into two smaller new grains with their grain nuclei slightly offset from the original nucleus.

4. Steps 1-3 are repeated until the grain average area and standard deviation are sufficiently close to the desired target.

The boundaries between the grains are considered to be non-magnetic in nature. These are modelled by shrinking the grain areas obtained from steps 1- 4 above inward toward the nucleus by 10% (Todd et al., 2009).

Figure 2.4 shows the pictorial view of some grains plot sample, with the grains represented in black, grain boundaries in white, bit cell boundaries in yellow, and the centroids in green.

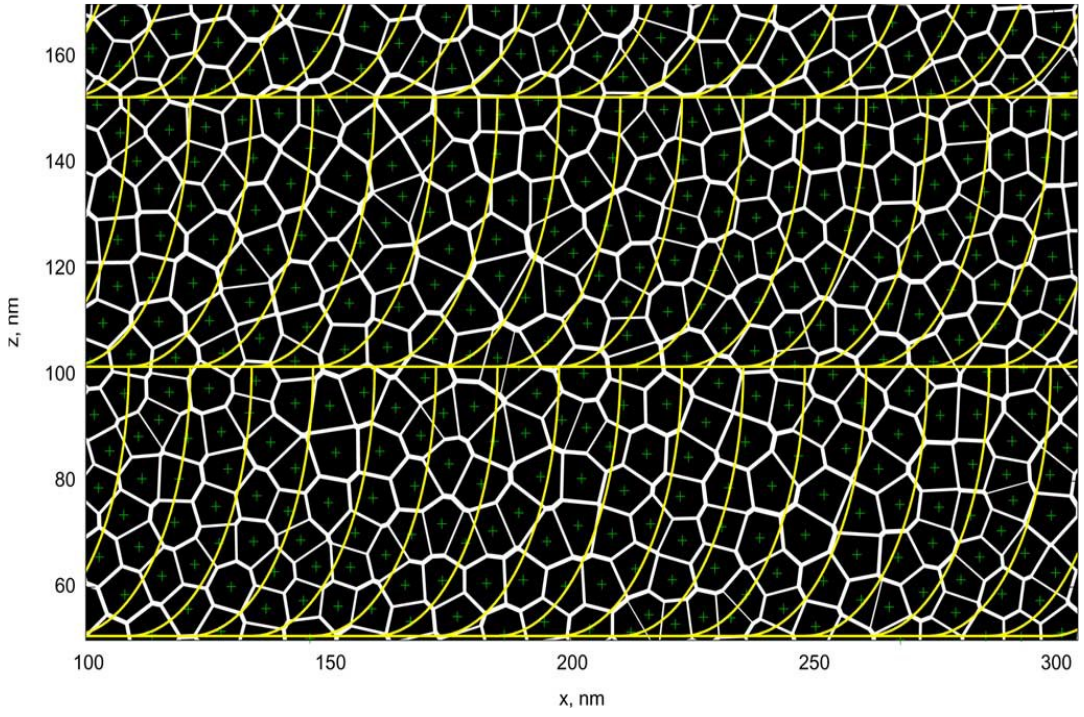


Figure 2.4: Sample of grain layout, with grain centroids (green), grain boundaries (white) and bit cell boundaries (yellow) with, ${}^{\sigma_A}/_{A} = 0.25$, 10 grains/bit and Bit Aspect Ratio=4:1 (Todd et al., 2009).

After modelling the grain distribution on the medium, the next task is to model the writing of the grains. This involves making decision on which grain gets magnetised by which bit and what polarity is to retain. Each grain is assumed to have an initial magnetisation associated to it that is ideally random.

The bits are written on the medium by magnetising the bit-cell regions associated to them on the media. A function is defined that gives the probability that a grain within a certain bit-cell region is magnetised to the value of the bit associated with the bit-cell or outside it. The function attached a small probability that grains in neighbouring bit-cell will get overwritten by bit that is already written. This function is used to determine which grains are successfully written (magnetised) and those unwritten (not magnetised).

The readback process is modelled by convolving the magnetisation of each bit cell region together with the response function of the Read head. Equation 2.1 gives the expression for the read data obtained from the disk during the read process.

$$y(v_1, v_2) = x(v_1, v_2) * h(v_1, v_2) \tag{2.1}$$

Where the term on the left hand side $y(v_1, v_2)$ represent the read data, on the right $x(v_1, v_2)$ and $h(v_1, v_2)$ are the bit magnetisation and Read head response function respectively. The asterisk (*) sign denotes the convolution operation. "v_1" and "v_2" are the data position along track and across track direction respectively.

In literature, the head transition response is simulated using three different approximations. These include, the hyperbolic tangent function (Wu, 2009), (Moon and Park, 2005), (Madden et al., 2004), a Gaussian function, and an error function (Erden et al., 2002), (Yang and Kurtas). The head transition response for a 1-D system using the hyperbolic tangent and error function is expressed by the equations 2.2 and 2.3 respectively.

$$s(t) = V_{\max} \tanh\left(\frac{2t}{0.5795\pi T_{50}}\right) \tag{2.2}$$

$$s(t) = V_{\max} erf\left(\frac{0.594t}{T_{50}}\right) \tag{2.3}$$

where V_{max} is the zero-to-peak (maximum) amplitude of the isolated response, T_{50} is the time taken for the transition response to rise from $-V_{max}/2$ to $V_{max}/2$, "t" is the sampling time or time separation of the magnetisation read with respect to the Read head centre position. T_{50} is normalised to symbol bit period. Since the speed of head rotation is considered to be constant for any HDD system, then the time taken for the head to move from one-bit position to another is directly proportional to the distance (Speed = Distance × Time). Therefore, "t" in equations (2.2) and (2.3) can denote either distance/position or time (Abdulrazaq, 2017).

The value of T_{50} significantly affects the areal density of the recording medium. Higher values mean high areal density as transitions are very close to each other, while lower values signifies low areal density (transitions are consistently apart from each other).

The dipulse response is obtained by the superposition of the positive and negative bit transition separated at one-bit period apart (Wu, 2009). Equation 2.4 represents the dipulse response of a two-dimensional head function with central two-dimensional Gaussian term and an overshoot Bessel function (Todd et al., 2012).

$$h(v_1, v_2) = \frac{\exp\left(-r_1^2/2\right)}{2\pi\sigma_{v_1}\sigma_{v_2}} - \frac{K_o(r_2)}{2\pi l_{v_1} l_{v_2}} \tag{2.4}$$

where;

$$r_1^2 = v_1^2 / \sigma_{v_1}^2 + v_2^2 / \sigma_{v_2}^2 \tag{2.5}$$

and

$$r_2^2 = v_1 / l_{v_1}^2 + v_2^2 / l_{v_2}^2 + \varepsilon \tag{2.6}$$

where "v_1" and "v_2" are positions in the along-track and across-tracks directions, K_o is a Bessel function of the first kind of order zero, σ_{v_1} and σ_{v_2} are parameters for controlling the width of the 2D central Gaussian part of the dipulse response in both directions (serve same purpose as T_{50}) , and ε is small term used to prevent singularity in the Bessel function at $v_1 = v_2 = 0$ (Todd et al., 2012).

Electronics noise and other noises of significant interest are modelled as White Gaussian noise and then added to the convolution of magnetisation to the channel response to form the final read signal.

2.2.3 Grain Flipping Probability Model

The Grain Flipping Probability (GFP) model is a variant of the Voronoi model that tends to have a more realistic approach in determining which grain is to be flipped. It uses the regular Voronoi cell structure but employs a statistical method in determining the probability of grain flipping base on micromagnetic simulations (Miles et al., 2003), (Chan et al., 2010). Compared to the regular Voronoi model, where grain magnetisation is decided based on whether the grain nucleus falls under influence of the Read head or not; the GFP model uses the probability of grain flipping in determining the grain magnetisation. The grain flipping probabilities are computed by running micromagnetic simulations at the medium characterisation stage and are stored in a look-up table (LUT).

Micromagnetic simulations are computationally intensive and very time-consuming but are an accurate way of modelling the evolution of the magnetisation of each magnetic grain particle during the write process. The simulations attached a flipping probability to each grain which tells how likely a grain is to flip under a given set of conditions per bit interval. Thus, this improves the reliability of grain magnetisation, and consequently gives a more realistic model of the recording medium. In (Chan et al., 2010), micromagnetic simulations are run to evaluate the GFP only at the initial phase of characterizing the medium. This avoids the delays associated with the constant running of these simulations after each write process.

The steps followed by (Chan et al., 2010) to characterize and use the LUT to generate the GFP model involves: First, grain magnetic parameters and tensor statistic information are generated and computed for the Voronoi medium geometry. Then, for a given head field, micromagnetic simulations are run on the media using the previously computed data for a range of bit patterns. This generates granular magnetisation of the grains in the medium as shown in Figure 2.5. The statistics from each simulation are used to characterize the flipping probabilities of

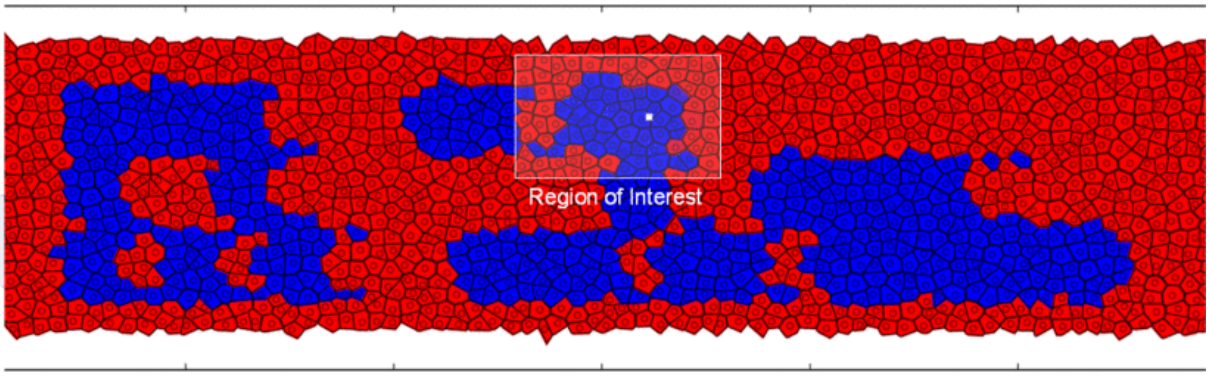


Figure 2.5: Grain magnetisations from micromagnetic simulation. The grains in red are positively magnetised while the grains shown in blue are negatively magnetised (Chan et al., 2010).

the grains, which are then stored in a multidimensional LUT. There are several parameters that have influence on the probability of grains flipping. These parameters have to be chosen

carefully in the order of their greatest influence on the probabilities. Finally, after populating the LUT, the information stored (in form of probabilities) is utilised to flip grains quickly.

2.2.4 Jitter Noise Model

The jitter noise model can be viewed as an alternative media model that accounts for the random nature of magnetic grains. It tries to capture the effect of random irregular grains sizes and irregular transitions that may occur due to irregular size/boundaries of the magnetic grains.

Jitter can be defined as a deviation in the read/write head position or in a bit boundary specifically due to randomness of the medium. As the head read/write mechanism has no prior knowledge of the media grains shapes and sizes (Krishnan et al., 2009), a situation may arise where the Read head jolts forward due to movement of the HDD and reads a bit ahead of the timing, or jolts backward and reads a bit later than the timing. This deviation in position affects the timing of the bits in the medium. The irregularity of the grains also creates another problem of grain boundaries. The boundary of the bit can extend deeper into the area where the bit is ideally supposed to be located, or the boundary may occur before the position the bit. This problem causes a shift in the time at which the head registers the magnetisation of the bit. Also, electronic noise generated by the timing circuit due to passive elements has some random effect on the read data. The deviations in timing due to the trio (position, electronic noise, and irregular magnetic grain) is termed timing jitter. Since timing jitter affects the timing position of bits, it is modelled as a random deviation in the time of transition of the Read head impulse response. Timing jitter also affects the magnitude or value of the readback signal waveform causing some changes from its ideal form. This changes in magnitude or value of the read signal due to the timing is termed the jitter noise (Du, Zhang and Ong, 2006).

In the jitter noise channel model, jitter noise is modelled as a random Gaussian variable representing the shift in transition positions due to the timing jitter. This is then added into the readback signal as shown in equation 2.7 (Wu, 2009).

$$y(t) = \sum_i d_i s(t + a_i - iB) \tag{2.7}$$

where a_i is random Gaussian variable representing the transition jitter; B is the channel bit spacing; $s(..)$ represent the Read head transition impulse response; "i" is a counter that counts through all the bits with ISI contribution to the signal at time "t"; and d_i represents the bit transition which is $+1$ positive transition (for transition from 0 to 1), -1 negative transition (for transition from 1 to 0), or 0 no transition (for transitions 1 to 1, or 0 to 0).

By applying Taylor's series expansion to equation 2.7, the interfering signal can be separated from the rest of the other noise signals contributed to the read signal from jitter noise and white noise sources as shown in equation 2.8.

$$y(t) = \sum_i d_i s(t - iB) + n_j(t) + n_w(t) \tag{2.8}$$

where n_j represents the jitter noise contribution and n_w is the Additive white noise contribution which consists of electronics noise, noise emanating from the Read head, and other sources.

The jitter noise variable (a_i) is assumed to have a White Gaussian distribution. In the magnetic recording medium, sometimes the channel bit can have a negative area when the bit boundaries at the starting or end of a bit experienced jitter in opposite directions. The boundaries tend to move inwards toward one another to an area that is physically impossible to simulate. To prevent this situation, a maximum limit is imposed on the amplitude of the jitter so that is will not exceed half of the bit period (Kovintavewat et al., 2002). When a limit of *0.5B* is put on the amplitude of a_i, the worst bit area to be recorded will happen when the leading boundary has

jitter of $-0.5B$ and the trailing boundary has $0.5B$. Then, the net area will have a value of $(0.5B - |-0.5| = 0)$. This is equivalent to total bit erasure where due to the irregular random grains, a bit is erased by writing the bits in its neighbourhood region. However, because of the limit put on the jitter amplitude, it viewed to have a truncated white Gaussian distribution (Kovintavewat et al., 2002), (Wu, 2009).

2.3 SMR and Two-dimensional Magnetic Recording

As a candidate technology for future recording systems, SMR envisioned some radical changes in the writing and reading process of the media, while maintaining the same media and head structure of the conventional recording system.

In conventional recording media, the write-head usually limits the continuous scaling of the bit size as smaller bits require smaller and sharper write-heads. This however, poses a write-ability problem of the medium. With SMR technology, the limitation of the write-head is overcome by heavily overlapping bits and data tracks. This allows a wider write-head to be employed for writing a series of overlapping bits and tracks such that, with the initial track overwritten, only a small portion of the adjacent track is left for data storage. This results in data tracks that are much narrower than the originally written track width, thereby allowing tremendous increase in areal recording density. Figure 2.6 depicts the writing of tracks using the Shingled-write process.

The large pole corner-edge writer produces strong writing fields that are directed towards the edge of the down-track and cross-track direction only, with no limit on the amount of flux reaching its corner. This generates much stronger fields that can penetrate the medium to a much greater depth (Wood et al., 2009) which allows easy magnetisation of the grains.

Using the SMR system depicted by Figure 2.6 offers some interesting benefits. One of them is the higher fields obtained from the corner head, which facilitates the media writing without the need for energy assist. Also, adjacent track erasure (ATE) which occurs due to repetitive writing of tracks in conventional media is no longer an issue. This is because in SMR, tracks are written sequentially, and each track only needs to survive a single overwrite from adjacent track (Chan and Elidirissi, 2013).

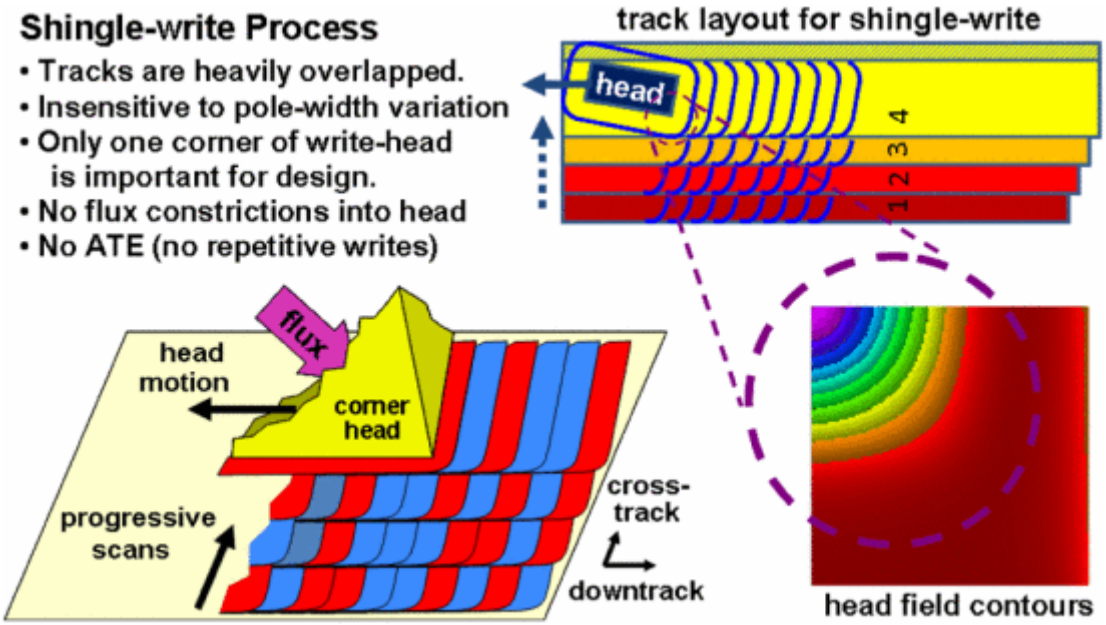


Figure 2.6: Shingle-write writing process (Wood et al, 2009).

However, the SMR architecture has to deal with the problem of interferences from both directions especially at higher recording densities. As shingling becomes more aggressive, the closely packed tracks make ITI more severe in addition to the ISI along track. This may lead to performance loss when 1D codes and detectors were to be used. Apart from the problem of increased interference, another significant drawback of the SMR system is the lack of an "update-in-place" mechanism, when a single track or portion of a track that was previously written need to be altered. This is because as a result of the shingled writing, updating a single bit or track will damage information on the adjacent track. Updating a track portion requires

rewriting of a whole sector that contains many tracks of subsequently written data, which slows down the writing speed and complicates the write process. Therefore, in order for this system (SMR) to flourish, a new data management protocol is needed for the operating software to work with the new update system (Amer et al., 2011), (Lin et al., 2012).

The SMR system can be deployed as standalone with conventional reader head and 1D codes and detectors or used together with 2D coding and signal processing techniques. When used as standalone, it can enable an areal density increase up to around 2 Tb/in^2 (Tagawa, 2009), (Greakes, Kanai and Muraoka, 2009). However, when SMR is deployed together with 2D coding and signal processing techniques, the system is referred as Two-Dimensional Magnetic Recording (TDMR) and can achieve the highest areal densities possible on the continuous media which is estimated at $10Tb/in^2$ (Hwang, Negi and Vijaya Kumar, 2010), (Wood et al., 2009).

TDMR used SMR technique in writing the data across multiple tracks and 2D readback signal processing to recover the information from multiple tracks simultaneously. It requires that, the readback signal be available from several tracks so that information from adjacent tracks can be exploited in making decision on the recorded data. With powerful 2D coding and detection algorithms, ITI which is normally avoided in conventional media now becomes an integral part of the detection process. The ITI is considered as an important signal whose information is utilised, rather than a noise that degrades system performance. The 2D readback signal which contains information from multiple tracks can be obtained either with an array head that reads many tracks at one go, or a single head with several passes run to build up the equivalent information required. Therefore, data from at least one or two adjacent tracks from both sides of a given sector is needed to account for the ITI in order to recover the data on the main track correctly. The illustration of the writing and reading processes for the TDMR system model is

shown in Figure 2.7. With the TDMR model set up of Figure 2.7, the aim of storing each user bit on very few grains, with the ultimate goal of storing one bit per grain seems achievable.

Although SMR and TDMR are interwoven together and at times used independently (in case of SMR) or used together (as TDMR), but the two are different. The key difference between the two technologies is that, SMR writes the entire 2D shingle block as one single entity, but when reading treated each track independently. While, TDMR employed the SMR writing process, and in addition, reads back the entire 2D shingle block as one unit. Therefore, the TDMR is more sophisticated in the readback process.

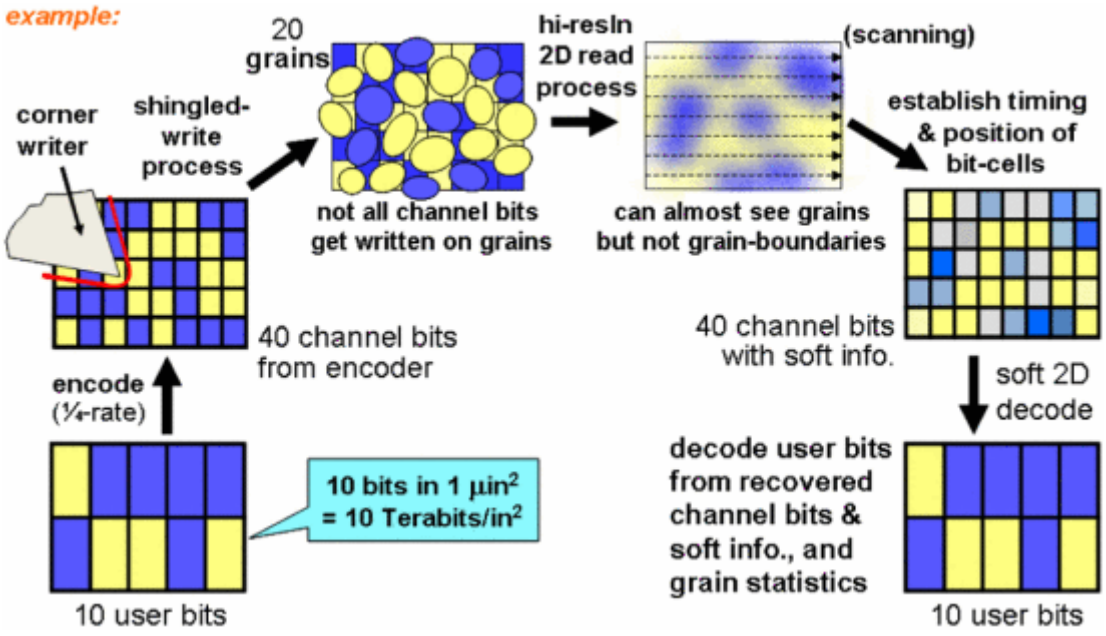


Figure: 2.7: TDMR system model (Wood et al, 2009).

However, there are some challenges surrounding the implementation of the TDMR concept. One is the additional system memory requirement needed for the SMR/TDMR system to match the performance of the current random-access HDDs as the entire 2D shingle block need to be stored before written on the disk. Also, there is the computational cost and complexity of implementing the full 2D readback signal processing algorithms.

2.4 Signal Processing for Magnetic Recording Channel

Digital magnetic recording is the process of storing and retrieving information/data on a magnetic media. One of the most important aspects in digital magnetic recording is the readback process whereby information stored on the media is recovered. However, the readback signal is always corrupted by channel distortions and other noise sources within the recording system. The main aim of any communications system is to reliably process and recover the information that was transmitted on the media with minimum probability of error. The same applies to digital magnetic recording systems. This is usually achieved with the application of signal processing techniques. A block diagram of the magnetic recording system is shown in Figure 2.8.

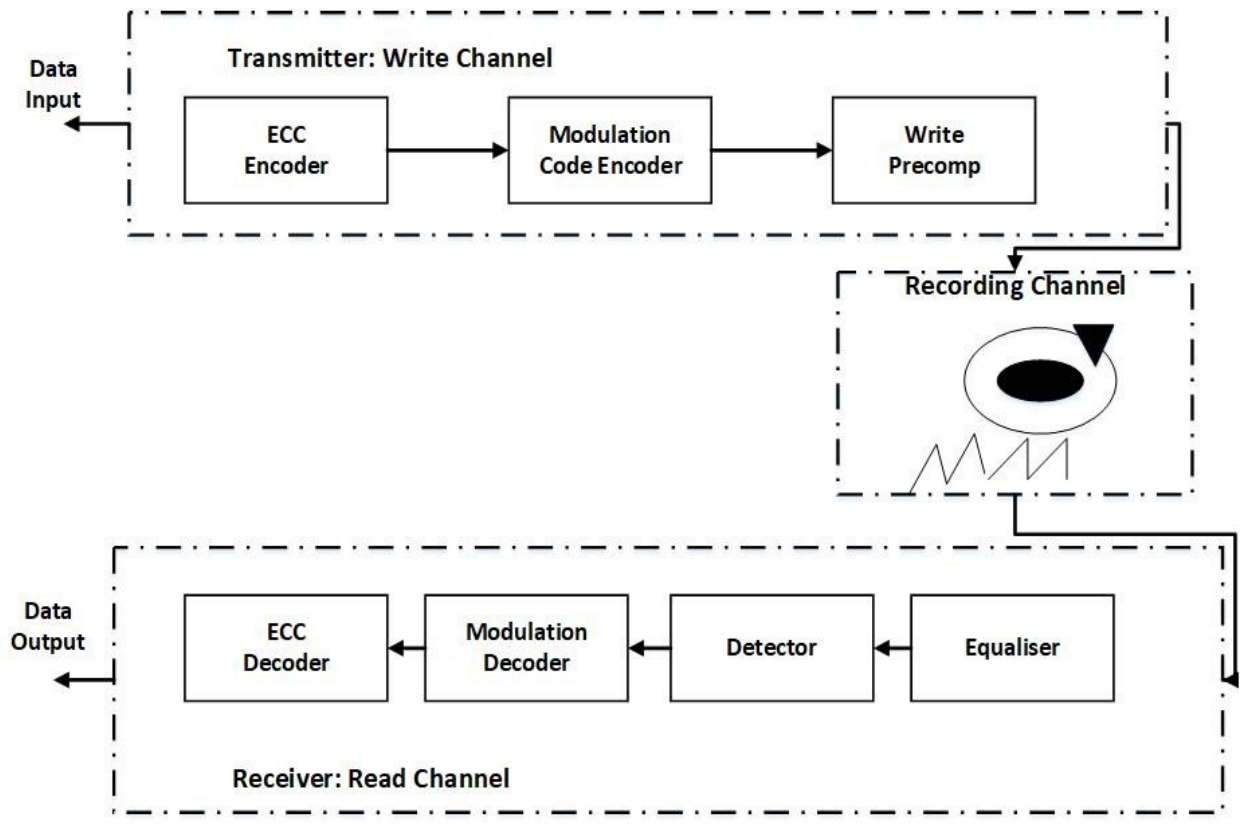


Figure 2.8: Block diagram of digital magnetic recording system.

At the transmitter side which in the case of magnetic recording the write channel, the user data bits are first encoded with an Error correction code (ECC) and then with a modulation code prior to recording them on the media. Write precompensation is used to adjust the transition positions in the write current in order to reduce the effect of non-linear transition shifts. The read channel is equivalent to the receiver side as of a communication system. Here the readback signal from the Read head is sampled before being equalised to match the desired channel response. The equalised signal is then passed through the detector for Maximum likelihood sequence detection (MLSD), or in some cases if soft output is needed; a Soft output Viterbi Algorithm (SOVA) detector or a Bahl Cocke Jelinek Raviv (BCJR) detector is used in place of the Viterbi Algorithm (VA) detector. After detection, modulation codes and ECC are then decoded to finally recover the user data bits.

In the next following sections, the readback signal processing and coding techniques for magnetic recording channels will be presented.

2.5 PRML System

Peak detection was primarily used as the detection method for magnetic recording system for decades until the 1990s when it was replaced by Partial response maximum likelihood (PRML) system. In peak detection, the isolated peak of each transition written on the media is used in detecting the data. This method was well suited for low density recording where transitions are isolated from each other. However, as the recording density increases, the transitions become much closer and overlap with each other. This results in adjacent symbols interfering with one another creating ISI. The peak detector can no longer be able to recover the signal reliably at such high recording density due to the ISI.

Consequently, an alternative detection strategy in the form of PRML system was introduced as a solution to high density recording for both longitudinal and perpendicular magnetic recording systems. The idea was introduced by kobayashi and Tang (Kobayashi and Tang, 1970), (Kobayashi, 1971), where it was showed that, correlative level coding (Lender, 1966) also known as partial response signalling can be applied in conjunction with maximum likelihood detection to improve detection performance. More also, it was proven in (Cideciyan et al., 1992) and (Dolivo, 1989) that the PRML system is well suited for digital magnetic recording application and can provide substantial increase in recording density compared to convention system with RLL coding and peak detection. This is why PRML was made the standard for most hard drive industries till date.

The PRML system consists of a partial response (PR) equaliser and a Viterbi detector that implement the maximum likelihood sequence detection. A controlled amount of ISI is allowed to pass to the detector via the PR equaliser, thereby shortening the span of the ISI spread. This reduces the complexity of the Viterbi detector as its complexity is exponentially dependent on the ISI span (Vasic and Kurtas, 2004). Also, another advantage of this method is that, noise enhancement due to full channel equalisation is avoided, thus improving the performance of the detector.

By controlling the amount of ISI into the detector, the signal spectrum is transformed into the desired channel response. This is achieved with a PR equaliser that satisfies the minimum mean square error (MMSE) criterion. The desired channel response is known as the target or target response. The equaliser controls the amount of spreading by converting the signal shape to that of the set target. The recorded sequences are then finally reconstructed from the desired equalised readback signal samples at the detector.

2.5.1 PR Equalisation

An equaliser is a digital filter that is configured and implemented at the receiver to compensate for transmitter and channel induced distortions. In digital magnetic recording, the aim of equalisation is to restore the signal spectrum to the desire channel response set by the target.

In the classical peak detection scheme, an equaliser is used to completely remove the ISI introduced into the system, which in the process amplifies and colourizes the noise from the readback signal due to spectral mismatch. This is because the equaliser modifies the correlation properties of the noise which in magnetic recording is uncorrelated, as a result colouring the noise (Shah et al., 2007). This becomes uncontrollable as the recording density increases. A solution to this problem in digital magnetic recording is employing PR equalisation.

PR equalisation unlike full channel equalisation allowed for a controlled amount of ISI into the detector in order to shape the signal spectrum closed to the desired channel response. The basic idea behind the PR equalisation is the fact that, the ISI is not completely suppressed but rather, a controlled amount is left for the sequence detector to handle. The controlled amount of the ISI is dictated by the PR target set which ultimately determined the match between the signal spectrum and the desired response. A closer match kept the noise enhancement level lower even when amplitude distortion is severe (Vasic and Kurtas, 2004).

For a magnetic recording channel to be transformed into a PR channel and subsequently PR equalisation applied, the channel must satisfy the following properties (Shah, 2008).

i. The shape of the readback signal from an isolated transition is exactly known and determined.

ii. The superposition of voltage pulses from adjacent transition is linear.

iii. The channel must operate in a bandwidth limited region.

The PR polynomial for a PRML channel is expressed generally as:

$$h(D) = h_0 + h_1 D + h_2 D^2 + ... + h_k D^k \tag{2.9}$$

where D is the delay operator, and $h_0, h_1, h_2 \ldots h_k$ are finite numbers of the non-zero samples of the equaliser.

Among the popular PR schemes developed earlier for magnetic recording is the class-4 partial response (PR4) given by:

$$h(D) = (1 - D)(1 + D) \tag{2.10}$$

This is well suited for channel bit densities with D≈2. A general class of partial response models for higher recording densities that are better match to the actual channel response was introduced by Thapar and Patel in (Thapar and Patel, 1987) as: $h_n(D) = (1 - D)(1 + D)^n$, $n \geq 1$.

For PR4 class $n=2$. Other variants of this class are referred to as the extended class-4 models denoted by E^{n-1}PR4. These schemes are well suited for bandpass magnetic recording channels that have nulls at Nyquist frequency and at DC (Cideciyan et al., 1992).

The pulse response of the PR4 channel is approximated as (Vasic and Kurtas, 2004), (Shah, 2008):

$$s(t) = \frac{\sin\left(\pi \frac{t}{T}\right)}{\pi \frac{t}{T}} + \frac{\sin\left(\pi \frac{t-T}{T}\right)}{\pi \frac{t-T}{T}} \tag{2.11}$$

The frequency response of the PR4 channel is given as (Shah, 2008):

$$D(w) = 2\sin(wT) \tag{2.12}$$

where, w is the frequency term and T is the sampling period.

However, for a lorentzian pulse in the frequency domain, the frequency spectrum is described as:

$$H(w) = \int_{-\infty}^{\infty} \frac{1}{1+\left(\frac{2t}{PW_{50}}\right)^2} e^{-jwt} dt \tag{2.13}$$

And the dibit response is expressed as (Shah, 2008):

$$D(w) = (1 - e^{(-jwT)}) \frac{PW_{50}}{2} \pi e^{-w\frac{PW_{50}}{2}} \tag{2.14}$$

where w is the frequency term, and T is the sampling period.

At lower recording densities, the readback signal from the magnetic recording channel contains high frequency components and the distance between transitions is much wider compared to the readback pulses. Therefore, little amount of equalisation is needed to match the signal spectrum to the desired channel response. However, as the recording densities increases, the spectral properties change rapidly towards the lower frequency region and therefore, more equalisation efforts are needed to restore the signal spectrum to the desired target.

To design an equaliser that will transform the shape of the signal spectrum to the desired target, the number of equaliser taps suited for the task need to be chosen. The equaliser taps give the total length of the impulse response of the digital filter and provides an insight into the frequency response of the filter. Usually, the number of taps of the equaliser is set to a length that will contain the most signal energy of the stored symbols.

For a 7-taps PR equaliser, the coefficients are given as:

$$c = [c_0 \quad c_1 \quad c_2 \quad c_3 \quad c_4 \quad c_5 \quad c_6] \tag{2.15}$$

The matrix for the 7-taps equaliser coefficient is formed from the channel response equation as:

$$H = \begin{bmatrix} h_n & h_{n+1} & h_{n+2} & h_{n+3} & h_{n+4} & h_{n+5} & h_{n+6} \\ h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} & h_{n+4} & h_{n+5} \\ h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} & h_{n+4} \\ h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} \\ h_{n-4} & h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} \\ h_{n-5} & h_{n-4} & h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} \\ h_{n-6} & h_{n-5} & h_{n-4} & h_{n-3} & h_{n-2} & h_{n-1} & h_n \end{bmatrix} \tag{2.16}$$

where h_n is the magnitude of the strongest (t=0) bit that is convolved with the surrounding bits (….h_{n-1}, h_{n+1},…) all derived from the channel transition response.

Finally, the equaliser coefficients are determined by evaluating the matrix equation

$$C = H^{-1}T \tag{2.17}$$

C gives the equaliser coefficients required to transform the signal shape to that of the chosen target response, while H is the matrix approximation of the channel response. T is a column matrix of length equal to the number of taps chosen. It is formed by padding zeros to the chosen PR target from left and right to form a column matrix.

2.5.2 PR Target

In the PRML system, the PR equaliser always tries to transform the signal spectrum to match the desired channel response. This desired response is known as the PR target. The more closely matched the readback signal is to the PR target, the better the performance of the system and

the further the recording density can be increased. Furthermore, the noise enhancement penalty in equalisation is drastically reduced by choosing a target that closely matches the readback signal spectrum (Thapar and Patel, 1987).

A number of different PR target responses have been introduced over the years. Among the earliest introduced are the PR target of the form $(1 - D)(1 + D)^n$ introduced in (Madden et al., 2004) referred as PR-4 target and its variants. The D is the delay operator signifying the delay of single bit period (D^k delay for k bit period), and n is non-negative integer. For PR-4 target, the value of n is equal to 1. The $(1 - D)$ term provides a dc-free response which matches the lower frequency response of the overall channel response, and $(1+ D)$ denotes the separation of transitions over neighbouring bits. This class of PR target are well suited for longitudinal magnetic recording (LMR) systems since the first term $(1 - D)$ gives a dc-free response that matches the low frequency response of the dc-free LMR signal (Madden et al., 2004).

For magnetic recording systems with channel bit densities ≤ 2, PR-4 target can be applied easily to shape the signal spectrum to the desired response. However, as recording densities increases, more equalisation is needed to transform the signal spectrum to the desired form. As such superior target need to be applied. EPR4 targets which are variants of the class-IV PR target can support high density recording with more than 33% increase in recording density compared to PR-4 target response (Vasic and Kurtas, 2004). However, the trellis structure for the VA detector of this target which is much complex makes its practical implementation very difficult. Therefore, a good target selection must take into account; trellis complexity, equalisation noise, and spectral matching. Table 2.1 gives an insight into the popular PR-4 target and its variants used for magnetic recording channels.

Table 2.1 Popular Class-IV PR targets for magnetic recording channels

Nomenclature	Polynomial	Isolated pulse samples	Impulse response samples
PR4	$(1-D)(1+D)$	...0 1 1 0….	…..0 1 0 -1 0….
EPR4	$(1-D)(1+D)^2$	…0 1 2 1 0….	….0 1 1 -1 -1 0….
E^2PR4	$(1-D)(1+D)^2$	…0 1 3 3 1 0….	*….0 1 2 0 -2 -1 0….*

However, the class-IV PR targets are not suitable for Perpendicular Magnetic Recording (PMR) channel due to the fact that the output signal of the PMR system has a dc component at non-zero (Madden et al., 2004). Ide in (Ide, 1996) proposed a target response that is suited for PMR channel. The target polynomial is expressed as:

$$H(D) = (1+D)^P \left(D^Q - 1\right)(1-D) \tag{2.18}$$

where the first term represents the response generated by a single pulse, while the second term represents the response due to superposition of pulses. *P* and *Q* indicate the number of samples corresponding to a single pulse and the extent of shifting at superposition. However, the choice of values of *P* and *Q* for different densities is non-trivial. Hence, various target responses are used by researchers. Table 2.2 shows some target responses for PMR channel class with different values for Q and P.

Table 2.2 PR target response for PMR channel class

	P	Q	Target response
PMR1	1	2	-1 0 2 0 -1
PMR2	1	3	-1 0 1 1 0 -1
PMR3	2	2	-1 -1 2 2 -1 -1
PMR4	2	3	-1 -1 1 2 1 -1 -1

Another PR target designed for PMR channel was the generalized partial response (GPR) targets proposed in (Madden et al., 2004) with their polynomial expressed as:

$$F(D) = \sum_{k=0}^{K-1} f_k D^k \tag{2.19}$$

where f_k positive, real-value coefficients, and K is the length of the target response matched to the channel. The $(1 - D)$ component that corresponds to a DC-Null is not needed in the GPR target unlike the other PR targets. This is because significant amount signal energy in PMR channel is concentrated in the low frequency component and filtering this energy to match a dc-null target polynomial result in eliminating the useful signal energy.

A new method of designing GPR targets for PRML channel that is based on maximizing the ratio of Minimum Square Euclidian distance of the PR target to the noise penalty introduced by the PR filter was proposed by (Shah, Ahmed and Kurihara, 2007). This technique can find targets with optimal performance without the need for noise prediction.

Recently a 2D GPR target for TDMR channel equalisation was proposed in (Zheng et al., 2014) and (Matcha and Srinivasa, 2015). The joint design of the 2D equaliser and the 2D GPR target in (Zheng et al., 2014) is solemnly aimed at minimizing the Mean Square Error (MSE) between the output of the 2D equaliser and that of the 2D target. However, in (Matcha and Srinivasa, 2015), an additional constraint with regard to separability of the target response was exploited in order to deploy low complexity detectors optimized for a separable 2D ISI channel (Wu et al., 2003), (Matcha and Srinivasa, 2015). This results in additional reduction in detector complexity and improved performance compared to a non-separable target of the same size.

2.5.3 2D PR Target/Equalisation

In channels with significant 2D interference such as the SMR/TDMR channel, where a 2D detector is used for detection, the equaliser and the target response polynomial also need to be in 2D for optimal performance. Figure 2.9 shows the schematic diagram for the 2D equalisation and 2D detection process of a 2D channel, where *i* and *j* represent the bit position in the along-track and across-track direction respectively.

The 2D polynomial functions for the equaliser and target response can be expressed as equation 2.20 and equation 2.21 respectively.

$$F(D_1, D_2) = \sum_{k=-K}^{K} \sum_{l=-L}^{L} f_{k,l} D_1^k D_2^l \tag{2.20}$$

$$G(D_1, D_2) = \sum_{m=-M}^{M} \sum_{p=-P}^{P} g_{m,p} D_1^m D_2^p \tag{2.21}$$

Where D_1 and D_2 are shift operators denoting unit shifts in the along-track and across-tracks directions, respectively.

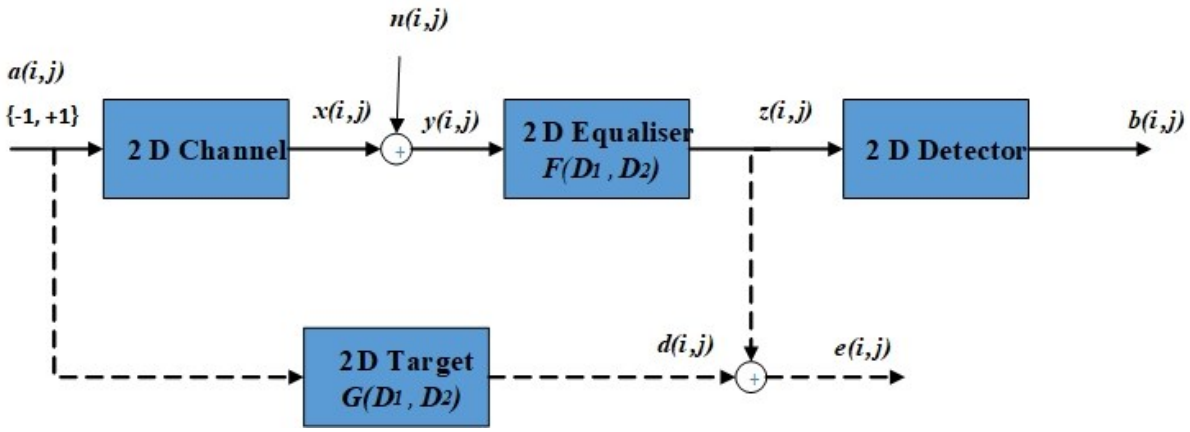


Figure 2.9: Schematic diagram of Two-dimensional equation and detection process

The equaliser output $z(i,j)$ is the 2D convolution of equaliser function and the channel output $y(i,j)$. Similarly, the target output (desired output) $d(i,j)$ is obtained by the convolution of the target function and the 2D channel input $a(i,j) \in \{-1,+1\}$.

The output *y(i, j)* from the 2D channel is expressed as given by equation 2.22.

$$y_{i,j} = x_{i,j} + n_{i,j} \tag{2.22}$$

Where $x_{i,j}$ is determined by the convolution of the 2D input data $a_{i,j}$ with the 2D channel transition response $h_{k,l}$ and is given by equation 2.23.

$$x_{i,j} = \sum_{k,l} h_{k,l} a_{i-k,j-l} \tag{2.23}$$

Now, for simplicity, let the 2D channel input signal at time "*k*" be expressed as a column vector, and represented by a_k. Let the 2D signal from the channel output at time "*k*" be expressed as a column vector and represented by y_k. Also, given the 2D equaliser coefficient matrix and the 2D target coefficient matrix expressed as column vectors, and represented by f^T and g^T respectively, where exponent of *T* denotes transpose. Then, the error signal (e_k) is the difference between the equaliser output signal and the target output signal expressed as shown in equation 2.24.

$$e_k = f^T y_k - g^T a_k \tag{2.24}$$

The equaliser and the equalisation target are designed based on the MSE criterion presented in (Zheng et al., 2014). This is achieved by minimizing the MSE between the signal at the output of the equaliser and target output. Accordingly, the MSE can be obtained from equation 2.24 as,

$$E(e_k^2) = f^T R f - 2 f^T Q g + g^T A g \tag{2.25}$$

where $R = E\{y_k y_k^T\}$ is the autocorrelation matrix of the 2D channel output, $Q = E\{y_k a_k^T\}$ is the cross-correlation matrix of the 2D channel output and input, and $A = E\{a_k a_k^T\}$ is the autocorrelation matrix of the 2D channel input. *E* denotes the expectation.

A trivial solution of *f*=*g*=0 may exist when minimizing the MSE in equation 2.25. To avoid that, a constraint is imposed on *g* so that certain entries of *g* have some specific values. In other implementations, the constraint on *g* is chosen to force the adjacent tracks contributions to zero so as to circumvent the 2D detector (Wang, Frohman and Victoria, 2014), (Nabavi and Kumar, 2007). The constraint on *g* is expressed as shown in equation 2.26.

$$E^T g = c \tag{2.26}$$

where E^T is a matrix whose number of rows is determined by the number of entries in *g* that does not need to be optimised. While *c* is the column vector obtained from the application of the constraint. An example from (Nabavi and Kumar, 2007) assumed a 3× 3 target coefficient vector *g* that is constrained as

$$g = \begin{bmatrix} 0 & 0 & 0 & g_{0,-1} & 1 & g_{0,1} & 0 & 0 & 0 \end{bmatrix}^T$$

From the above constraint on *g*, the constraint matrix E^T is obtained as

$$E^T = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

And the column vector *c* is given as

$$c = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T$$

With the constraint in place, a constrained minimization of the MSE is achieved by minimizing the Lagrange function of equation 2.27 given by,

$$J = f^T R f - 2 f^T Q g + g^T A g - 2\lambda^T (E^T g - c) \tag{2.27}$$

where λ is a column vector containing the Lagrange multipliers.

Further calculations produced the optimised target and the equaliser coefficients vectors as follows:

$$\lambda = \left(E^T \left(A - Q^T R^{-1} Q \right)^{-1} E \right)^{-1} c \tag{2.28}$$

$$g = \left(A - Q^T R^{-1} Q \right)^{-1} E \lambda \tag{2.29}$$

$$f = R^{-1} T g \tag{2.30}$$

2.6 Detection Techniques

In the PRML system, after transforming the readback signal to the desired shape by using the PR equaliser and other filtering techniques, the equalised signal is passed through the detector to get the stored data out of the equalised signal. The detector is utilised to provide an estimate of the binary information sequence stored on the disk. Maximum Likelihood (ML) detection is usually used in recording channels and other digital systems to detect the data sequence. Two different types of ML detection strategy that are trellis-based are discussed below:

1. Maximum Likelihood Sequence Detection (MLSD).

2. Maximum A-posteriori Probability (MAP) Detection.

2.6.1 Maximum Likelihood Sequence Detection

The optimum detector for signals with ISI in AWGN channel as proposed by Forney (Forney, 1972) consists of a whitened matched filter, a sampler and an MLSD detector implemented using the Viterbi algorithm (Viterbi, 1967). The noise sequences are assumed to be additive white Gaussian with zero mean and variance $\sigma_n^2 = N_0 x_0 / 2$. Therefore, the output signal sequence from the sampler is expressed as (Vasic and Kurtas, 2004):

$$y_n = a_n x_0 + \sum_{\substack{k=-\infty \\ k \neq n}}^{\infty} a_k x_{n-k} + v_n \tag{2.31}$$

where the first term on the right-hand side of the equation is the desired term and second term represents the interference term. As can be seen from equation 2.31 the ISI spread across infinite number of bits which affects the desired bits. For lower recording densities, the ISI spread affects only few bits but at high density can extents to several bits. A preferred solution is to replace the matched filter with a PR equaliser so as to model the magnetic recording channel as discrete-time FIR system. The output from the sampler is then passed to the MLSD detector to obtain an estimate of the binary information sequence.

The MLSD detector tries to minimize the probability of error events by selecting the sequences that are at minimum Euclidean distance to each other. This maximizes the probability of selecting the set of sequences that are very close to the correct sequence of symbols. The output from the MLSD detector is a hard decision in the form of 0's and 1's. However, it conveys no information on the reliability of the decision taken. MLSD can be implemented in magnetic recording channels using the Viterbi algorithm (VA) designed for decoding of convolutional codes with some modification. The VA was first proposed by Forney as a means for decoding convolution codes (Forney, 1972).

The Viterbi detector is a maximum likelihood detector that determines the most likely sequence of binary symbols that are received. The VA has a recursive structure that does not grow with the length of the message but has a complexity proportional to m^L, where m is the size of the input alphabets, and L the length of the impulse response. The VA tries to find the sequence of symbols in a given trellis that is a closest distance to the received sequence of noisy symbols. When Euclidean distance is used as the distance measure, then the VA is the optimum MSLD method in AWGN channel (Hui and Moura, 1995).

The Viterbi detector consists of three functional units namely: Branch Metric Unit (BMU), Add Compare and Select Unit (ACSU) and the Trace-Back Unit (TBU). Figure 2.10 shows the schematic arrangement for the basic functional unit of the VA.

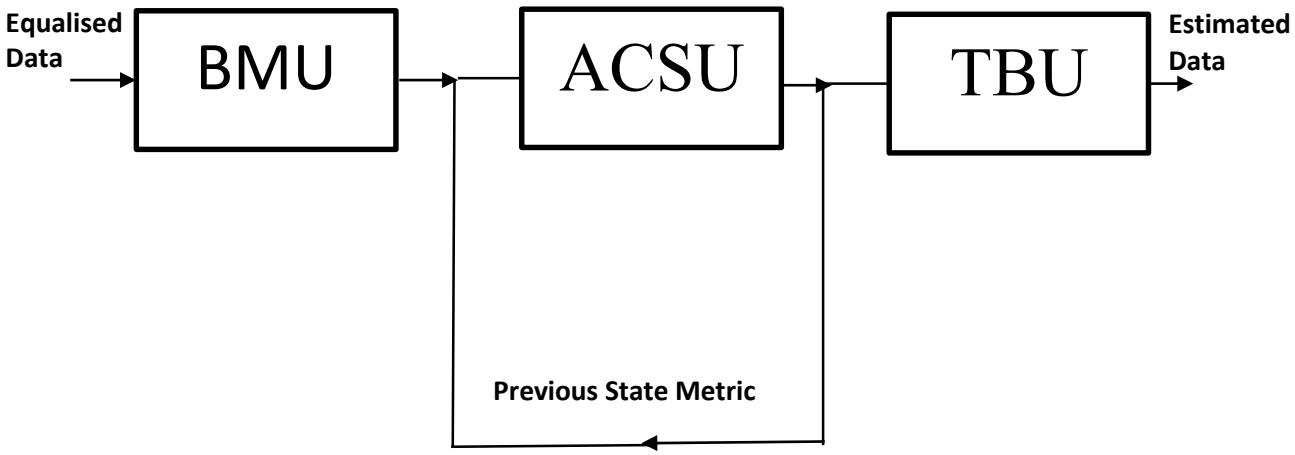


Figure 2.10: Functional units of the Viterbi algorithm (VA).

BMU is the cost of traversing along a specific branch, and in AWGN it is evaluated as the square distance between the received noisy sample and ideal noiseless output sample of the transition (equalisation target value). It determines how far the received sequence is from all the possible received sequences. In magnetic recording channels with ISI and ITI, Euclidean

distance is used as the branch metric and can be determined using the reduced Gaussian equation as:

$$BMU_{t,n} = e^{-(y_t - s_n)^2} \tag{2.32}$$

where y_t is the received signal at time "t" and s_n is the ideal noiseless signal received at time t. Equation 2.32 can be simplified further by taking logarithm of the equation such that in determining the state metric, multiplication operation reduce to addition. Therefore, the BMU is now calculated as:

$$BMU_{t,n} = -(y_t - s_n)^2 \tag{2.33}$$

The **ACSU** has all the records of the previous state metrics with their corresponding branch metric. It calculates and add the branch metrics of all transitions to their corresponding state metrics, and then compare them to select the minimum among them as the new set of state metric for the next transitions. The **ACSU** operation can be explained best with the aid of a trellis as shown in Figure 2.11.

At time t_3 for example, the branch metric for transiting from 00 to 00 is calculated and the result is added to the previous state metric. Similarly, the branch metric for 00 to 01 is calculated and added to previous state metric. The two results are compared and the best which is the minimum is selected as the next state metric. A history is kept to indicate the state in which the metric is selected and the symbol responsible for such transition is known.

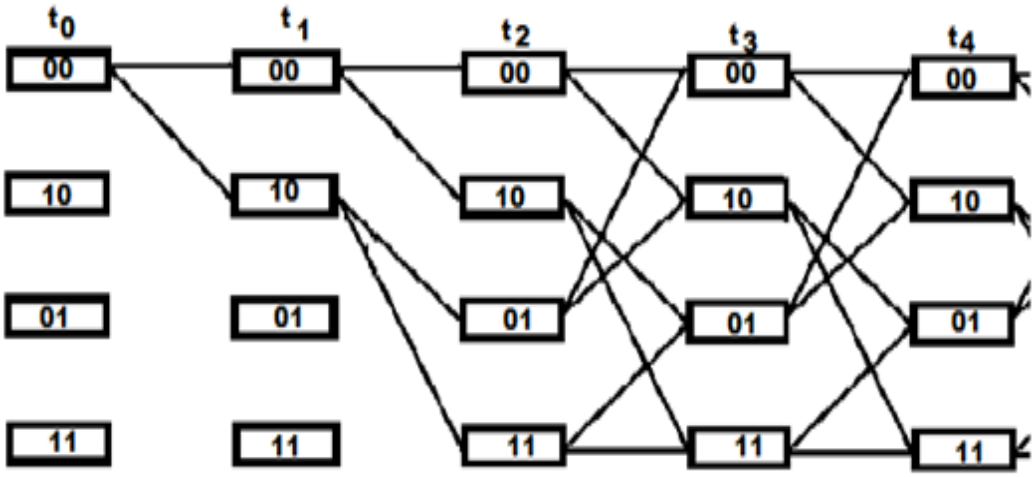


Figure 2.11: Four state trellis of VA with m=2 and k=1, starting from 00 State.

The trace back process starts the end of the trellis when all the states metrics have been determined. The **TBU** selects the state with the lowest state metric as the starting point for the trace back. The history kept for that state is used to determine the preceding state and the symbol responsible for the transition is save as the last output. This continued until the beginning of the information chosen is reached. For any given number of symbols that has k bits, the number of transitions is given by:

$$n = 2^k \tag{2.34}$$

And for a Viterbi detector with a register containing m number of bits and k incoming symbols, the number of states is determined as:

$$St = 2^{mk} \tag{2.35}$$

The trellis in Figure 2.11 has $m=2$ and $k=1$, therefore the number of states was four states with two incoming and outgoing branches per states.

2.6.2 Maximum A-posteriori Probability Detection

The MAP detector is an optimal detector that determines the most probable bits of symbols that are received. Unlike the MLSD detector, the MAP detector is a bit-wise detector that works on bit by bit and does not takes into account a sequence of certain length, and hence produce a better Bit Error Rate (BER) compared to the MLSD detector. It provides soft information outputs and also information about the reliability of each bit (decision taken).

MAP detection is implemented in digital magnetic recording using the Bahl Cocke Jelinek Raviv (BCJR) algorithm proposed by (Bahl et al., 1974). The BCJR detection algorithm tries to minimize the bit error probability of the symbol that is received. It is a trellis-based detection algorithm optimized for channels with additive Gaussian noise. The aim of the BCJR decoder/detector is to determine the A-posteriori probability (APP) of the decoded/detected bit either 1 or 0 using the A-priori probability (AP) and the trellis structure. The AP probabilities are the probabilities of bits that are received (either 1 or 0) on the channel before decoding take place. These probabilities are computed using the probability density function of the received data bits. For a channel with AWGN, if x_k is the transmitted (saved) bit or symbol, and y_n is the received (read) bit or symbol, then the probability of receiving y_n given that x_k was transmitted through the channel is given by:

$$p\left(y_n / x_k\right) = \frac{\exp\left(-\frac{(x_k - y_n)^2}{2\sigma^2}\right)}{\sqrt{2\pi\sigma^2}} \tag{2.36}$$

where σ is the standard deviation of the channel noise. For any channel at a given time "*t*", σ is normally considered to be the same or approximately equal for all possible sampled bits or symbols. Therefore, equation 2.36 can be simplified further by eliminating σ and all other constants from the calculation. Equation 2.24 is now reduced to:

$$p\left(y_n/x_k\right)=\exp(-\frac{(x_k-y_n)^2}{2\sigma^2}) \tag{2.37}$$

In the BCJR algorithm, the APP which determines the most probable symbol or bit is computed using three key probabilities obtained using the trellis structure. These are; the forward recursive probability known as Alpha (α), the backward recursive probability Beta (β), and the transition probabilities Gamma (γ). The values of α are computed from the beginning of the trellis to the tail end, while β values are computed in the reversed other (i.e from the trellis tail end to the beginning start). In determining α, the α for all states is initialised with the initial condition that, for the first state having a probability of 1 and the rest having probabilities of 0. This is done when the sequence is needed to start from the first state. However, the β for all states is initialised with equal probability with a unit sum when the sequence is to end at any given state.

When a bit or symbol y_n is received at a given time "t", the transition probabilities (γ)s of all branches for each state, are computed according to equation 2.37 and the values are saved. Then, the forward recursive probability (α) for the next coming symbol is calculate using the initial (α) for the previous state and the saved transition probabilities as in equation 2.38.

$$\alpha_{t+1}=\sum_{s_{k-1}^{n}}\alpha_t\gamma^{s_k,s_{k+1}} \tag{2.38}$$

where s_k represents the current state at time "t", s_{k+1} represents the next state at time "$t+1$" and s_{k-1}^{n} indicates a summation over all the possible states that leads to the next state where α is determined. This process is repeated in a similar manner for all incoming symbol until the last symbol or bit in the selected block is received.

The backward recursive probabilities (β)s are then calculated in similar manner starting from the last symbol or bit backward up to the first received symbol toward the start of the trellis. The (β) for each symbol or bit at time "*t*" is calculated using equation 2.39.

$$\beta_{t-1} = \sum_{s_{k-1}^{n}} \beta_t \gamma^{s_k, s_{k+1}} \tag{2.39}$$

Note that both the forward recursive probability (α) and the backward recursive probability (β) required the transition probability (γ) for their computation. Therefore, the transition probability (γ) is calculated first. When all the values of α and β for a given symbol or bit is determined, the APP for that symbol or bit is evaluated using the expression in equation 2.40.

$$APP(x) = \sum_{s_x} \alpha_{s_k} \gamma^{s_k, s_{k+1}} \beta_{s_{k+1}} \tag{2.40}$$

where s_x denotes summation over all states that produced the transition when bit "*x*" is received. The probability of 1 and 0 are calculated using the equation 2.40 for a binary system. After the final computation, the bit with the largest probability is selected as the detected bit.

2.6.3 Full 2D Detection

For multilevel systems where 2D interference is prominent such as optical communications system, wireless channels involving ISI and Inter-Channel Interference, and TDMR channel with ISI and ITI. Full 2D detection is required to reliably recover the data from the channel. However, the 2D ML detector for these channels is very complex and its complexity is exponential to the number of information bits involved. Therefore, it was practically impossible to implement (NP hard) (Ordentlich and Roth, 2006) over the years and did not receive much attention until recently (Losuwan et al., 2012), (Zheng et al., 2014), (Zheng and Zhang, 2015), (Abdulrazaq, Ahmed and Davey, 2015a).

In the TDMR channel, multi-track joint detection is carried out by using a full 2D detector that detects data simultaneously from multiple tracks. The data from the multiple tracks are equalised with a 2D GPR target equalisers before being passed to the 2D detector.

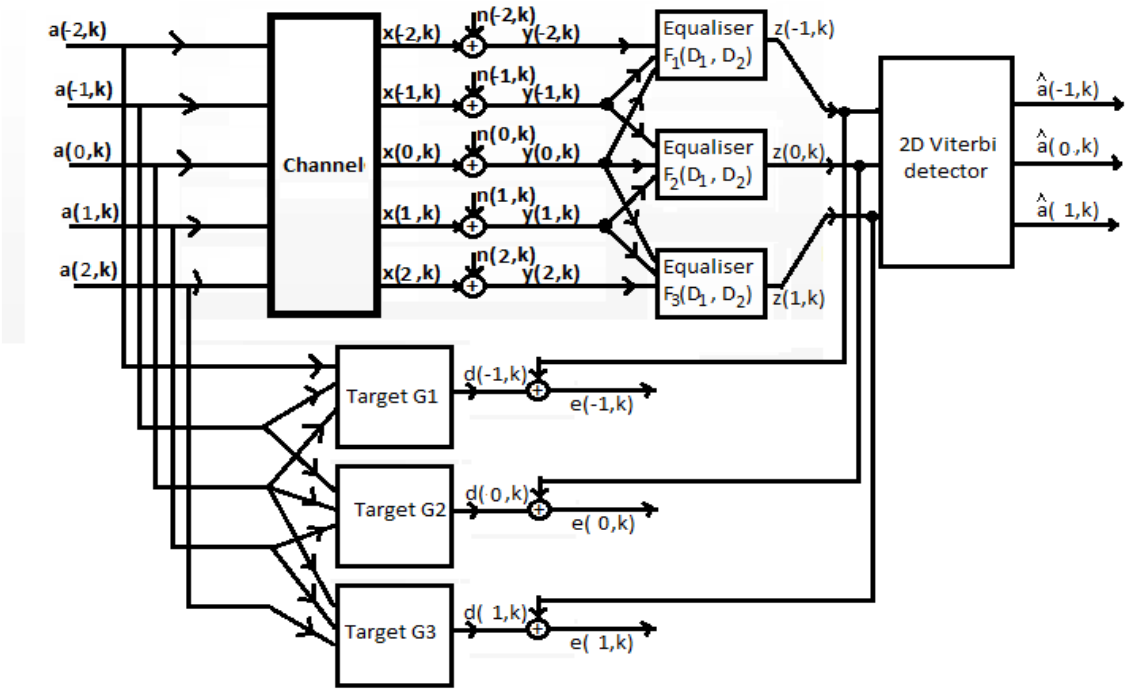


Figure 2.12: Joint-track detection of three data tracks, using readback data from five consecutive tracks read simultaneously. a=binary data, x=saved data, y=noisy data, z=equalised data, e=error, â= detected data and d= dibit (Zheng et al., 2014),

In (Zheng et al., 2014), 2D GPR target equaliser and 2D Viterbi detector are employed in extracting information on the main tracks from a multi-track TDMR channel with SMR media. It was suggested that for data to be recovered reliably from the three main tracks simultaneously, data from five tracks (including tracks adjacent to the main tracks) need to be read and utilised to get the equalised data for the three main tracks. The data for the three main tracks are simultaneously detected with a full 2D Viterbi detector or its soft output version

(SOVA). The depiction of the process involved in detecting three tracks simultaneously using data from five tracks is shown in Figure 2.12.

Compared to the use of 1D detector, the 2D detector provides a considerable performance gain at moderate recording density. But as the recording density increases, the gain in the performance gradually diminished. This was also reported by (Losuwan et al., 2012). In (Zheng and Zhang, 2015) a low-complexity 2D detector was proposed for multi-track detection of SMR channel. The 2D detector achieved a considerable gain over 1D detector for a relatively low data density system. Thus, this gives room for further improvement of the 2D detectors for use in TDMR systems.

2.7 Error Correction Codes

An Error Correction Code (ECC) is used in magnetic recording channels to detect, identify and possibly correct errors that may occur during writing and reading of data on the disk. The ECC adds some information (redundant bits) to the user data before it is transmitted or recorded on the magnetic media. At the receiving end, the receiver exploits the redundant bits and their relationship with the user data in correcting errors that may occur during transmission or storage. The redundant bits are sometimes referred to as parity bits in binary data systems. These parity bits can be formed by either a simple repetition of the original user data or by a result of a more complex function involving the user data.

A single parity code adds a single bit to the user data in order make the number of 1s in the codeword even (Even parity) or made it odd (Odd parity). A more complex code requires the addition of several parity bits to a block or group of data to form a codeword.

ECC are classified according to the way in which the parity bits are added. These include block codes and convolutional codes.

2.7.1 Block Codes

The encoder for block codes encodes a fixed number of information bits or symbols into a vector of length n by dividing the information bits or symbols into blocks of k bits or symbols that are independent of each other. Information bits or symbols are processed block by block, and each codeword is independent from the other, so that the whole process becomes a memoryless operation. Suppose $u = (u_1, u_2 \ldots u_k)$ represent a message block of bits, then there are 2^k different possible messages. At the encoder, each of the u block of bits is transformed independently into $v = (v_1, v_2 \ldots v_n)$ codeword such that, for every 2^k block messages, there correspond a 2^k codewords at the output of the encoder. Therefore, the set of 2^k codewords of length n is called the (n, k) code and the code rate R is the ratio $R = k/n$; which is the number of information bits entering an encoder per transmitted symbols (Lin and Costello, 1983). Block codes are widely used in ECC because of their ease of implementation. Their encoder is memoryless and requires only a combinational logic for implementation. There are wide varieties of blocks codes with different block length sizes. They include block codes of block length containing few bits like Hamming (7, 4) code and block codes of block length containing thousand bits like the Low-density Parity Check (LDPC) code.

2.7.2 Convolutional Codes

Convolutional codes offer an alternative approach to error control coding that is substantially different to block codes. The encoder for convolutional coding transformed the entire message sequence into a single codeword, unlike in block coding where the original message sequence is segmented into different blocks of codewords. Also, the encoder for convolutional codes has memory and the output of the encoder depends not only on the current input, but also on the previous input symbol. The power of convolutional codes lies on the nature of their design and

evaluation. They are primarily based on constructional techniques which make their implementation very easy using finite shift registers, compared to block codes that are based on algebraic/combinatorial techniques.

Convolutional codes were first introduced by Elias in the1950s as an alternative to block codes. Subsequently thereafter, sequential decoding was proposed by Wozencraft as a decoding technique for convolution codes. In 1967, Viterbi (Viterbi, 1967) proposed an algorithm for ML decoding of convolutional codes with small memory order. The Viterbi algorithm simplifies the decoding of convolutional codes, and that facilitate their deployment in deep-space and satellite communication in the early 1970s.

Three key parameters (*n, k, m*) describes a convolutional code. *n* is the number of bits outputted at the encoder's output at a given time, *k* is the number of bits input to the encoder at a given time, while *m* is the number of previous input blocks used to generate each output which represents the encoder memory. The performance of a convolutional code is determined by the constraint length (K) and the code rate (R_c). K is the maximum number of bits in a single output stream that are affected by the previous input bit. In most realizations, $K = m + 1$. The code rate is given as $R_c = k/n$. Longer constraint length improves decoding reliability, but also, results in complex decoder implementation. However, higher code rates provide better coding gain but with reduced bandwidth efficiency. The encoder is implemented using a linear finite state shift register to produce a finite state machine. Convolution codes are described using either a tree diagram, state diagram, or trellis diagram.

2.7.3 Concatenated Codes

In error correction coding, codes with very long block lengths are often required in order to achieve optimal performance. However, encoding and decoding of such codes becomes very

complex as the size of block lengths increases. Therefore, it is very important to devise a means of generating large block length codes that can achieve good performance with less complexity.

Concatenation of two or more simpler codes is used to produce an overall powerful code with better performance, and at the same time very easy to decode. This concept was first introduced by (Forney, 1967), where two simple codes (an outer non-binary code and an inner binary code) were concatenated serially to produce a more powerful overall code. Codes can be concatenated either in series, parallel, or combination of both (Hybrid concatenation).

Very often, an interleaver is normally used in concatenated coding to separate the inner code from the outer code. For example, in turbo coding, the two concatenated recursive systematic convolutional codes that are in parallel are separated via an interleaver. The interleaver is effective in re-arranging the order of the transmitted bits or symbols so as to randomise the burst of errors that may occur after decoding the first inner code.

2.8 Interleaver

There are two types of error that occur in communication or storage systems. One is the random error in which the error locations are independent of each other. This kind of error can easily be corrected using error correction coding. The other type of error is the burst error, which occur due to local concentration of many errors. Burst errors spread across several bits streams, with the error in one location having contiguous effect on other bits. Hence, the error locations are dependent of each other.

An interleaver is normally used in conjunction with error correction coding to counteract the effect of burst error. The aim of interleaving is to disperse the sequence of bits in a bit-stream according to some permutations so that error bursts are distributed evenly across different codewords (Andrews, Heegard and Kozen, 1997). This minimized the effect of burst errors

introduced into the transmission system and improves the error performance of the system. However, for every interleaver there is a corresponding de-interleaver which acts to restore the original order of the symbols. Interleavers are basically classified into block interleavers and convolutional interleavers. However, only interleavers of block type will be discussed in this thesis.

2.8.1 Matrix/Square Interleaver

The matrix interleaver or square interleaver is a special type of block interleaver that performs very well with small number of block length (Shukla, Gupta, and Bhatia, 2011). The data bits are stored in a matrix array form where they are written in along rows and read out along columns (Tullberg and Siegel, 2000). The parity bits are computed and added column wise according to the parity equation where the data bit represents bits elements along each column space. The column space denoted as *n* represents the depth of the interleaver whereas the row space denoted as *m* represents the span of the interleaver. The interleaver is completely defined by *n* and *m* and is referred to as (*n, m*) matrix interleaver (Chaturvedi, Gupta and Dehradun, 2012).

2.8.2 Dithered Relative Prime Interleaver

A random interleaver is a block based interleaver that tries to randomise the order of the bit positions by generating a pseudo-random number for the addresses to which the bits are taken. A version of this type interleaver is the Dithered Relative Prime (DRP) that performs very well with turbo codes. It is a low-memory, high-performance interleaver that breaks the whole interleaving process into 3 distinct stages. The first stage involves breaking down the whole data into smaller blocks of equal length with each block permuted locally. This is termed the read dither. Then, the whole resulting data is permuted globally using a pseudo-random relative

prime generator. Finally, the resulting data is again broken into smaller blocks and each block is permuted locally. This is called the write dither (Crozier and Guinand, 2001).

2.9 Review of Similar Work

This section presents the review of works done in the areas of equalisation, detection, error correction coding and decoding techniques for magnetic recording channels. It is worth mentioning that this thesis work will be carried out using conventional PMR media based on the jitter noise model, with subsequent modifications to be done on the media, leading to SMR/TDMR media channel model. Therefore, it is imperative that literatures based on conventional PMR media and SMR/TDMR media channel are discussed in this section.

The review includes introductory on the earlier equalisation, detection and decoding techniques developed, their subsequent modification towards performance improvement and complexity reduction, and also recent development in the implementation of these techniques. Special attention is paid on literature that focused on detection and decoding techniques that are pertinent toward improving the BER performance of both 1D and 2D magnetic recording channel with reduced complexity. The review will focus on the objectives behind the development or modifications to these techniques in some of the works in literature, the changes made on the existing techniques and the improvement in terms of performance, complexity, coding gain and implementation cost.

The optimum 1D detection based on MAP algorithm gives an excellent performance in detection compared to other equalisation and detection techniques in the 1D space. However, although implementable as widely used in today's HDD, it complexity is proportional to the high PR polynomial order. Coding and detection techniques for high density recording have been proposed over the years to support the areal density growth of the HDD industry.

Elidrissi and Mathew, 2004 proposed a parity-check code based on parity check coding combined with distance-enhancing code for improving the performance of a PMR channel. The distance-enhancing code is designed to eliminate the most dominant error event from the output of the Viterbi detector, while the remaining dominant error events are handled by parity check coding. The overall code design entails combining RLL code and parity constraints through concatenating certain number of maximum transition run (MTR) codewords with some parity bits appended. The parity-based postprocessor employed at the output of the Viterbi detector detects the error events, identify type and location of the error events, and finally correct the error events that might have occur. Their approach reduces certain complexity issues at the postprocessor stage and also improves the BER performance compared to other postprocessor schemes such as in (Conway, 1998) and (Cideciyan et al., 2001). A gain of about 4.2 dB was recorded with the coded scheme against an uncoded PR channel with AWGN.

In order to extend the parity-based coding and postprocessor technique to high density multi-track magnetic recording channel with severe ISI and ITI (TDMR channel), (Vasic and Venkateswaran, 2004) developed a low complexity soft-error event decoding algorithm for reducing the effect of ISI and ITI in multi-track magnetic recording channel. The approach considered the use of a joint PR equaliser that equalises the readback signal from multiple tracks to a joint PR target. An adaptive equaliser was then employed to cancel out ITI from adjacent tracks which was considered as an independent data sequence coming from the adjacent tracks. A bank of single track Viterbi detector was used for detection instead of a multi-track Viterbi detector to reduce complexity. Finally, multi-track parity-based postprocessor was designed to detect and correct the most dominant error events due to the Viterbi detectors and the joint PR target.

However, while equalisation, coding and detection using constrained parity check coding and parity based post processing have been shown to improve system performance (Conway, 1998), (Cideciyan et al., 2001), (Elidrissi and Mathew, 2004), (Vasic and Venkateswaran, 2004), the loss in code rate due to the constraint coding, and the additional complexity burden, together with decoding delay at the postprocessor stage are the drawbacks to these approaches.

An alternative to constraint coding and parity-based post processing for high areal density recording is the use of iterative decoding together with 2D ISI detection. This approach enabled the detection and decoding of symbols in a turbo fashion. (Wu et al., 2003) considered an iterative detection and decoding for separable 2D ISI system. The complex 2D detection process is treated as concatenation of two separate 1D channel which can be carried out separately to reduce the complexity of 2D ISI equalisation. This is possible through the transformation of the 2D ISI channel matrix into a product of two separate vectors. Then, iterative decoding is facilitated by connecting the output from the 1D MAP detector to a low density parity check (LDPC) decoder for soft information exchange. Two different schemes were proposed for the separable 2D ISI detection. The first scheme applies a linear equaliser in one direction and then performed MAP detection in the other direction, while the other scheme utilises the MAP detector for both directions. However, even though decomposing the 2D ISI channel matrix into a product of separate two ISI vector helps in reducing the complexity of the 2D ISI detection process, in most practical application the process is not really feasible.

Marrow and Wolf, 2003 developed an iterative row column soft decision feedback algorithm (IRCSDFA) for 2D ISI channels, where soft information exchange between MAP detectors operating on multiple rows and multiple columns is utilized to improve detection performance. Similarly, (Cheng, Belzer and Sivakumar, 2007) also proposed an IRCSDFA algorithm that is similar to that of (Marrow and Wolf, 2003) with some modifications to enhance the algorithm

performance. The first modification done was to take decision after each and every row at given time interval and to use soft decision feedback, rather than after two rows at a time and use feed forward (Marrow and Wolf, 2003), (Cheng, Belzer and Sivakumar, 2007). The other modification is to assign weights to the extrinsic information passed between the SISO decoder and increment the weights with the number of iterations carried out. Even though there was an improvement in performance due the modification on the algorithm, the algorithm is susceptible to feedback errors and takes more time to converge.

Chen and Srinivasa, 2012 also developed a 2D iterative detection algorithm that operates by exchanging extrinsic information between multiple row/column detectors in a turbo fashion. The algorithm considers using the feedback information from neighbouring bit cells outside the local 2D ISI span. In (Chen and Srinivasa, 2013), 1D soft linear MMSE equalisation was extended to a 2D setting by concatenating the equaliser with the 2D MAP detector to produce an iterative multi row/column joint equalisation detection scheme for handling 2D interferences. The self-iterating 2D equaliser and the multi-row/column iterating detector are combined together to operate in a turbo fashion. A performance close to that of optimal 2D MAP detection was reported with some increasing level of complexity.

Low complexity IRCSDFA with Gaussian approximation (GA) was proposed in (Zheng et al., 2013) in order to reduce the complexity of the IRCSDFA algorithm. GA was employed to reduce the complexity of the IRCSDFA detector by decreasing the number of branches in the ISI trellis section of the individual component detectors. BCJR algorithm was then applied over the simplified ISI trellis in conjunction with LDPC decoding. A loss of about 0.3 to 0.35 in dB was recorded compared to the IRCSDFA without GA algorithm. Consequently, (Guan et al., 2014) improve the IRCSDFA-GA detection algorithm by redesigning the LDPC code to remedy the performance loss incurred due to the GA approximation.

While detector employing iterative decoding and detection paradigm tends to yield good result in channels with both 1D and 2D interference, the algorithm is suboptimal considering the effect of short cycles present in the decoder's factor graph, and also due iterations processes between the detector and the decoder and within the decoder itself (Shafiee, Sann and Liang, 2015). Also, the fact that the performance of the iterative process been highly dependent upon the number of iterations carried out makes the decoder suboptimal.

The use of multi-Read head array for multi-track magnetic recording first proposed by (Barbosa, 1990) has provided an alternative solution towards achieving high areal density recording. Using the concept of multi-head multi-track recording, Yao et al. 2015 developed a 2D equaliser for array-reader two-track model that jointly process array readback signal for two tracks. The detector is designed to jointly process two input streams on a symbol basis. The advantage of using the array-read headers is that they provide diversity gain that deals with the noise as similar to MIMO systems in communications systems. It also facilitates ITI handling and multi-track detection (Yao et al., 2015). A considerable gain was recorded with this scheme compared to single-reader single-track detection.

However, even though the 2D signal processing techniques discussed so far above in this section do provide some trade-off between detection performance and computational complexity, they do not fully utilize the 2D interference available at the channel to give improved performance. Therefore, there is the need to consider the design of optimal 2D detectors that can fully perform 2D equalisation and detection across multiple tracks jointly by exploiting the 2D interference available in the channel for improved detection performance (Zheng et al., 2014). In response to this, (Zheng et al., 2014) studied the implementation of full 2D multi-track joint signal detection and its implementation cost for shingled magnetic recording. A multi-track joint 2D soft output Viterbi (SOVA) detector was designed for

implementing the multi-track joint 2D detection. Although the full multi-track joint 2D SOVA detector seems to have some detection complexity, their result show that with the projected scaling down of CMOS technology approaching 16nm, the optimal multi-track joint 2-D detection is a viable option to consider for future high areal density recording.

To address the complexity issues of the full multi-track joint 2D SOVA detector, (Zheng et al., 2015) in a follow up paper to their prior work developed a low complexity 2D multi-track joint 2D SOVA detector for shingled magnetic recording system. They proposed two schemes for the low complexity multi-track 2D SOVA. The first approach decomposes the 2D non-binary signal space into an individual binary signal space for soft information update. Each individual track is treated separately so that soft information update is performed bit-wise on each track similar to 1D SOVA. This reduced the complexity of the overall system as a linear function with tracks rather than exponential as in the case of the complete full 2D SOVA. The second approach has some additional complexity compared to the first approach but can be applied to enhance the performance of the low-complexity 2D SOVA by dynamically adjusting the number of competing paths for soft information update. However, for the multi-track joint 2D detection, the trellis runs only in the down-track direction. It does not however perform full 2D detection which requires taking states transitions in both the cross-track and down-track directions especially when high track density is involved.

Recently, in (Abdulrazaq, Ahmed and Davey, 2015b) both linear equaliser and maximum likelihood detector were used to perform 2D equalisation in both the down-track and across-track direction to cancel the effect of ISI and ITI in shingled magnetic recording channel. Their result showed that applying linear equaliser in one direction of the interference and ML detector at the other interference direction reduced the complexity of the 2D detection. However, as the ISI along track and ITI across tracks increase, the performance of the 2D detection degrades

significantly. In (Abdulrazaq, Ahmed and Davey, 2015a) a serial concatenation of SOVA with ML detector was used to limit the complexity of 2D multi-track joint detection. While (Shafiee, Sann and Liang, 2015) proposed a novel joint Viterbi detector decoder (JVDD) that performed detection and decoding jointly on a single trellis structure. The JVDD operates on a trellis and attempt to find a sequence in the trellis that belongs to a valid codeword with minimum metric.

2.10 Summary

- The various channel models for modelling and simulation of SMR/TDMR system have described in detail. Comparison of these channel models based on design complexity and accuracy of result have been made.

- Jitter noise model as an alternative media model that captures the effect of random irregular grain sizes and irregular boundaries of medium grain has been fully described. All channel models used in this research are based on the jitter noise model introduced in this chapter.

- An overview of SMR and TDMR technologies proposed for increasing the areal density of future magnetic recording media beyond the conventional limit of 1 Tb/in^2 have been presented. A detailed description of the SMR/TDMR system architecture along with the challenges regarding the system implementation have been given.

- Signal processing method for magnetic recording channels such as coding, PR equalisation techniques and MLSD/MAP detection algorithms for 1D and 2D systems have been studied and discussed.

- Review of similar works done in areas of equalisations, coding, and detections of information from the magnetic medium have been presented.

Chapter 3

PRML Channel Modelling and Implementation

As discussed in the previous chapter, the PMR media is the most widely used recording media technology for today's HDD industry. Future recording technologies such SMR and TDMR are to be developed based on the foundation of the PMR media with modifications to support ultra-high areal densities. Therefore, it is imperative to study extensively the performance of the PMR media. This chapter details the modelling and implementation of PRML detection on the PMR media. It also discusses in detail, digital equaliser design and implementation for PR equalisation. Two types of ML detection algorithms, Viterbi algorithm and the BCJR algorithm are implemented for performance comparison. The PRML system for the PMR media has been implemented using the GNU/Linux based C programming language. BER/FER vs SNR plots were used as the performance measure for the comparison of the detector.

3.1 PRML System Model

The PRML technique is used in storage systems to combat ISI and to increase recording density. PRML technique is implemented using a PR equaliser and an ML detector. Figure 3.1 shows the schematic diagram of the PRML implementation for the PMR Channel.

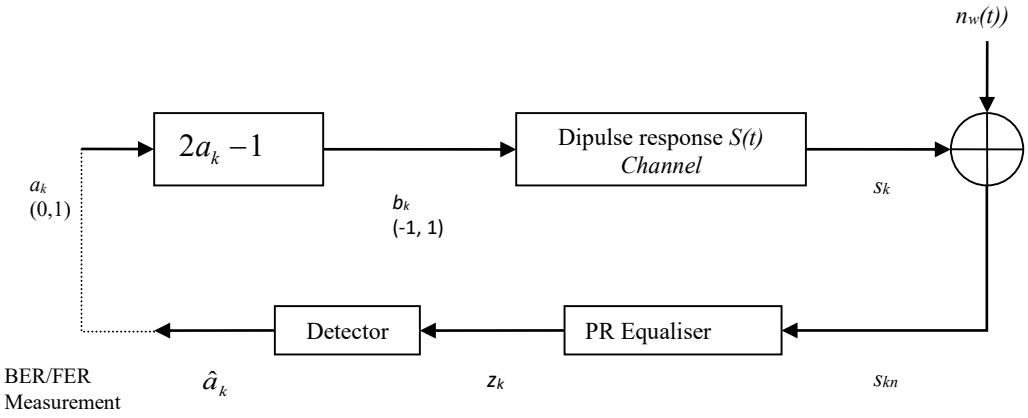


Figure 3.1: Schematic diagram of PRML implementation on PMR channel

The binary sequence a_k represents the data to be saved or recorded on the PMR media. This is generated in C-programming using the random number generator function *rand()*.The a_k sequence is mapped into sequence b_k of [1, -1] to simulate the write current using the expression $2a_k - 1$. The write current generates the magnetic transition patterns according the sequence b_k, with 1 representing the transition from state 0 to 1 and -1 representing the transition from state 1 to 0 (Awad, 2013). The transitions are recorded on the channel (PMR media) to represents the saved data. Additive white Gaussian noise source is added to the readback signal, and the result is passed for equalisation and subsequently detection.

3.2 Channel Model

The PMR channel was modelled using the jitter noise model described previously in section 2.2.4. The choice for this model is due to its computational simplicity for simulation purpose compared to other models described in the previous chapter. Also, it accounts for the net effect of irregular grain size/boundaries of the magnetic media grains, which forms the primary source of noise in high areal density recording.

3.2.1 Channel Response Modelling

The transition response read from the PMR media was modelled using the hyperbolic tangent function of equation 2.2 defined in chapter 2. The value of the peak voltage V_{max} is set to 1 for amplitude normalisation purposes. The "T_{50}" and time "t" are also normalised by the channel bit period "B". The isolated response involves the presence of a positive transition (0 to 1) at time "$t + 0B$" and then followed by a negative transition (1 to 0) at time "$t + 1B$". Therefore, this implied that response is the superposition of $s(t)$ and $s(t + 1B)$. In reading the data from the medium, the data is read at the centre of the bits. Therefore, to get the actual head response, the function is shifted by $B/2$ toward the centre of the sampled bit. The isolated response is determined using the expression as shown in equation 3.1.

$$h(t) = s\left(t + B/2\right) - s\left(t - B/2\right) \tag{3.1}$$

Now, let d_i denote the transition of data bit at time "i", for binary data, the value of d_i is one of +1, 0, or -1 for positive transition, no transition or negative transition respectively. If x represents the saved data in binary, then the transition d_i is expressed as shown in equation 3.2.

$$d_i = \frac{\left(x_i - x_{i-1}\right)}{2} \tag{3.2}$$

Then, the read signal from the PMR medium (noiseless data) is expressed as in equation 3.3.

$$y(t) = \sum_i d_i s(t - iB) \tag{3.3}$$

Substituting d_i for equation 3.2 into equation 3.3 and re-arranging the equation yielded the equation 3.4.

$$y(t) = \sum_i x_i h(t - iB) \tag{3.4}$$

Where

$$h(t - iB) = \frac{s(t - iB) - s(t - i(B + 1))}{2} \tag{3.5}$$

From the equation 3.4, it is clear that the received signal from the PMR media is represented as the convolution of the saved data bits (x) with the isolated transition response of the channel (h). The channel ISI is due to the contributions from bits positions at $iB \neq t$.

3.2.2 Timing Jitter Modelling

Timing jitter is the deviation in the transition time due the randomness of the magnetic grain's sizes and boundaries in the medium. As a result of this deviation, the transitions do not occur at the exact position of iB and $(i + 1)B$. Rather, there is a random deviation for the position of the transition. This is modelled as jitter noise represented by a white Gaussian variable a_i with zero mean and standard deviation (σ_j). It is then added into the transition time of equation 3.3 as shown in equation 3.6 (Wu, 2009).

$$y(t) = \sum_i d_i s(t - iB + a_i) \tag{3.6}$$

The jitter noise standard deviation (σ_j) is defined by the grain granularity of the media. It has high significance at higher recording densities and less effect at lower recording density. "a_i" is normally truncated to a value of $\pm 0.5B$ to avoid having bit energy values below zero.

Now equation 3.6 is expand using the Taylor's series expansion technique to further separate the interfering signals from the jitter noise. This simplifies the channel simulation process. The Taylor's expansion of equation 3.6 yielded the expression given by equation 3.7.

$$y(t) = \sum_i d_i s(t - iB) + \sum_i d_i a_i s'(t - iB) + \sum_i \frac{d_i a_i^2}{2!} s''(t - iB) + \sum_i \frac{d_i a_i^3}{3!} s'''(t - iB) + ... \quad (3.7)$$

Equation 3.7 can be reduced further by taking its first order Taylor's approximation. This is because the contributions from the higher order terms becomes negligible as the order is progressed. Therefore, equation 3.8 gives the first order Taylor's approximation of equation 3.7.

$$y(t) = \sum_i d_i s(t - iB) + \sum_i d_i a_i s'(t - iB) \quad (3.8)$$

The first term of equation 3.8 gives the data transition while the second term represents the first order approximation of the jitter noise. To get the value of the stored bit read by the Read head, the first term of equation 3.8 is substituted with equation 3.4. This yields equation 3.9.

$$y(t) = \sum_i x_i h(t - iB) + \sum_i d_i a_i s'(t - iB) \quad (3.9)$$

From the definition of $s(t)$ by the equation 2.2 in chapter 2,

$$s'(t - iB) = \frac{2}{0.579\pi T_{50}} \left(\operatorname{sech}^2 \left(\frac{2(t - iB)}{0.579\pi T_{50}} \right) \right) \quad (3.10)$$

3.2.3 Additive White Gaussian Noise

Apart from the media noise which is predominantly jitter noise in our case, other sources of noise exist in the HDD system. These include electronic noise generate by the electronic circuit components such as resistors and transistors, thermal noise generated by the amplifier circuitry, noise generated by the MR Read head, and noise due to dirt and scratches on the medium. These noises are modelled as additive white Gaussian noise (AWGN) and are subsequently added to the read signal. Therefore, the final read signal can be given by equation 3.11 as:

$$y(t) = \sum_i x_i h(t - iB) + \sum_i d_i a_i s'(t - iB) + n_i \tag{3.11}$$

AWGN is added into the signal using the AWGN generator. The AWGN generator is implemented in C-programming using the Box-Muller method (Golder and Settle, 1976). The *rand()* function generates uniformly distributed random variables which are transformed into random variable, with Gaussian distribution having a zero mean and unit variance. The magnitude of the noise is determined by signal-to-noise (SNR) which is expressed in decibel (dB) as $SNR\ (dB) = 10log_{10}(SNR)$. From this relationship, the value of the SNR can be obtained as $SNR = 10^{(SNR\ (dB)/10)}$. In relation to the signal power and the noise, the SNR is defined as: SNR = s^2 / σ_N^2 , where s^2 is the signal power: i.e its mean square value and σ_N^2 is the variance of the random Gaussian variable *N*.

3.2.4 Signal to Noise Ratio Definition

The definition of SNR in digital systems varies for different system application. For instance, in digital communications system, SNR is defined as the ratio of information bit energy to noise spectral density E_b/N_o (Awad, 2013). While this definition is almost unique to all kinds of coding or modulation schemes in communications system, it varies for magnetic recording systems depending on the medium characteristics and the operating densities. So, different definitions of SNR are adopted in the literature for studying the performance of magnetic recording channels.

The general notation adopted for SNR definition in magnetic recording channel is expressed in equation 3.12.

$$SNR = 10\log_{10}\left(\frac{S}{N}\right) \quad (dB) \tag{3.12}$$

where "*S*" is the signal power or energy and "*N*" represents the noise power.

In some literatures, the variance (σ^2) of the signal or noise is used instead of the signal or noise power (Greaves, Muraoka and Kanai, 2008). Other literatures used the peak signal of the readback waveform or the maximum voltage registered by the Read head for an ideal isolated transition instead of the signal energy. That is, V_p^2 or V_{max}^2 respectively is used in place of σ_{Signal}^2. This SNR definition $\left(\frac{V_p^2}{\sigma_{noise}^2}\right)$ was adopted by (Wu, Armand and Cruz, 2014), (Nabavi, and Kumar, 2007) and (Saito, 2015). The variance σ_{noise}^2 is considered to be from the additive white Gaussian noise only. The noise is added to the read signal before equalisation. In (Zheng and Zhang, 2015) and (Abdulrazaq, Ahmed and Davey, 2015), the SNR definition was expanded to include both the white noise energy and the jitter noise energy. Therefore, the noise energy was given as the summation of white noise and jitter noise energy added to the read signal before equalisation. Equation 3.13 gives the expression for the SNR definition used in this report.

$$SNR = 10\log_{10}\left(\frac{V_{\max}^2}{\sigma_w^2 + \sigma_j^2}\right) \quad (dB) \tag{3.13}$$

where V_{max} is the peak voltage for the isolated transition pulse, while σ_w and σ_j are the standard deviations of the AWGN (n_w) and jitter noise (n_j) respectively.

3.2.5 Channel Simulation

The channel model developed is implemented using the C-programming platform. The data to be stored is assumed to be written in sectors of 4KB (4096×8), consisting of eight tracks with each track having 4096bits/track. A guard band containing some random numbers and -1s is

placed between sectors so that, there is -1s sectors separation and random data surrounding the data sectors. The extra random data bits are added for equalisation purpose.

The input parameters for the initialisation phase of the programme are first set and inputted into the programme. These parameters include; the value of T_{50} , as a ratio of the bit period (B) i.e, normalised value, the SNR of the channel and the length of the modelling equaliser taps. The value for V_{max} is chosen to be 1 unit.

During the initial phase, the initialisation function determines the channel isolated response $h(t)$ using equation 3.1. The number of terms that are evaluated for $h(t)$, in one-bit interval, is dictated by the number of the equaliser taps chosen. The central term in the $h(t)$ array has the highest value of all terms that corresponds to the peak amplitude of the isolated response. So, when the summation of all terms in the array is taken, the result gives a 1. This means that the peak amplitude achievable for the channel response is +1 or -1. Similarly, the jitter response $s'(t)$ is determined using equation 3.10, with the same array size as $h(t)$. The central term of $s'(t)$ and the one after is chosen to have the peak amplitude of the response. $s'(t)$ is then normalised such that the sum square of its elements sums up to 2. This is to ensure that, when convolving with the transitions, the power is normalised to 1, multiplied by the jitter noise amplitude determined by the SNR value.

After the initialisation stage, random binary data is generated in software and modulated to -1 and +1 to represents the write current. For each track, the transitions are determined from x_i and saved as d_i using equation 3.2. An AWGN with variance σ_j^2 is generated, and multiplied, term by term to the transitions d_i. The result is then convolved with the jitter response $s'(t)$ to generate the jitter noise for each bit position. To ensure that the operating SNR is not exceeded after the addition of the jitter and the white noise, the amplitude of the jitter response is modified, such that, after the multiplication of "d" by "a_i", and subsequently convolution with

jitter, the noise power remains a certain percentage of the total noise (Abdualrazaq, 2017). The factor in which the amplitude is modified is given by equation 3.14. This modifying factor transforms "a_i" into an AWGN with standard deviation σ_j.

$$J = \sqrt{0.5\sum (s')^2} \tag{3.14}$$

The data to be saved x_i is also convolved with the channel isolated response $h(t)$ along the track to generate the ISI data of each track. The resulting ISI data generated is then added to the jitter noise that was already determined above. This gives a signal containing ISI and 1D jitter noise. The final 1D signal output from the channel $Z(t)$ is determined by adding AWGN of variance σ_w^2 to the resulting signal containing ISI and 1D jitter noise, as demonstrated by equation 3.11. This is then passed to the PR equaliser for equalisation.

3.3 PR Equaliser Implementation

In the PR equalisation technique, instead of removing all the ISI from signal, a controlled amount of ISI is allowed to pass through the detector. It is then handled more efficiently by using an ML detector to remove the ISI completely. This prevents the problem of AWGN amplification associated with the use of linear equaliser Zero Forcing (ZF) or MMSE in cancelling the ISI.

A PR equaliser with a GPR target polynomial is used to transform the signal shape into a desired target response. The target selection is usually determined by the coefficients representing the controlled ISI. After selecting the target, a column vector (T) of length equal to the modelling equaliser length is formed to represents the PR equaliser target vector. For example, a target length of 3 given by $[t_1, t_2, t_3]$ is transformed to column vector of the equaliser target as shown by equation 3.15.

$$T = [0,.....,0,t_1,t_2,t_3,.....,0] \tag{3.15}$$

Now with the target vector set, the coefficients of the equaliser needed to transform the signal to this target are determined using the matrix expression given by equation 3.16.

$$C_{PREQ} = H^{-1}T \tag{3.16}$$

As an example, for a 7-tap equaliser (modelling length), to shape the noisy data from the channel output to the desired target response means, finding the PR equaliser coefficients C_{PREQ}, $[c_0,c_1,c_2,c_3,c_4,c_5,c_6]$, and then convolving the noisy data with the equaliser coefficients determined from equation 3.16. The following procedure was followed to implement the PR equalisation in this work.

i. The channel isolated response $h(t)$ is approximated into a (H) matrix form of size [7×7] to suite the number of taps chosen for the equaliser. That is, using equation 3.1 for specified values of V_{max} and T_{50}, the channel response $h = [h_{n-3}, h_{n-2}, h_{n-1}, h_n, h_{n+1}, h_{n+2}, h_{n+3}]$ is represented as;

$$h = \begin{bmatrix} h_n & h_{n+1} & h_{n+2} & h_{n+3} & 0 & 0 & 0 \\ h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} & 0 & 0 \\ h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} & 0 \\ h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} \\ 0 & h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} \\ 0 & 0 & h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} \\ 0 & 0 & 0 & h_{n-3} & h_{n-2} & h_{n-1} & h_n \end{bmatrix}$$

ii. Zeros are padded to the chosen target from left and right to form a column matrix (T) of length equal to the number of taps chosen. For this implementation, target [4 6 4] was prepared for the 7-taps equaliser as; T = [0 0 4 6 4 0 0].

iii. The equaliser coefficients required for shaping the signal to the desired target are calculated by evaluating the matrix equation;

$$C_{PREQ} = \begin{bmatrix} h_n & h_{n+1} & h_{n+2} & h_{n+3} & 0 & 0 & 0 \\ h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} & 0 & 0 \\ h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} & 0 \\ h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} & h_{n+3} \\ 0 & h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} & h_{n+2} \\ 0 & 0 & h_{n-3} & h_{n-2} & h_{n-1} & h_n & h_{n+1} \\ 0 & 0 & 0 & h_{n-3} & h_{n-2} & h_{n-1} & h_n \end{bmatrix} * \begin{bmatrix} 0 & 0 & 4 & 6 & 4 & 0 & 0 \end{bmatrix}$$

C_{PREQ} gives the required coefficients of the equaliser that will shape the received signal to the required target response. These coefficients are chosen carefully to ensure that there is a minimum mean square error (MMSE) between the output of the received data and the equalised data.

iv. Finally, the noisy data output is convolved with C_{PREQ} to produce a signal whose ISI is controlled by the desired target.

3.4 Maximum Likelihood detectors

After equalisation, the signal from the output of the PR equaliser is passed to the detector for data detection. The information content of the signal is now represented by the result of the convolution of the data with the target response. Therefore, at any given point in time, the signal at that time depends on "*k*" bits or symbols previously before it. This "*k*" the number of bits or symbols is termed the constraint length of the detector, and it is evaluated as $k = TargetLength - 1$.

Table 3.1: Dibit response for target [4 6 4] with 1-bit data input.

Incoming bit	Initial state	Transitions	Final state	SOP	Dibit response
0	00	000	00	-1*4-1*6-1*4	-14
1	00	100	10	1*4-1*6-1*4	-6
0	10	010	01	-1*4+1*6-1*4	-2
1	10	110	1	1*4+1*6-1*4	+6
0	01	001	00	-1*4-1*6-1*4	-6
1	01	101	10	1*4-1*6+1*4	+2
0	11	011	01	-1*4+1*6+1*4	+6
1	11	111	11	1*4+1*6+1*4	+14

The value of the ideal equalised signal response is evaluated by taking the Sum of products (SOP) of the target response and the saved data. This gives the desired response value and forms the reference value from which the path metric of each transition is calculated. It is sometimes referred to as the dibit response (Wu, 2009) in some text. Table 3.1 shows the dibit response for the target [4 6 4] for all possible bit combination as example. The value of the dibit response for the transition at any given point in time depends on the initial state and current incoming bit. This also determined the next state of the transition. A trellis diagram similar to that of Figure 2.11 can be used to work out the transitions for each of the states with their corresponding dibit response.

The number of states for the trellis in this example (for $n = 1$ bit input and target length 3) is $2^{n\times k} = 2^{1\times 2} = 4$, and each state has $2^n = 2$ number of incoming and outgoing branches per state. An ML detector operating based on this trellis structure is used to detect the data out of the remaining interference in the system. The detector can be implemented using the VA for MLSD detection or the BCJR algorithm for MAP detection. The following sections discuss the implementation of the detector using both VA and BCJR detection algorithms.

3.4.1 Viterbi Detector Implementation

The VA implements MLSD by finding the best path through the trellis. The path metric is calculated based on the Euclidean distance between the received symbol and the ideal target symbol. At any time interval "*t*", within the trellis, the path metrics are calculated for each and every transition. Then, at each state, all the path metrics entering the state are compared. The best path metric is selected as the *survivor path* which is stored and then used as the next state metric. This process continues until the end of the trellis is reached where the best state is selected, and then the *traceback* process is started from that state. The following example demonstrates how the VA was implemented in the PMR media.

3.4.2 Example of VA implementation for PMR channel

This section presents a step-by-step implementation example of the VA in PMR channel. Suppose we have a data sequence a_k [*0 0 1 0 1 1 0 0 1 0 0*] to be recorded on the disk. The data signal is to be equalised to a target of [*4 6 4*] and the channel contains AWGN. The noise sequence generated at the output of the channel representing the AWGN contribution and other impairments is given as n_k [*0.681 -1.161 0.09 1.564 0.95 -0.61 0.999 -1.55 -0.66 1.00 0.333*]. A trellis structure with four states and two incoming and outgoing branches per state was used to implement the VA algorithm. After mapping the data, convolving it with the channel dibit response, and adding the noise to the result, the Viterbi detection process is carried out as follows:

i. The first state at the beginning of the trellis is initialised to a state metric of 0 and the remaining states are assigned higher values greater than 1 (1500) each. This initialisation ensures that the trellis begins at state 00.

ii. At any given time "*t*", the branch metric is calculated for each path transition according to equation 2.33. i.e. for our example;

At $t = 1$, $y_1 = -5.319$ i.e ($-6 + 0.681$) was received, then branch metrics are:

- 000 i.e. from state 00 to state 00; $(-14 - (-5.319))^2 = 75.35976$
- 001 i.e. from state 00 to state 01; $(-6 - (-5.319))^2 = 0.463761$
- 010 i.e. from state 01 to state 10; $(-2 - (-5.319))^2 = 11.01576$
- 011 i.e. from state 01 to state 11; $(6 - (-5.319))^2 = 128.1198$
- 100 i.e. from state 10 to state 00; $(-6 - (-5.319))^2 = 0.463761$
- 101 i.e. from state 10 to state 01; $(2 - (-5.319))^2 = 53.56776$
- 110 i.e. from state 11 to state 10; $(6 - (-5.319))^2 = 128.1198$
- 111 i.e. from state 11 to state 11; $(14 - (-5.319))^2 = 373.2238$

The same procedure is applied to calculate the rest of the branch metric for each received symbol in a given time interval up to last sequence received.

iii. The next state metric is the previous state metric plus the branch metric transiting to that state. However, at each state, the *survivor metric* is evaluated by comparing the next state metrics and then, selecting the lowest metric as the survivor. This metric is saved as the metric for the next state transition. In our example at $t=1$,

- For state 00; the next state metric is computed as $min\ \{(0 + 75.35976), (1500 + 0.463761)\}$.

- For state 01; the next state metric is computed as *min* {(*0 + 0.463761*), (*1500 + 53.56776*)}.

- For state 10; the next state metric is computed as *min* {(*1500 + 11.01576*), (*1500 + 128.1198*)}.

- For state 11; the next state metric is computed as *min* {(*1500 + 128.1198*), (*1500 + 373.2238*)}.

iv. The history of the symbol responsible for the transition that produces the best metric, or the survivor metric is keep on a register which will be used later during the trace back process.

In our implementation at *t=1*.

- For state 00; *if* {(*0 + 75.35976*) ≤ (*1500 + 0.463761*)} *history = 0, else history = 1.*

- For state 01; *if* {(*0 + 0.463761*) ≤ (*1500 + 53.56776*)} *history = 0, else history = 1*

- For state 10; *if* {(*1500 + 11.01576*), ≤ (*1500 + 128.1198*)} *history = 0, else history = 1*

- For state 11; *if* {(*1500 + 128.1198*), ≤ (*1500 + 373.2238*)} *history = 0, else history = 1*

v. Finally, the trace back process starts as soon as the last symbol is received at the end of the trellis. The state with the lowest metric value is selected as the best state and the trace back process starts from that state. The history of each transition is taken as the outputted

data at that state as shown in Figure 3.2, which depicts the VA approach using a trellis diagram.

Table 3.2 summarizes the decoding process using the VA for PMR channel. It gives the values computed for all branch metrics, state metrics survivor paths, the history register and the trace back data. The implementation of the VA was done using Microsoft excel spread sheet to demonstrate the application of VA in the PMR media.

Table 3.2 Viterbi algorithm for PMR channel implementation example in excel

target		4	6	4							
data		0	0	1	0	1	1	0	0	1	0	0
mapped		-1	-1	1	-1	1	1	-1	-1	1	-1	-1
dibit		-6	-2	2	6	6	-6	-6	-2	-6	-10	-4
noise		0.681	-1.161	0.09	1.564	0.95	-0.61	0.999	-1.55	-0.06	1	0.333
noisy		-5.319	-3.161	2.09	7.564	6.95	-6.61	-5.001	-3.55	-6.06	-9	-3.667
Branch Metric												
000		75.3598	117.484	258.888	465.006	438.903	54.6121	80.982	109.203	63.0436	25	106.771
001		0.46376	8.05992	65.4481	183.982	167.703	0.3721	0.998	6.0025	0.0036	9	5.44289
010		11.0158	1.34792	16.7281	91.4701	80.1025	21.2521	9.006	2.4025	16.4836	49	2.77889
011		128.12	83.9239	15.2881	2.4461	0.9025	159.012	121.022	91.2025	145.444	225	93.4509
100		0.46376	8.05992	65.4481	183.982	167.703	0.3721	0.998	6.0025	0.0036	9	5.44289
101		53.5678	26.6359	0.0081	30.9581	24.5025	74.1321	49.014	30.8025	64.9636	121	32.1149
110		128.12	83.9239	15.2881	2.4461	0.9025	159.012	121.022	91.2025	145.444	225	93.4509
111		373.224	294.5	141.848	41.4221	49.7025	424.772	361.038	308.003	402.404	529	312.123
State Metric												
00		0	75.3598	192.844	67.2598	283.658	260.992	5.54048	86.5225	94.309	8.94458	33.9446
01		1500	0.46376	83.4197	1.81978	130.634	117.792	79.3005	6.53848	92.525	73.9046	17.9446
10		1500	1511.02	1.81168	99.6758	93.2899	5.16838	139.044	88.3065	8.94098	109.009	122.905
11		1500	1628.12	84.3877	98.7078	4.26588	53.9684	276.804	200.322	97.741	237.969	298.905
History												
00			0	0	1	1	1	1	0	1	1	0
01			0	0	1	1	1	1	0	0	1	0
10			0	0	1	0	1	0	0	0	0	0
11			0	0	0	0	1	0	0	0	0	0
Traceback Data			0	0	1	0	1	1	0	0	1	0
State Transitted			1	2	1	3	2	0	1	2	0	1

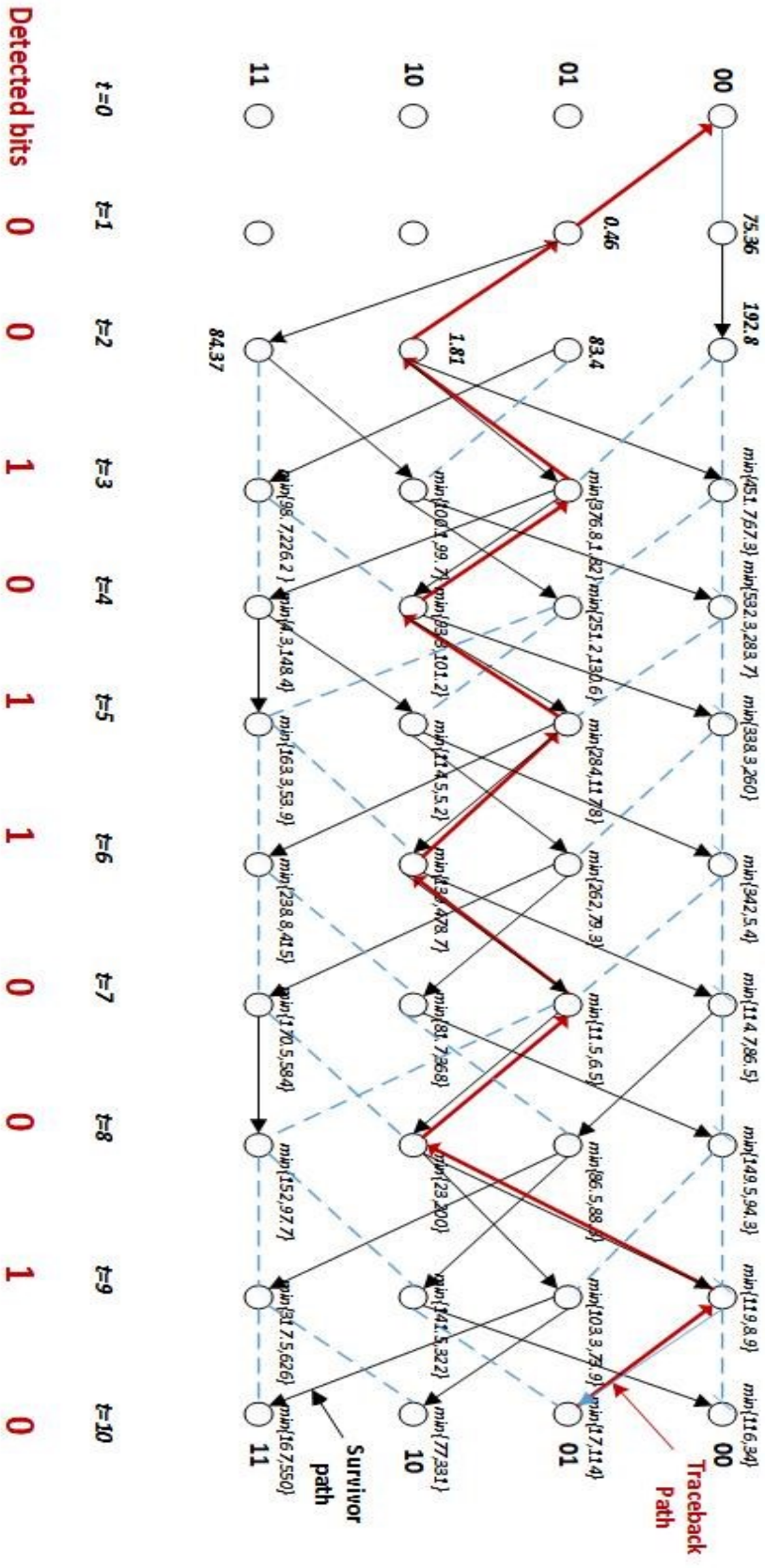


Figure 3.2: Trellis diagram of the VA detector showing the traceback path (Red), survivor path (Black with arrow head) and the detected bits.

3.4.3 BCJR Detector Implementation

The BCJR decoder is a MAP decoder that operates on bit-wise manner. It decodes the data bit by bit using the trellis structure and the a-priori probability to find the APP of the received data. The APP determines whether the received data is 1 or 0. The BCJR algorithm can be implemented in PMR channel for MAP detection. The outline of the BCJR algorithm implemented in the PMR channel is discussed in the next section.

3.4.4 Example of BCJR implementation for PMR channel

This section presents the practical example of BCJR decoding in PMR channel. The same set of data sequence a_k, GPR target, and noise n_k sequence used in the previous example of section 3.5.1.1 is adopted. A trellis structure with four states and two incoming and outgoing branches per state was also adopted. The BCJR algorithm was implemented as follows:

i. *Branch metric calculation*: The branch metric presenting each state transition was calculated for each state at any given time interval using equation 2.37. For instance, in our practical implementation example;

At time $t = 1$, when $y_1 = -5.319$, i.e. $(-6 + 0.681)$ was received, the branch metrics are calculated as:

- 000 i.e. from state 00 to state 00; $e^{-\left(\frac{-14-(-5.319)}{2\times1}\right)^2} = 7E-09$
- 001 i.e. from state 00 to state 01; $e^{-\left(\frac{-6-(-5.319)}{2\times1}\right)^2} = 0.8905$
- 010 i.e. from state 01 to state 10; $e^{-\left(\frac{-2-(-5.319)}{2\times1}\right)^2} = 0.0637$

- 011 i.e. from state 01 to state 11; $e^{-\left(\frac{6-(-5.319)}{2\times1}\right)^2} = 1E-14$
- 100 i.e. from state 10 to state 00; $e^{-\left(\frac{-6-(-5.319)}{2\times1}\right)^2} = 0.8905$
- 101 i.e. from state 10 to state 01; $e^{-\left(\frac{2-(-5.319)}{2\times1}\right)^2} = 2E-06$
- 110 i.e. from state 11 to state 10; $e^{-\left(\frac{6-(-5.319)}{2\times1}\right)^2} = 1E-14$
- 111 i.e. from state 11 to state 11; $e^{-\left(\frac{14-(-5.319)}{2\times1}\right)^2} = 3E-41$

The same procedure is applied to calculate the rest of the branch metric for each received symbol at a given time interval up to last sequence received.

ii. *Alpha initialisation and calculation (forward recursion)*: At the beginning of the trellis, the alpha value for the first state 00 is initialised to 1 and the rest are initialised to 0. This force the trellis to begin from the state 00. The alpha values are then computed recursively from the beginning to the end of the trellis using equation 2.38. For instance, in our practical implementation example, at time *t = 1*;

- Alpha for state 00 is $(1\times7E-09+0\times0.8905) = 7E-09$
- Alpha for state 01 is $(7E-09\times0.8905+0\times2E-06) = 0.8905$
- Alpha for state 10 is $(0\times0.0637+0\times1E-14) = 0$
- Alpha for state 11 is $(0\times1E-14+0\times3E-41) = 0$

After computing all the values of alpha up to the end to the trellis where the last symbol is received, the alpha values are normalised to unity. For example; at time interval *t = 1*;

- Normalised alpha value for state 00 is $\left(\frac{7E-09}{7E-09+0.8905+0+0}\right)=7E-09$

- Normalised alpha value for state 01 is $\left(\frac{0.8905}{7E-09+0.8905+0+0}\right)=1$

- Normalised alpha value for state 10 is $\left(\frac{0}{7E-09+0.8905+0+0}\right)=0$

- Normalised alpha value for state 11 is $\left(\frac{0}{7E-09+0.8905+0+0}\right)=0$

iii. *Beta initialisation and calculation* (*Backward recursion*): Once the last symbol in the data sequence is received at the end of the trellis, the calculation of beta recursion is started. At the end of the trellis, the value of beta for the first state 00 is initialised to 1 and the rest set to 00. This makes it possible to terminate the data at state 00. Then, the values of beta are calculated recursively from the trellis end towards the beginning of the trellis at each time interval, using equation 2.39. For example, in our practical implementation, at time interval $t = n - 1$;

- Beta for state 00 is $(1\times 0+0\times 0.26)=0$

- Beta for state 01 is $(0\times 0.5+0\times 0)=0$

- Beta for state 10 is $(1\times 0.26+0\times 0)=0.26$

- Beta for state 11 is $(0\times 0+0\times 0)=0$

After computing all the values of beta recursively from the end of the trellis to its beginning, the values of beta are then normalised.

For instance, at time interval $t = n - 1$;

- Normalised beta value for the state 00 is $\left(\frac{0}{0+0+0.26+0}\right)=0$

- Normalised beta value for the state 01 is $\left(\frac{0}{0+0+0.26+0}\right)=0$

- Normalised beta value for the state 10 is $\left(\frac{0.26}{0+0+0.26+0}\right)=0$

- Normalised beta value for the state 10 is $\left(\frac{0}{0+0+0.26+0}\right)=0$

iv. The APP value across each trellis section corresponding to the probability of transition due to either 1 or 0 is received is calculated using equation 2.40 with normalised values of alpha and beta. For example;

- APP for the first received symbol to be 0 is computed as:

  APP (*0*) = (*1*×*7E-09*×*2E-07* + *0*×*0.0637*×*2E-08* + *0*×*0.8905*×*2E-07* + *0*×*1E-14*×*2E-08*) = *2E-15*

  APP (*1*) = (*1*×*0.8905*×*1* + *0*×*1E-14*×*1E-09* + *0*×*2E-06*×*1* +*0*×*3E-41*×*1E-09*) = *0.8905*

  The same procedure is followed to compute all the APPs cross each trellis section from beginning up to the end of the trellis.

v. Finally, the *log likelihood ratio* (*LLR*) is calculated by taking the ratio of APP (1) to that of APP (0) i.e. *LLR* = *APP* (*1*)*/APP* (*0*). Then, decision about the data is taken based on the LLR value. For example;

- For the first bit received; $LLR=\frac{APP(1)}{APP(0)}=\frac{0.8905}{2E-15}=6E+14$

- Then we take the decision as; *if {LLR > 1}, decoded bit = 1 else decode bit = 0*

Table 3.3 summarizes the implementation of the BCJR decoding algorithm in the PMR channel. The table shows the values of the computed branch metric, all the alpha values calculated recursively and their corresponding normalised values, and all the beta values computed recursively with their corresponding normalised values. It also contains the APP values calculated across the entire trellis structure and the LLR values together with decision taken.

3.5 Results and Discussion

This section presents the simulation results obtained from the developed PRML channel model depicted by Figure 3.1. The performance of the PRML channel was measured by computing the number of errors obtained between the given saved data bits and the detected data bits. BER/FER vs SNR plots obtained from computer simulations are used for performance analysis purposes.

In high density magnetic recording systems, jitter noise is the dominant source of noise in the channel more than any other noise source (Krishnan et al., 2009). Therefore, in the channel implementation, jitter noise was set to constitute 80% of the total channel noise while white noise constitutes the remaining 20% of the channel noise. To make sure that our channel and the PR equaliser modelled are up and running before adding the detector into the PRML model, we evaluate the performance of the PMR channel with and without the PR equaliser. The effect of the PR equaliser on the signal from the channel output before detection is shown in Figure 3.3 for values of $T_{50} = 1.0$, and $T_{50} = 2.0$.

target	4	6	4										sigma	1
data	0	0	1	0	1	1	0	0	1	0	0			
mapped	-1	-1	1	-1	1	1	-1	-1	1	-1	-1			
dibit	-6	-2	2	6	6	-6	-6	-2	-6	-10	-4			
noise	0.681	-1.161	0.09	1.564	0.95	-0.61	0.999	-1.55	-0.06	1	0.333			
noisy	-5.319	-3.161	2.09	7.564	6.95	-6.61	-5.001	-3.55	-6.06	-9	-3.667			
Gamma														
000	6.6E-09	1.8E-13	7.8E-29	3.3E-51	2.2E-48	1.2E-06	1.6E-09	1.4E-12	1.4E-07	0.00193	2.6E-12			
001	0.89053	0.13332	7.8E-08	1.1E-20	6.2E-19	0.91117	0.77919	0.22299	0.9991	0.1054	0.25648			
010	0.06368	0.71392	0.01527	1.2E-10	2E-09	0.00493	0.10524	0.54847	0.01623	4.8E-06	0.49921			
011	1.2E-14	7.7E-10	0.02188	0.54252	0.79802	5.4E-18	7.2E-14	1.3E-10	1.6E-16	3.7E-25	7.1E-11			
100	0.89053	0.13332	7.8E-08	1.1E-20	6.2E-19	0.91117	0.77919	0.22299	0.9991	0.1054	0.25648			
101	1.5E-06	0.00128	0.99798	0.00044	0.00219	8.9E-09	4.8E-06	0.00045	8.8E-08	7.3E-14	0.00033			
110	1.2E-14	7.7E-10	0.02188	0.54252	0.79802	5.4E-18	7.2E-14	1.3E-10	1.6E-16	3.7E-25	7.1E-11			
111	3E-41	1.1E-32	4E-16	3.2E-05	4E-06	7.6E-47	6.3E-40	3.6E-34	2E-44	3.7E-58	1.3E-34			
Alpha														
00	1	6.6E-09	1.2E-21	5E-08	3E-31	5.2E-29	0.25029	4E-10	5.8E-11	0.10687	0.00021	1.2E-14		
01	0	0.89053	8.8E-10	0.63448	1.2E-14	1.9E-13	2.5E-09	0.19503	9E-11	9.5E-09	0.01126	5.3E-05		
10	0	0	0.63577	2.8E-11	8.5E-11	0.27469	9.1E-16	2.6E-10	0.10697	1.5E-12	4.6E-14	0.00562		
11	0	0	6.9E-10	1.9E-11	0.34422	1.4E-06	1E-30	1.8E-22	2.4E-11	1.5E-26	3.5E-33	8E-13		
Beta														
00	1.2E-14	3.3E-21	1.5E-21	9.4E-43	2.3E-36	2.6E-08	4.8E-14	9.8E-16	1.2E-06	4.9E-15	2.6E-12	1		
01	1.5E-23	1.4E-14	2.5E-20	1.9E-14	8.9E-23	3.8E-18	2.9E-08	6.2E-14	4.4E-15	1.2E-06	0	0		
10	2.4E-20	2.3E-22	1.9E-14	3.9E-26	8.2E-21	4.4E-14	7.6E-16	2.7E-07	1.1E-13	2.7E-13	0.25648	0		
11	2.9E-36	1.5E-23	8.5E-28	1.1E-18	3.5E-14	4.1E-33	2E-20	1.4E-23	4.4E-29	9.5E-26	0	0		
Prob														
0x	1.6E-15	0.71392	9E-23	3.1E-17	1.4E-06	1.5E-06	1E-09	5.1E-08	4E-09					
1x	0.89053	1.3E-15	0.99792	0.54252	7.7E-23	8.9E-09	1.8E-07	1.6E-18	8.9E-08					
LLR	5.6E+14	1.8E-15	1.1E+22	1.8E+16	5.7E-17	0.00582	171.814	3.2E-11	22.1551					
Detected Bits	1	0	1	1	0	0	1	0	1					
								Bit in error						

Norm Alpha												
	1	7.4E-09	1.8E-21	7.9E-08	8.7E-31	1.9E-28	1	2.1E-09	5.4E-10	1	0.01799	2.2E-12
	0	1	1.4E-09	1	3.6E-14	6.7E-13	9.8E-09	1	8.4E-10	8.9E-08	0.98201	0.00932
	0	0	1	4.5E-11	2.5E-10	0.99999	3.6E-15	1.3E-09	1	1.4E-11	4E-12	0.99068
	0	0	1.1E-09	3E-11	1	5E-06	4E-30	9.1E-22	2.3E-10	1.4E-25	3.1E-31	1.4E-10
Norm Beta												
	1	2.4E-07	7.9E-08	4.9E-29	6.5E-23	1	1.7E-06	3.6E-09	1	4E-09	1E-11	1
	1.2E-09	1	1.3E-06	0.99994	2.5E-09	1.4E-10	1	2.3E-07	3.6E-09	1	0	0
	2E-06	1.7E-08	1	2E-12	2.3E-07	1.7E-06	2.6E-08	1	9.3E-08	2.2E-07	1	0
	2.3E-22	1.1E-09	4.4E-14	5.9E-05	1	1.6E-25	6.9E-13	5.2E-17	3.6E-23	7.8E-20	0	0

Table 3.3 BCJR algorithm for PMR channel implementation example in excel

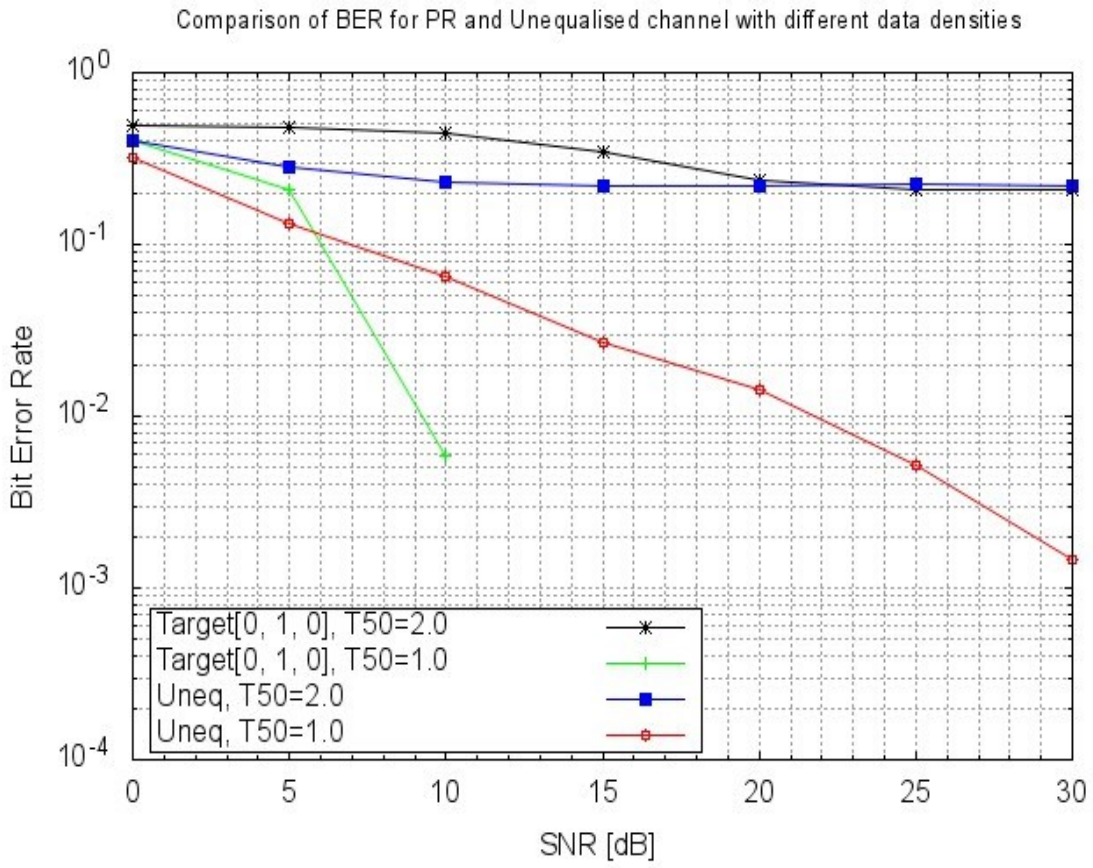


Figure 3.3: Performance of PR equaliser before detection.

Figure 3.3 shows the BER vs SNR plot of the PMR channel with and without the PR equaliser. The values of $T_{50} = 1.0$ and $T_{50} = 2.0$ represent the data densities along-track direction. A PR target [0, 1, 0] (PR4) and an equaliser length of 21 was assumed initially. It can be seen in the fact that, the PR equaliser when applied was able to reduce the amount of ISI present in the signal to an acceptable limit in which can be handle by the detector effectively. This is more observed at lower data densities, where the PR equaliser is more effective in removing the ISI present within the signal without necessary using a detector. But at higher data density, the ISI is very severe to the extent that it cannot be completely suppressed. Therefore, the equaliser can only reduce the amount of the ISI within the signal to a control level which the detector can handle. Hence, a detector is needed to deal with the remaining ISI present within the signal.

There are a couple of parameters that need to be considered carefully when analysing the performance of the PRML channel. These parameters significantly affect the performance of the ML detector. Among them are the length of the PR equaliser (equaliser taps) used to equalise the data; the data density along the track represented by the T_{50} value, and the equaliser PR target.

Figure 3.4 shows the effect of the equaliser taps on the performance of the MAP detector for $T_{50} = 1.0$. Preference is made on odd equaliser taps so as to achieve having symmetric equalisers. As it can be seen in the Figure 3.4, equaliser with 5 taps has an inferior performance compared to equalisers with taps above 5 (9-15). Therefore, for $T_{50} = 1.0$, an equaliser with 9 taps is sufficient for good performance, as increasing the number of the taps beyond 9 does not translate to any performance improvement instead adds complexity.

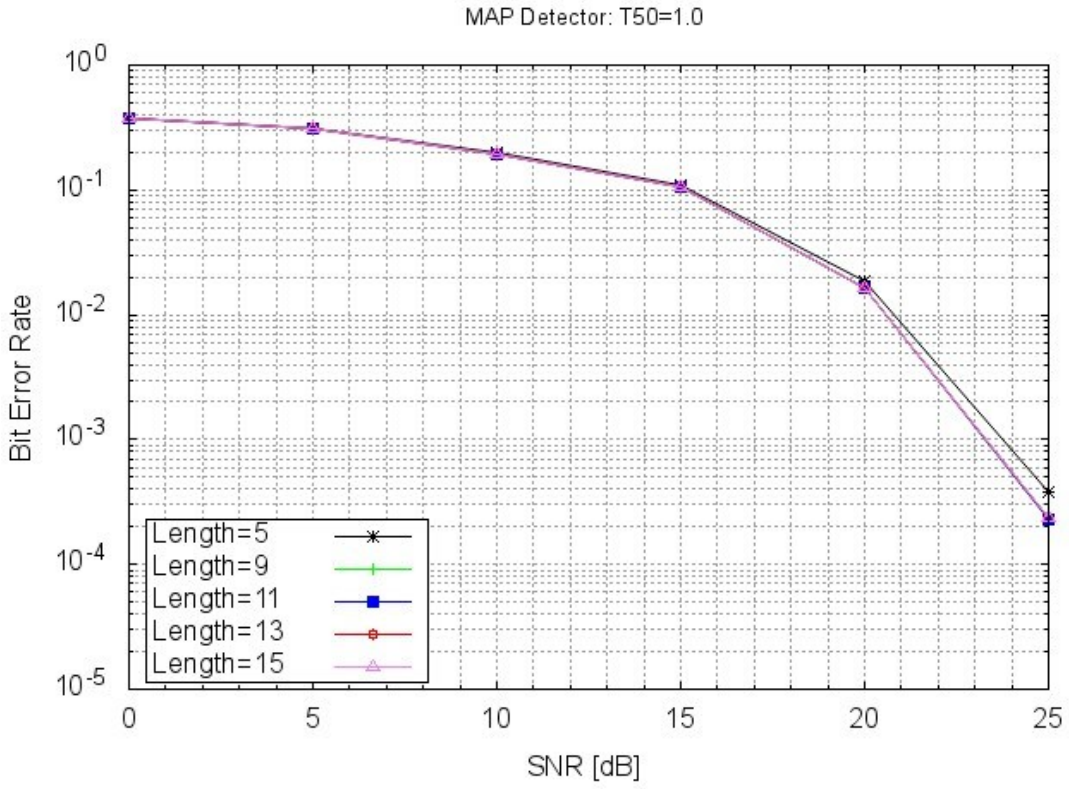


Figure 3.4: Performance of MAP detector with different equaliser lengths at $T_{50} = 1.0$.

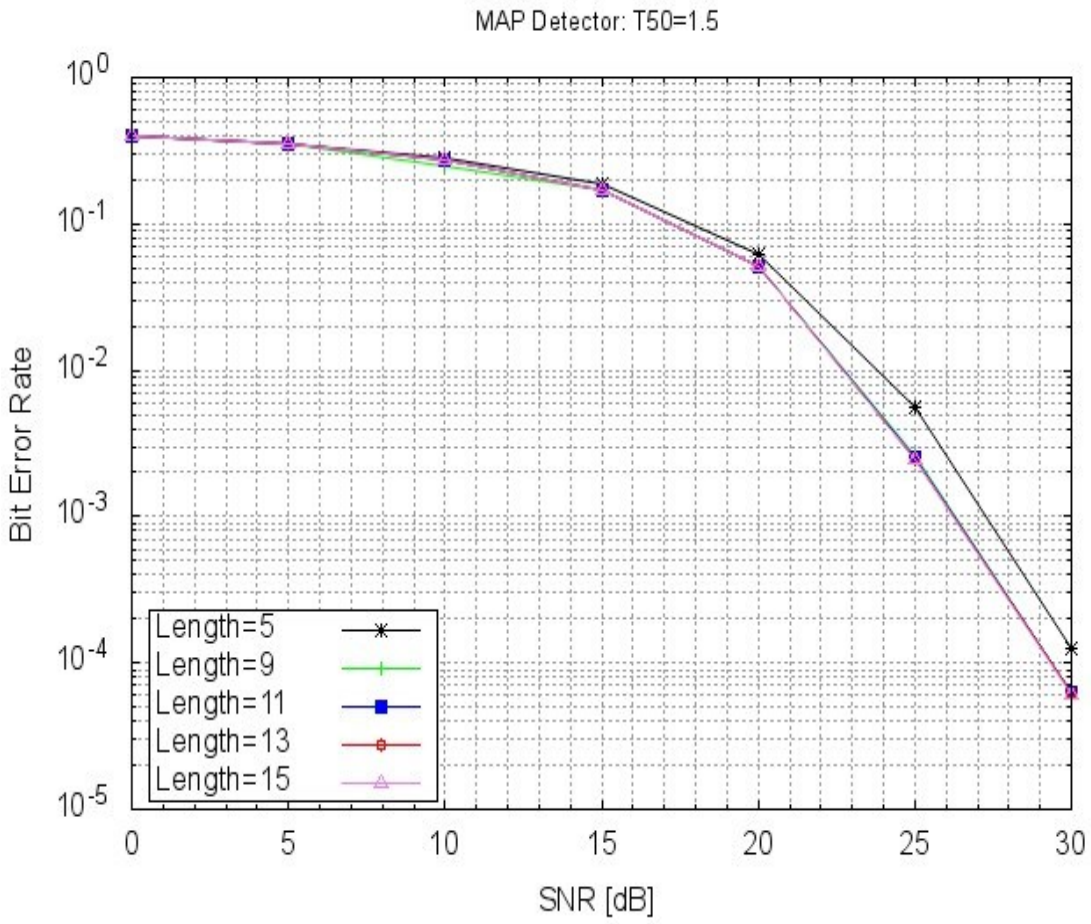


Figure 3.5: Performance of MAP detector with different equaliser lengths at $T_{50} = 1.5$.

A similar performance is observed for the equaliser taps at $T_{50} = 1.5$ as depicted by Figure 3.5. The loss in performance by the equaliser with 5 taps is more evident in this scenario as compared to the case of $T_{50} = 1.0$. But the performance of equalisers with taps above 5 (9-15) is similar in all the cases. However, when the data density along the track is increased, as for the case of $T_{50} = 2.0$ shown in Figure 3.6, the performance of equaliser with 9 taps becomes inferior to other higher equaliser taps above it (11-15). The performance degradation is as a result of errors within the equaliser introduced into the system. But these errors can be overcome when equalisers of higher lengths are employed. Therefore, in this scenario where high data density is involved ($T_{50} = 2.0$), equaliser taps of length 11 and above are needed for good

detection performance. Hence, equaliser length between the ranges of 11-15 will be adopted in our analysis for optimal results throughout the rest of this section.

After finding the best equaliser length that will achieve good detection performance, the next task is to select the GPR target that has the best performance in order to obtain good results.

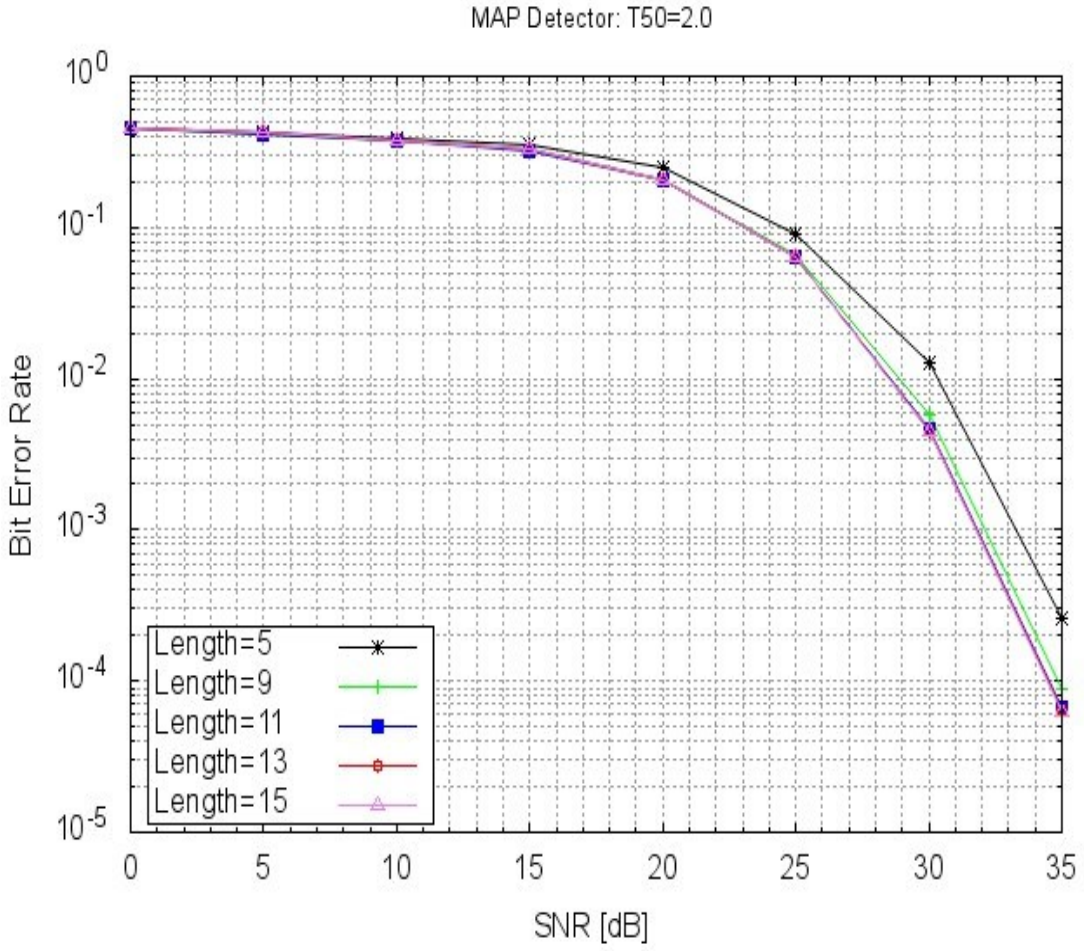


Figure 3.6: Performance of MAP detector with different equaliser lengths at $T_{50} = 2.0$.

An exhaustive search for the suitable GPR equaliser target was carried out to select the best target for the PRML simulation model that was developed. Both symmetric and non-symmetric targets of length 3 are considered in the search for the best GPR equaliser target. The effect of the different GPR targets under various degrees of data density along the track on the

performance of the detector was investigated in order to determine the best GPR target. This will ensure that this analysis is taken based on the best possible result that was obtained.

Figure 3.7 depicts the bit error performance of the PRML detector (MAP detector) with symmetric GPR targets at low data density ($T_{50} = 1.0$) along the track. As it can be seen from the figure, the GPR target [4, 5, 4] has the best performance compared to the other symmetric GPR targets at low data density within the SNR region of 15-20 dB. However, as the SNR value is increased (25 dB above), the other GPR targets [3, 5, 3] and [1, 2, 1] tries to slightly catch-up with the [4, 5, 4] target in terms of performance. The two GPR targets [3, 5, 3] and [1, 2, 1] have similar performance. The GPR target [1, 5, 1] perform worst as compared to all the symmetric GPR targets tested at this condition of low data density along track.

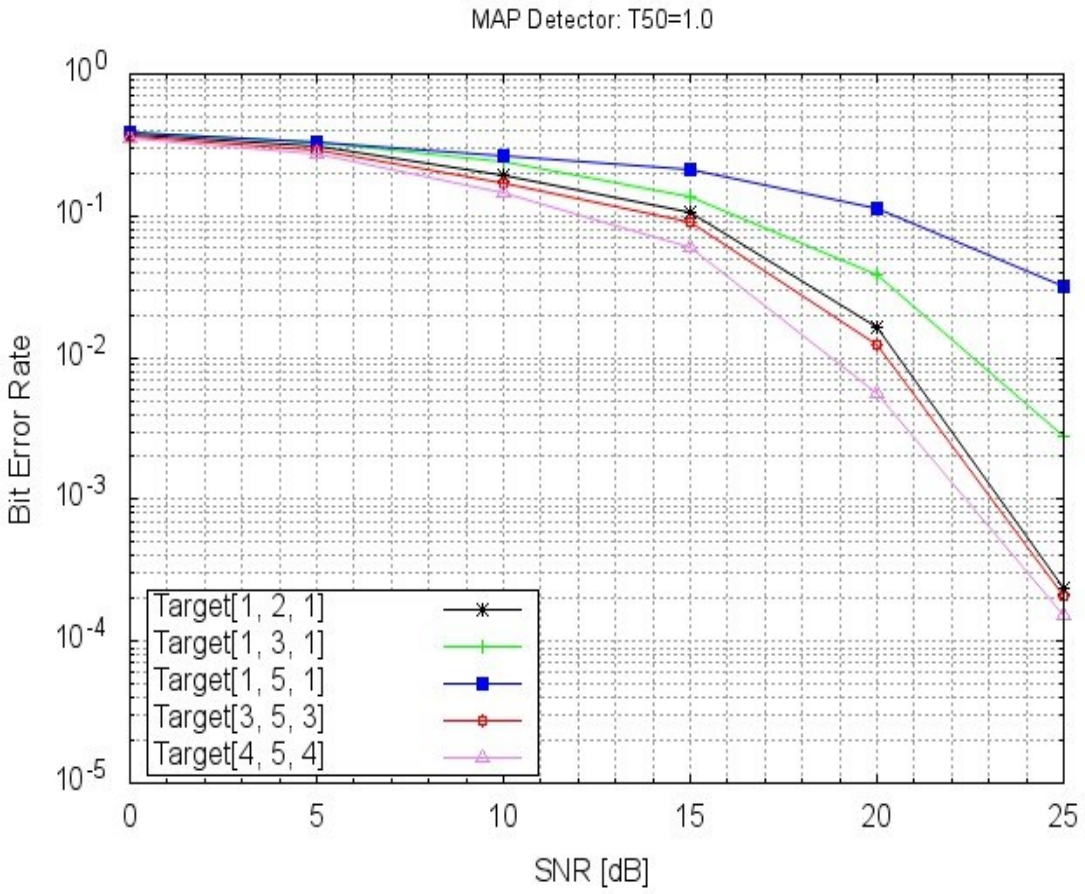


Figure 3.7: Comparison of symmetric GPR targets at $T_{50} = 1.0$.

The performance of the MAP detector with symmetric GPR targets at $T_{50} = 1.5$ is shown in Figure 3.8. As it can be observed by the figure, the performance of the GPR target [3, 5, 3] degrades as the SNR value increases beyond 24 dB, while that of GPR target [1, 2, 1] improves with increase in the SNR value.

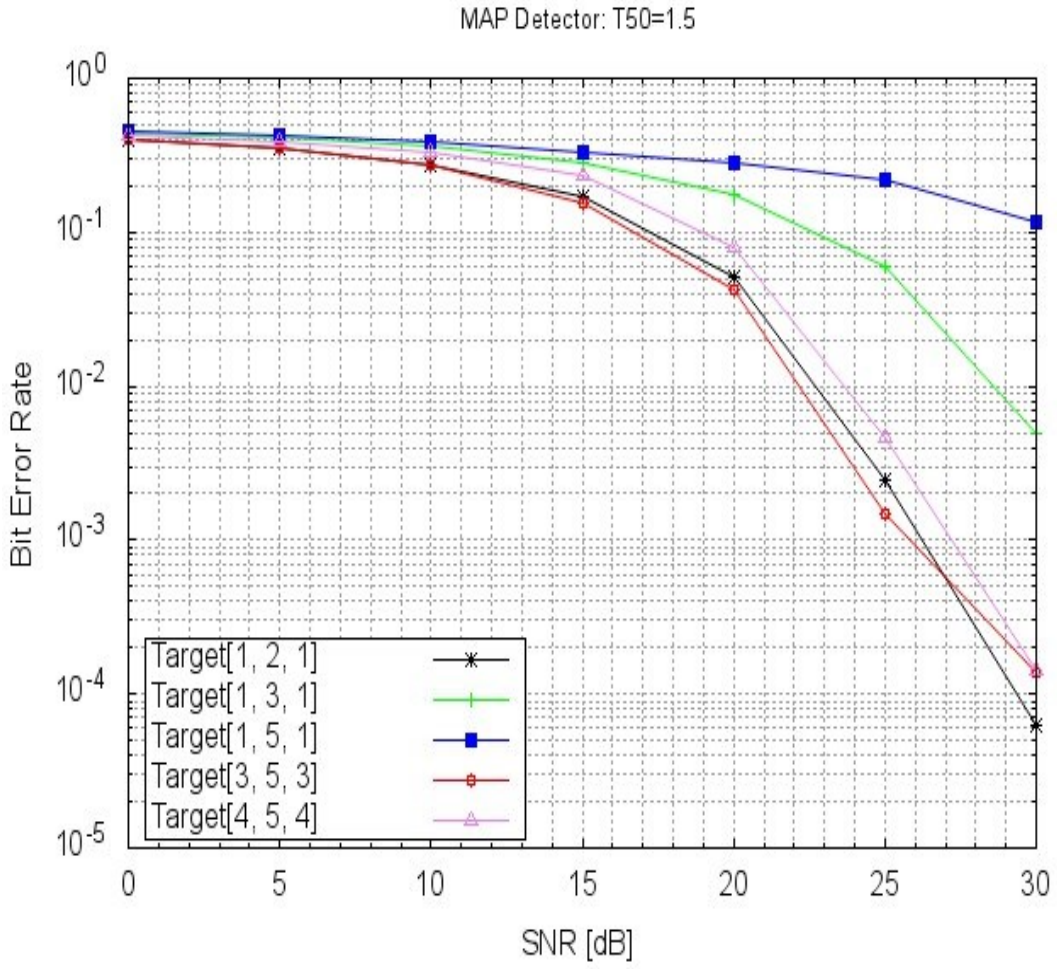


Figure 3.8: Comparison of symmetric GPR targets at $T_{50} = 1.5$.

In Figure 3.9, the GPR target [1, 2, 1] shows superior performance compared to all the other symmetric GPR targets tested for the MAP detector at high data density of $T_{50} = 2.0$ along

track. This because the target [1, 2, 1] provides good separation between the interfering symbol bits within the data and this improve the performance of the detector.

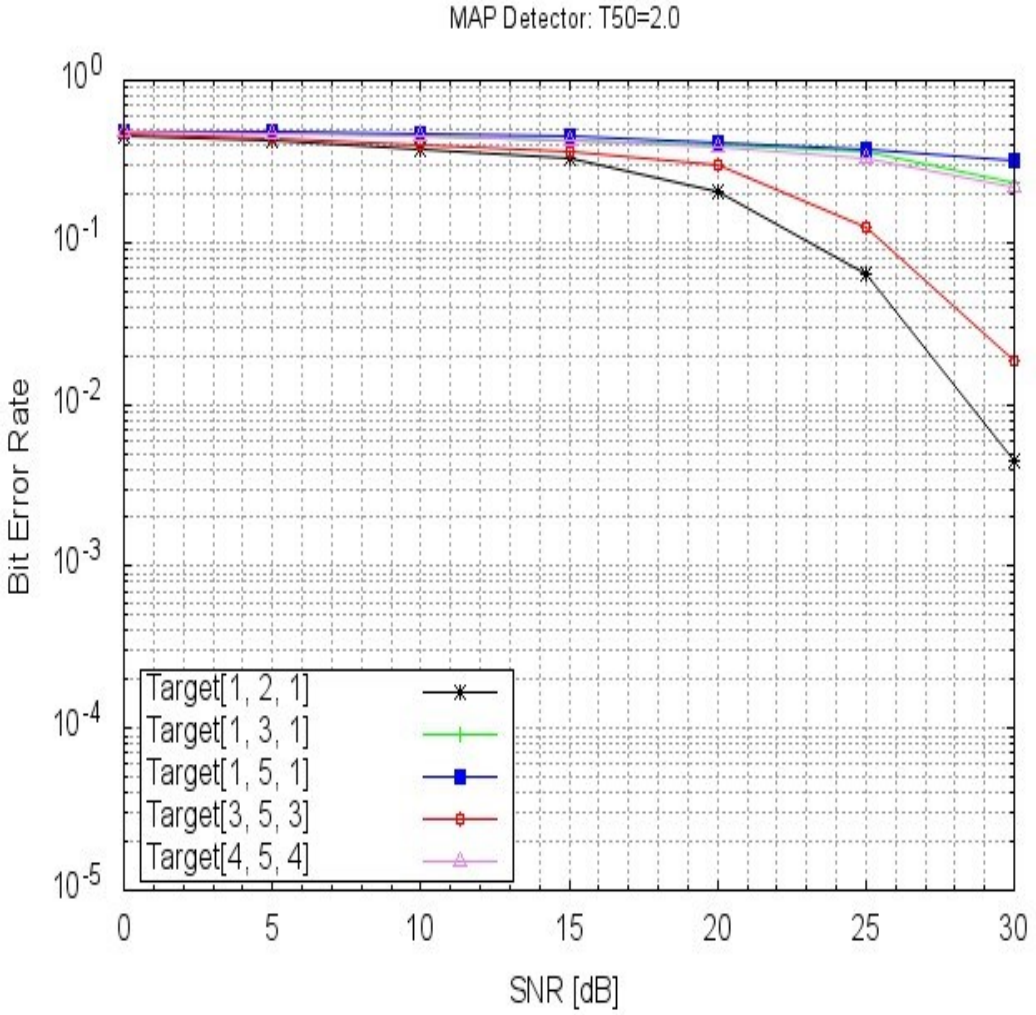


Figure 3.9: Comparison of symmetric GRP targets at $T_{50} = 2.0$.

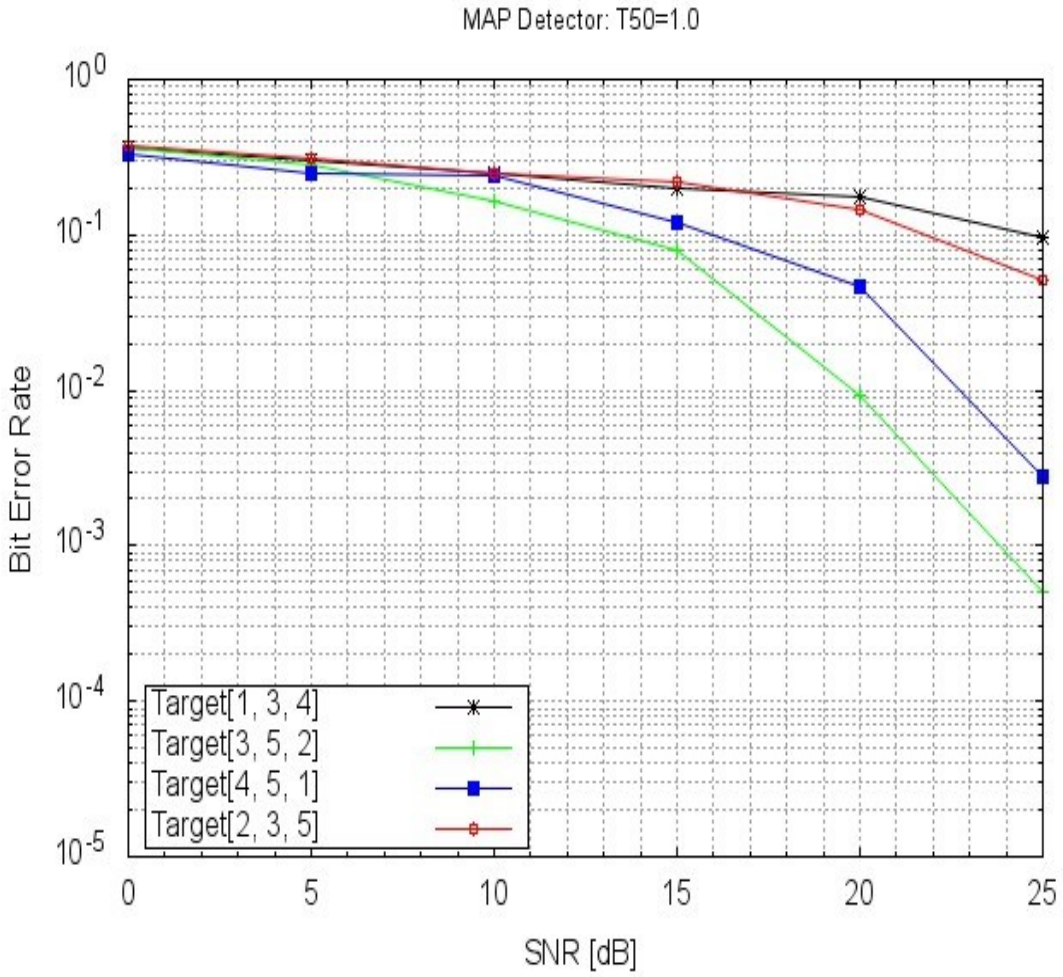


Figure 3.10: Comparison of non-symmetric GPR targets at $T_{50} = 1.0$.

Similarly, Figure 3.10 to Figure 3.12 shows the performances of the non-symmetric GPR targets on the PRML channel with densities at $T_{50} = 1.0$, $T_{50} = 1.5$, and $T_{50} = 2.0$ respectively. The GPR target [3, 5, 2] outperformed all the other non-symmetric GPR targets tested at both conditions of high and low data density along the track (at $T_{50} = 2.0$ and $T_{50} = 1.0$, see Figure 3.10 and Figure 3.12). It is observed that the best performance obtained when using the non-symmetric targets is recorded at $T_{50} = 1.5$ (see Figure 3.11), that is when the data density along the track is moderate.

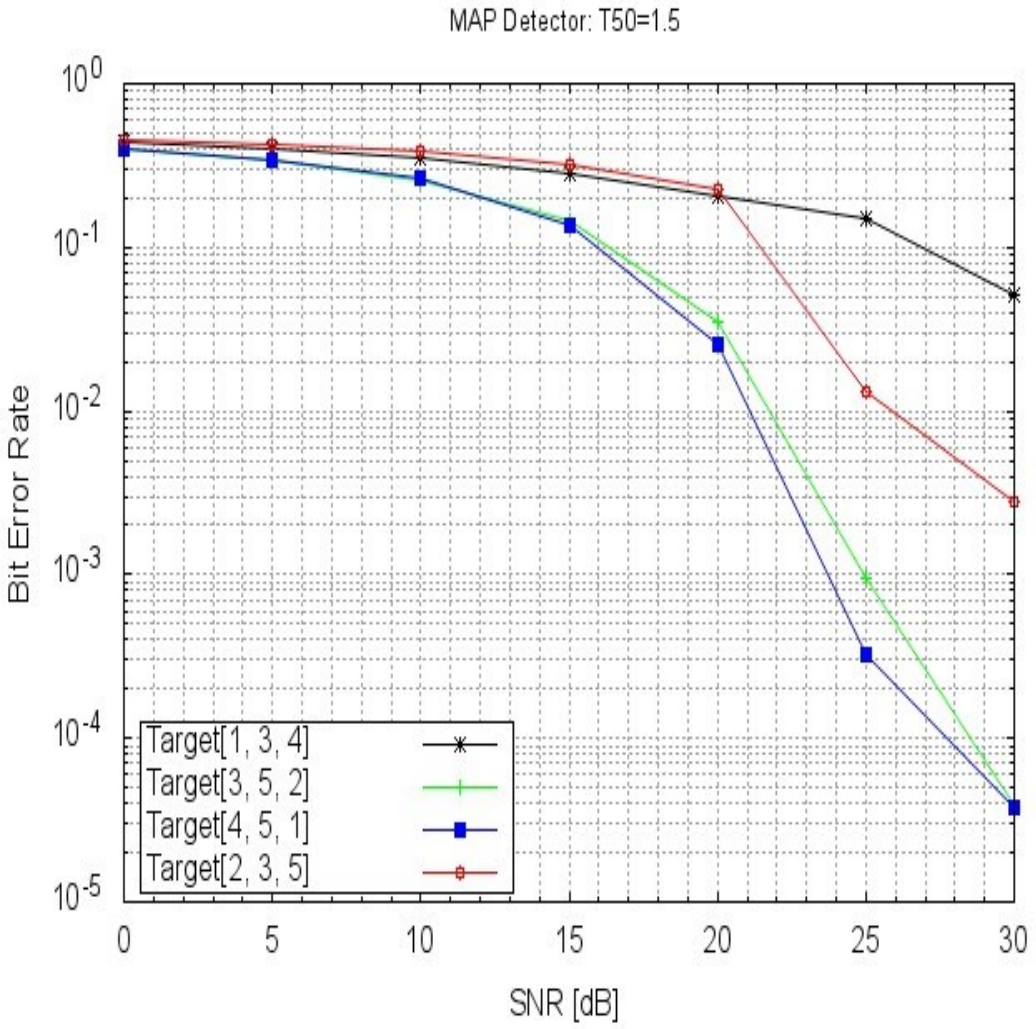


Figure 3.11: Comparison of non-symmetric GRP targets at $T_{50} = 1.5$.

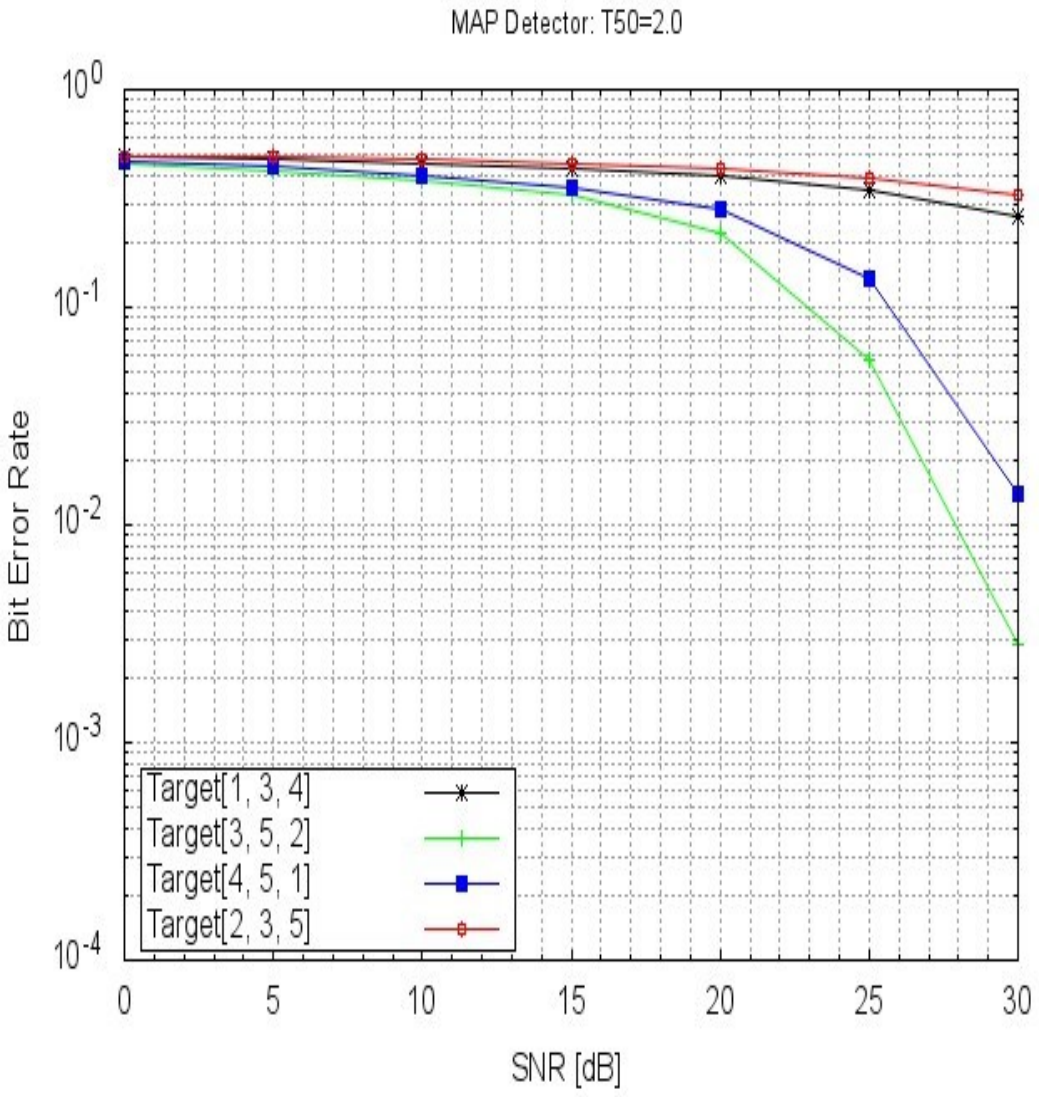


Figure 3.12: Comparison of non-symmetric GPR targets at $T_{50} = 2.0$.

However, as the SNR level increase beyond 24 dB, the performance of some non-symmetric GPR targets ([4, 5, 1], [2, 3, 5]) begins to floor. As compared to that of symmetric GPR targets at $T_{50} = 1.5$, which shows little or no error floor for all targets. Therefore, we conclude that for a PMR channel with our given conditions, symmetric targets are the preferred targets for achieving better results and performance.

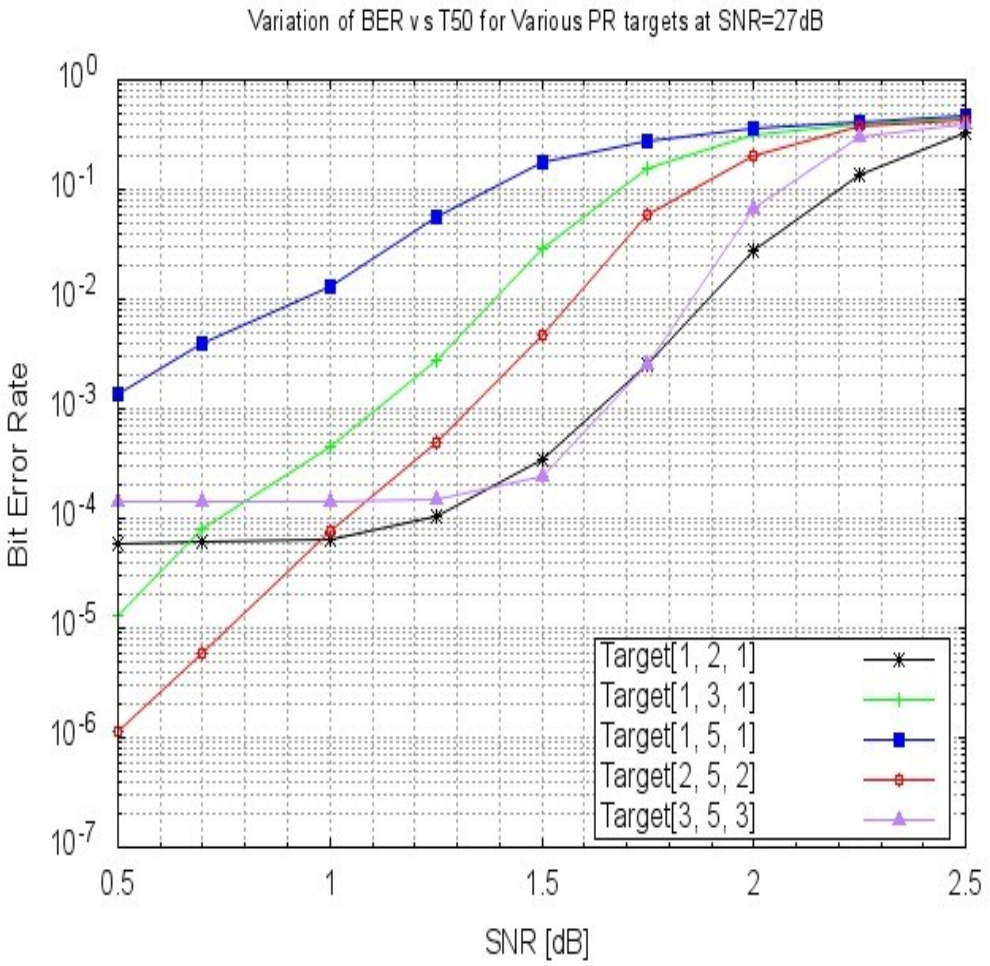


Figure 3.13: BER vs T_{50} performance of Symmetric GPR targets at SNR=27 dB

Figure 3.13 shows the T_{50} Vs BER performance of MAP detector for the PRML channel at an SNR of 27 dB. It shows the variation of BER with respect to changing data densities (T_{50}) along the track for different symmetric GPR targets. It is observed that different GPR targets exhibits certain individual behaviour at different T_{50} values. It is seen that at very low density ($T_{50} < 1$), target [2, 5, 2] has better performance in comparison to all the symmetric GPR targets tested so far. But at higher T_{50} regions (above 1.5 to 2.3), GPR target [1, 2, 1] outperformed all the other targets. There is a close match of performance between target [1, 2, 1] and target [3, 5, 3] at T_{50} range of 1.3-1.7, but the later becomes better as it exceeds this range. Generally, for all the GPR targets, it is seen that as the T_{50} increases, their performances begin to degrade and

becomes worse when high density values are reached. This is always as expected due to high interference at these regions. The best target is the one that is able to provide good symbol separation between the data symbols at high interference and also keeps the noise enhancement level minimum under such conditions at high SNR level. Therefore, based on these properties, GPR target [1, 2, 1] is considered as the best symmetric target for PRML channel based on the characteristic of our model under study.

Figure 3.14 and Figure 3.15 show the BER performance of detectors implemented using the VA algorithm and the BCJR algorithm at T_{50} values of 1.0 and 2.0 respectively. Based on the results as achieved, it is clear that the two algorithms have performances that are close to each other, although the BCJR has superior performance against the VA detector. The performance of the un-equalised system begins to improve at certain SNR values and later, deteriorates due to saturation of the jitter noise power present in the channel. This is because the PR equaliser is not able to fully utilize the jitter noise power unlike the detector which fully utilizes the jitter noise power in the detection process. The BCJR detector outperformed the VA detector with a gain of around 1.5 to 2.5 dB at BER point 10^{-3}. This is as expected because the BCJR algorithm is optimal in terms of minimizing the probability of bit error by taking into account bit by bit contribution in decoding the received data. The VA algorithm on the other hand is based on minimizing the probability of sequence error and considers only the entire sequence in decoding process.

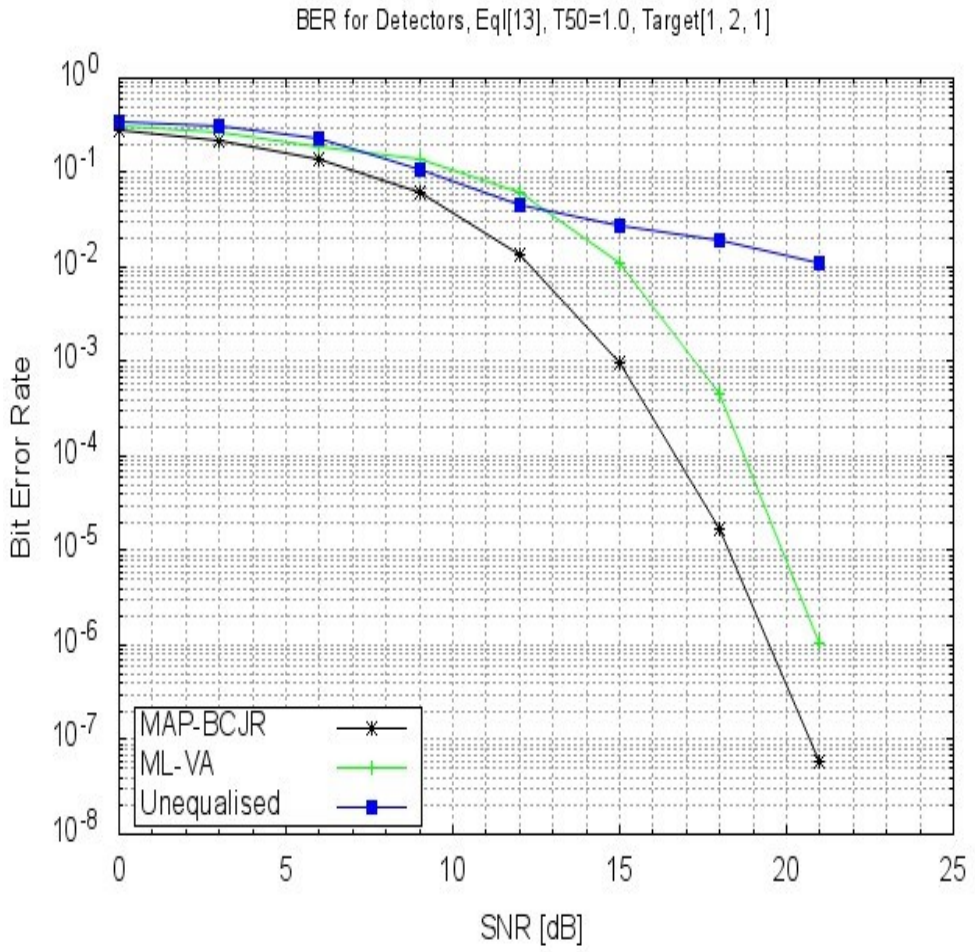


Figure 3.14: BER comparison of detectors at $T_{50} = 1.0$.

However, the VA detector has a better frame error rate (FER) performance as compared to the BCJR detector as it is seen in Figure. 3.16. The FER performance of the VA detector improves significantly with increase in the SNR level especially at higher dB values while for the BCJR detector there is no much significant improvement in the FER performance with increase SNR levels. This is also in accordance with existing literature, and it shows that the VA detector is optimal in terms of minimizing the probability of sequence error in the received data.

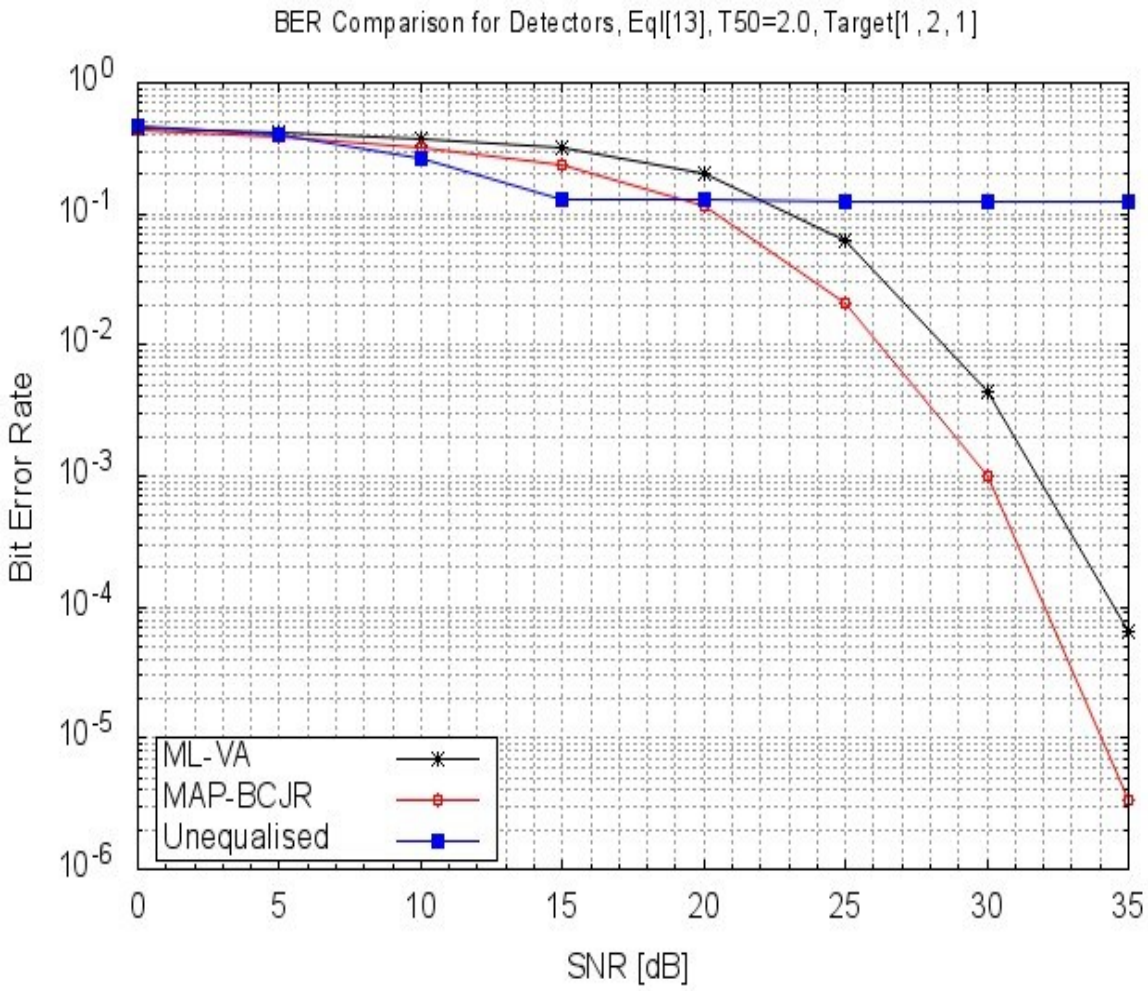


Figure 3.15: BER comparison of detectors at $T_{50} = 2.0$.

However, in terms of computational complexity comparison, the MAP decoder is more complex than the VA decoder. The complexity of the MAP decoder is about 3 times that of the VA decoder. This is because the MAP-BCJR decoder requires a separate calculation for forward recursion (α), backward recursion (β) and subsequently A-posteriori probability (APP) determination before a symbol is decoded. It also requires more memory and an extra latency is incurred in the process due to the fact that α, γ, and β, values need to be saved before APP is determined.

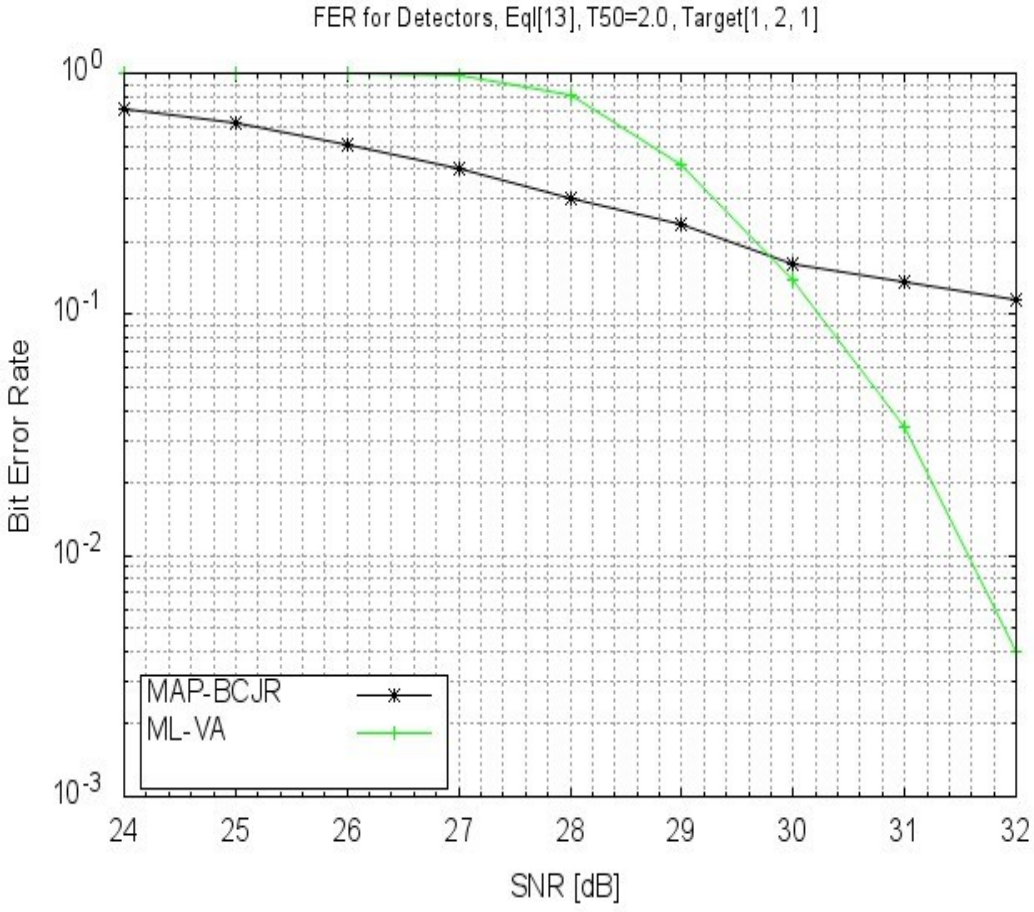


Figure 3.16: FER comparison of detectors at $T_{50} = 2.0$.

3.6 Summary

- Modelling and implementation of the PRML read channel system as a mechanism for data recovery from a PMR medium has been described and presented in this chapter.

- Modelling and implementation of the PMR channel using jitter noise model described in chapter 2 have been presented. This involves modelling the channel transition response using the hyperbolic tangent function and the timing jitter modelled as jitter noise represented by white Gaussian variable having zero mean and standard deviation of σ_j .

- PR equaliser with integer coefficients GPR target polynomial has been designed and implemented as part of the PRML implementation of the read channel. Target selection was carried out based on MMSE criterion to get the target with the best performance.

- A detailed description on the implementation of the ML detector using the VA and MAP detector using BCJR has been fully given. These detectors are used to extract the information record on the PMR media.

- The performances of the PMR channel using the PRML read system with both MAP and ML detectors have been simulated and analysed under various parameters and channel conditions.

- Various results have been presented for the PRML read system of the PMR media for different GPR targets, equaliser lengths and data density, with comparison of the results obtained.

Chapter 4

Decoding and Detection of PRML Channel Using Single Parity Coding

This chapter presents a novel joint detection decoding scheme for magnetic recording channel using interleaved parity-check coding and BCJR detection algorithm. The performance of the proposed scheme was verified by using it to extract information from a 1D PMR media with ISI. Investigation into the effect of using different interleaver configurations and decoding methods on the performance of the coded scheme are also presented. The joint detection decoding scheme based on interleaved parity coding and constrained MAP detector serves as the foundation for the work presented in chapter five. Parts of this chapter appear in the conference digest of the following conference: Almustapha Mohammed D., Abdulrazaq Muhammad B., Ahmed Mohammed Z., Marcel Ambroze A., & Davey Paul (2016, July). Decoding and detection for magnetic recording channel using single parity check coding. In *2016 Asia-Pacific magnetic recording conference* (*APMRC 2016*), IEEE conferences, pp. 56-57, July 13-15 2016, Korea.

4.1 Introduction

Advanced coding and signal processing techniques are essential tools towards increasing the areal density of magnetic recording channel beyond the convention limit. Coding combined with channel equalisation and signal detection mitigates the effect of ISI which is predominant in both 1D and 2D magnetic recording systems. However, for higher areal densities, coding and detection in magnetic storage becomes more complex due to high computational complexity caused by high order polynomial (Vasic and Kurtas, 2004). Highly efficient low complexity decoding, and detection algorithms are therefore needed.

Consequently, over the years, many researchers have proposed various techniques aimed at improving the efficiency of the decoding and detection algorithms. Among these techniques includes, the iterative decoding and detection scheme introduced by (Wu et al., 2003), and the joint self-iterating equalisation and decoding (Chen and Srinivasa, 2013). These techniques are based on the iterative decoding paradigm. However, the iterative algorithm is suboptimal because of the fact that it performance is highly dependent on the number of iterations performed.

Multi-track constrained codes for reducing the effect of ITI was proposed by (Davey et al., 1998) and (Ahmed et al., 2001). The unique design of these codes allows for only transition of the same polarity on adjacent tracks, thereby providing addition gain in the areal density. However, their implementation for high order polynomial results in a very high complex decoder design, and as such the codes were only suitable for two-track model implementation.

Conway (Conway, 1998) and (Cideciyan et al., 2001) presented a parity-based postprocessor scheme that detects, locates, and corrects the most dominant error events that occur at the output of the Viterbi detector. The scheme offers good performance with reasonable increase in

complexity (Cideciyan et al., 2001). Also, in (Elidirissi and Mathew, 2004) and (Vasic and Venkateswaran, 2004), a parity check code combined with time varying maximum-transition-run (MTR) code and parity constraints was proposed for improving the BER performance of PMR channel. Although, the postprocessor improves the performance of the Viterbi detector, it incurred additional complexity burden and introduces a decoding delay. This is due to fact that a list of the most dominant error events has to be maintained with their error type and location for the postprocessor operation.

In this chapter, a combined detection and decoding scheme based on single parity check-constraint with MAP detection of the BCJR algorithm is presented. The need for the postprocessor stage was eliminated by jointly performing decoding and detection on a single trellis. Additionally, to combat burst errors in the recording channel, a DRP interleaver (Crozier and Guinand, 2001) or Matrix interleaver was incorporated within the encoder before adding the second parity bit. Also, the performance of the coded system with different interleaver design configuration was investigated when the final parity bit decoding is designed based on either MAP or MLSD criterion. Finally, in this chapter a concatenated system employing both the Matrix and the DRP interleaver connected serially was presented.

4.2 System Model

Figure 4.1 depicts the block diagram of the system under study. Information data are generated in binary (0, 1) and encoded using single parity check coding. The coded data is then interleaved using DRP or Matrix/Square interleaver to provide good spreading of information and parity bits. Second parity bits are then added to the interleaved coded data before recording the data on PMR channel with jitter noise and AWGN.

The readback data is equalised using a PR equaliser and the result of the equalised data is passed to the MAP detector for joint detection and second parity bit decoding. Finally, the second parity bits are removed; the data bits are de-interleaved in order to restore their original bit positions. MAP or ML criterion is applied to decode the first parity bits and subsequently decision is made on the data.

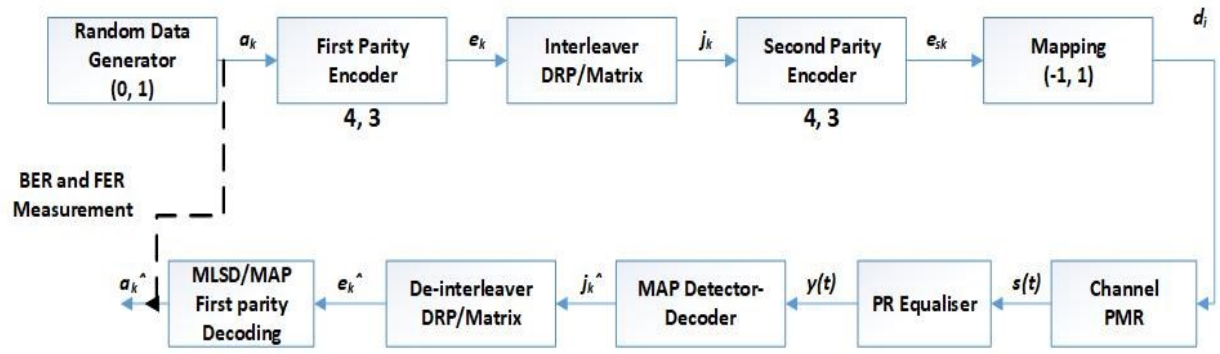


Figure. 4.1 System block diagram.

4.2.1 Data Encoding

The system model depicted in Figure 4.1 was implemented in the C-programming environment with a C-program code written by the author. The data to be recorded on the media are generated in binary (1, 0) using the C *rand()* function. A single parity bit is added to a small block of data to form a single parity check code. This helps to reduce the number of edges in the trellis needed for detection, and therefore limit the number of errors that may occur in the system. Two single parity check system separated by an interleaver in the form of either a DRP or a Matrix/Square interleaver, are used in this work.

The first single parity code adds a parity bit to a data block of 3 bits according to the even parity check constraint. This means, for each 3 consecutive data bits, a single parity bit is added to the data block, whose value is obtained by taking the exclusive or (xor) of the 3 consecutive bits. The result produced a code with a code length of 4 and a code rate of ¾. For example;

Let $a_k = \{s_0, s_1, s_2, s_3 \ldots\ldots\ldots s_{k-1}\}$ represent the sequence of data generated. The encoded data is given as; $e_k = \{s_0, s_1, s_2, p_0, s_3, s_4, s_5, p_1 \ldots\ldots\ldots s_{k-3}, s_{k-2}, s_{k-1}, p_{k-1}\}$. Where p represents the parity check bit and s represents the data bit. For the even parity check constraint, with four bits data sequence, the possible valid sequence combinations are; 0000, 0101, 0011, 1001, 1010, 1111, 0110, 1100. Consequently, based on the possible valid sequence combination the parity check bit p is evaluated using the expression:

$$p_0 = s_0 \oplus s_1 \oplus s_2 \tag{4.1}$$

For the first pair of the 3 consecutive bits sequence and the same also applied to all other data blocks of the bits sequences. The symbol $\oplus$ denotes the xor operation.

In our implementation, a total of 2304 data bit per track was initially generated before adding the first parity bits. After the first parity bits are added into the data bits according to the even parity check constraint using equation 4.1, the total data bits per track now becomes 3072 bits. An interleaver is then used to randomise the data bits positions so as to ensure good spreading of the data bits positions. The interleavers used in this work are discussed in the following sections.

4.2.2 DRP interleaver Implementation

After adding the first single parity bits, the data bits positions are randomised using DRP interleaver in this case. The DRP interleaver is implemented in three basic stages. The first stage called the read dither, involves randomising the bits positions locally using a small read dithered length R. For a given row vector of length L, if "i" is the position occupied by the bit in a row to be dithered ($i \leq L$), and "j" is the new position to which the bit is to be moved, then the relationship between "i" and "j", given L and R can be expressed as given by the equation 4.2.

$$j = R\lfloor i/R \rfloor + [(m + n*i) \bmod R] \tag{4.2}$$

Where "*m*" and "*n*" are integer constants less than *R*. *n* is chosen to be relative prime to *R*, while the "mod" denotes modulo division operation.

In our implementation, *R* is chosen as 8 to be 8-bit length while *L* is set as 3072 which is the total data bits per track after adding the first parity bits.

The second stage of the interleaver involves randomising the bit positions across the whole length of the data. This is done using a relative prime interleaving function. Equation 4.3 gives the expression for the function used to randomise the whole of the data in a row.

$$j = (m' + b'*i) \bmod L \tag{4.3}$$

where b' is a relative prime of and less than *L*. The same value for *L* is adopted as used previously in equation 4.3.

Finally, a local write dither of length *W* is used to randomise the bits positions locally similar to the read dither discussed above. The same dither length (*W*=8) of 8-bits is used as in the case of the read dither. Equation 4.4 gives the expression for the relationship between "*i*" and "*j*" for write dither.

$$j = W\lfloor i/W \rfloor + [(s + p*i) \bmod W] \tag{4.4}$$

Where "*s*" and "*p*" are also integer constants less than *W*. "*p*" is also chosen to be a relative prime to *W* and "mod" denotes modulo division.

The following practical example shows how the DRP interleaver can be implemented for a small length data sequence.

Let us consider the output of an encoder given as a sequence $e_k = \{s_0, s_1, s_2, p_0, s_3, s_4, s_5, p_1, s_6, s_7, s_8, p_2, s_9, s_{10}, s_{11}\}$. To implement DRP interleaving, first we do the local read dither permutation. From equation 4.2, since the vector sequence contains 15 elements $L=15$, choose $R=5$, $m=1$ and $n=3$. i is the index representing the bit position in the sequence. The read dither permutes the sequence changing the elements positions as follows;

Initial bits positions and values within the sequence before the read dither permutation;

Bit position	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Bit value	s_0	s_1	s_2	p_0	s_3	s_4	s_5	p_1	s_6	s_7	s_8	p_2	s_9	s_{10}	s_{11}

Bit positions and values within the sequence after the read dither permutation;

Bit position	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Bit value	s_1	s_3	s_2	s_0	p_0	s_5	s_7	p_1	s_4	s_6	p_2	s_{11}	s_9	s_8	s_{10}

The output from the read dither is then permuted using relative prime interleaving using equation 4.3. In this case we choose $m' = 7$, and $b' = 11$. Applying the relative prime interleaver permutes the bits positions as follows;

Bit position	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Bit value	p_1	s_0	s_{10}	p_2	s_7	s_2	s_8	s_6	s_5	s_3	s_9	s_4	p_0	s_1	s_{11}

After the relative prime interleaving, the resulting output sequence is then permuted locally with the small write dither using equation 4.4. W is set to 3, s is set to 1, and p is set to 5. The final interleaved coded sequence is given as follows:

Bit position	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*
Bit value	s_0	p_1	s_{10}	s_7	p_2	s_2	s_6	s_8	s_5	s_9	s_3	s_4	s_1	p_0	s_{11}

4.2.3 Matrix/Square interleaver Implementation

The Matrix/Square interleaver converts the whole row of the data into a matrix form consisting of certain number of rows and columns. Data is then read out column wise (that is one column at a time) to give the output of the interleaver. In our implementation, a row of 3072 bits of data representing the number of bits per track is converted into a matrix of 3 rows and 1024 columns. The data is then read column wise to give the output of the interleaver. A second single parity bit is then added for each of the columns three bits base on the odd parity check constraint. The following practical example shows how a Matrix/Square interleaver can be implemented.

Adopting the same encoded sequence output as used in the previous example for DRP interleaver, $e_k = \{s_0, s_1, s_2, p_0, s_3, s_4, s_5, p_1, s_6, s_7, s_8, p_2, s_9, s_{10}, s_{11}, p_3\}$ in the previous section, a matrix is formed to store the bits in the sequence as follows;

$$j_{mT} = \begin{bmatrix} s_0 & s_1 & s_2 & p_0 \\ s_3 & s_4 & s_5 & p_1 \\ s_6 & s_7 & s_8 & p_2 \\ s_9 & s_{10} & s_{11} & p_3 \end{bmatrix}$$

The interleaved coded sequence is now read across column as $e_{mT} = \{s_0, s_3, s_6, s_9, s_1, s_4, s_7, s_{10}, s_2, s_5, s_8, s_{11}, p_0, p_1, p_2, p_3\}$.

4.2.4 Second Parity Coding

After the interleaving process, a second parity bit is added to the data output of the interleaver. A single parity is added to a data block of length 3 again, but at this time using the odd parity check constraint. This is to ensure that, there are no streams of all ones or all zeros occurring

on a large number of bits in the data. The single parity code serves as a RLL (0, 6) modulation code for synchronisation purposes and also, as a FEC code during detection. This improves the performance of the detection process.

For a single parity bit on data block of length 3, based on the odd parity check constraint, the possible valid sequence combinations after the parity addition are; 0001, 0100, 0010, 0111, 1000, 1011, 1110, 1101. The parity bit p can be computed using the expression given by the equation 4.5.

$$p_0 = \overline{(s_0 \oplus s_1 \oplus s_2)} \tag{4.5}$$

where s_0, s_1, and s_2 are the data bits belonging to the small data block of length 3.

After adding all the parity bits to the data (that is first and second parity bits), the initial length of the data which was 2304 bits per track is now transformed into a length of 4096 bits per track. This gives the overall data length per track of data to be stored on the PMR media.

4.2.5 Channel

After preparing the data through first parity coding, interleaving, and subsequently, second parity addition, the data is then passed on the PMR media channel where the data is recorded. The PMR media channel is modelled using the jitter noise channel model previously discussed in Chapter 2. Modelling and implementation of the PMR media channel using the jitter noise channel model was already presented in Chapter 3. Therefore, the same approach for the channel is adopted for this system as presented earlier in the previous chapters without any modifications.

4.2.6 PR Equalisation

The readback signal from the PMR channel is equalised using a PR equaliser. In this implementation, a PR equaliser with a PR target length of 4 is used for equalisation. The choice for the target length 4 is due to the code length which is also 4, and to satisfy the code constraint which has a parity bit added to small blocks of data bits of length 3. Also, the target length 4 is needed to allow simultaneous detection and decoding of the parity bit from the equalised channel signal. The polynomial for the PR target is expressed as shown in equation 4.6.

$$T(D) = t_0 + t_1 D + t_2 D^2 + t_3 D^3 \tag{4.6}$$

Where D is the delay operator, and t_0, t_1, t_2, t_3 are non-zero coefficients that define the PR target.

A target column matrix is formed by padding zeros from both left and right side of the chosen target $[t_0, t_1, t_2, t_3]$ so as, to be of length equal to the number of modelling equaliser taps chosen. The channel response is also approximated in matrix form whose dimension is given according to the number of taps of the equaliser.

Equalisation is carried out by first, finding the coefficients of the equaliser that will shape the signal response to the desired target according to equation 3.16, and then, convolving this set of coefficients with the read signal from the PMR channel. The same methodology is followed in implementing the PR equalisation as described in the previous chapters 2 and 3. After equalisation, the output from the PR equaliser is passed to the MAP detector for simultaneous signal detection and second parity bit decoding.

4.2.7 MAP Detection and Second Parity Bit Decoding

The BCJR algorithm is used to simultaneously detect the signal and decode the second parity bit on the same trellis. This approach eliminates the need for the postprocessor stage utilised in (Elidirissi and Mathew, 2004) and (Vasic and Venkateswaran, 2004) thereby, reducing the complexity of the system thus, facilitating the ease of implementation. Since a target length of 4 was needed for PR equalisation in this scenario, a trellis with 8 states and 2 branches per state (total of 16 transitions) was employed. In this implementation, ITI across the tracks was not considered. The focus is mainly on a 1D PMR channel with severe ISI along the track. However, due to the nature of the code (code length 4), and the parity check constraint imposed by the code, the trellis is modified such that at the point where the odd parity bit comes into the equalised signal, the number of branch transitions reduced to 8 instead of 16, for the chosen target length 4. This is because only the branch transitions whose bit components satisfied the parity check constraint defined by the parity equation are possible. Figure 4.2 depicts the modified trellis structure for the odd single parity check code of length 4 and target length 4 used to simultaneously detect signal and decode the single parity bit in 1D PMR channel.

Now looking into the trellis of Figure 4.2, whenever the odd parity bit comes into the equalised signal, which corresponds to every fourth transition in the trellis, the valid transition from state [000] is to state [001]. This is because the bits component of the branch responsible for the transition is [0001] which satisfied the odd parity check constraint. Transition from state [000] to [000] is not valid because the bits component responsible for the transition [0000] does not satisfy the odd parity check constraint. The same checks applied to all states and their corresponding branch transitions. The joint detector/decoder is basically designed to select only the valid branch transitions that satisfied the odd parity check constraint imposed by the code whenever the parity bit entered the signal.

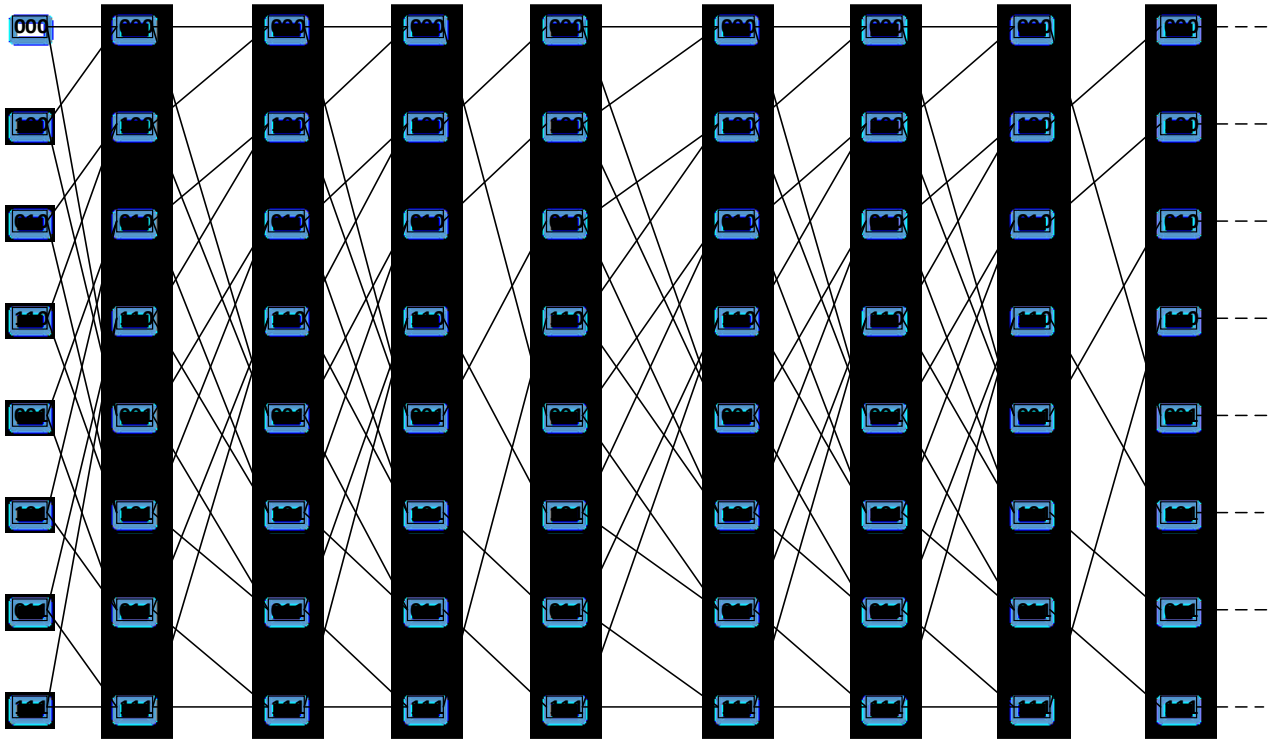


Figure 4.2: Modified trellis structure for joint detection decoding.

The BCJR algorithm was implemented using the same methodology adopted in the previous chapter 3. The only difference is the way in which the code constraint was handled, and some modification made in the branch transition probability computation to take into account the channel responses and shaping equaliser characteristics. The branch transition probabilities were compute using following expression in equation 4.7.

$$\gamma_k^{x_{k=i}}\left(s_{k-1}^n, s_k^n\right) = e\left(-\frac{x_k - y_n}{2\phi^2}\right)^2 \tag{4.7}$$

where x_k is the received symbol or bit at time t, y_n is the ideal symbol or bit at time t. ϕ^2 is the channel noise variance and is computed as:

$$\phi^2 = \sum_{i=-\infty}^{\infty} sh_i * \sum_{j=0}^{i} sh_j * \sigma_w^2 + \sum_{i=-\infty}^{\infty} h_i \sum_{j=0}^{i} sh_j * \sigma_j^2 \tag{4.8}$$

where *h* and *sh* are the channel response and shaping equalisers coefficients while σ_j and σ_w are the standard deviation of jitter noise and AWGN respectively.

After computing the branch transition probabilities for all states, the forward recursive probabilities (Alpha's (α)'s) for all states are determined recursively across the trellis section using equation 2.38, starting from the beginning to the tail end of the trellis. Similarly, the backward recursive probabilities (Beta's (β)'s) are computed recursively for all states across the trellis section using equation 2.39, starting from the trellis tail end backward till the beginning of the trellis. The values of the (α)'s and the (β)'s obtained are then used in conjunction with the branch probabilities, to determine the A-posteriori probabilities (APP)s of the received bits across the trellis section either 1 or 0 using equation 2.40. The values of the APP's give the soft output from the detector/decoder. This APP's are the saved in a register as history for further processing.

4.2.8 De-interleaving

Once all the APP values across each trellis section are computed, the detected data bits are now ready for the first parity check bit decoding. The decoding process start by first removing the decoded second parity check bits from the detected data. The history stored is then de-interleaved to restore the data bits back to their original positions. The de-interleaving process is done sequentially starting with the inverse write-dither, then the inverse RP interleaver and finally the inverse read-dither. That is, applying inverse operations of the three stages discussed in the interleaver design section (4.2.2) in case of the DRP scheme. Also, the same procedure is applied to the Matrix/Square interleaver. The de-interleaver is designed by selecting carefully different values of the integer constants that restored the original order of arrangement of the bits in all the cases. After de-interleaving, the final data output is obtained by MLSD decoding

or MAP decoding of the APPs using the possible valid data sequences to decode the first parity check bit, which appear at the last end of the valid sequence.

4.2.9 MAP Decoding of First Even Parity Check Bit

Under the even single parity check constraint, the possible allowable data sequences for four blocks of data considering the code length are, 0000, 0011, 0101, 0110, 1001, 1010, 1100, and 1111. Here the first three bits in the data sequence are taken as the information bits, while the last bit is taken as the even parity check bit. The APPs are therefore, arranged in a manner that satisfies the parity check constraint defined by the parity check equation. The probability of having each sequence pattern occurring is calculated by multiplying the APPs forming that particular sequence pattern. The MAP decoding is then implemented by finding the probability of each bit position within the valid data sequence given as either 1 or 0. Table 4.1 gives the probability of having each of the valid data sequences occurring in the data based on even single parity check.

After calculating the probability for each of the valid data sequence patterns as shown in table 4.2, the probability of each bit position for the information bits being either 1 or 0 is calculated and the fourth bit is discarded. Similar procedure is applied for all the four-bit block data combination until the last group of the data block is reached. The following example illustrates the process of determining the probability of each bit position.

Table 4.1 Probability of valid data sequence for even single parity check code

Possible pattern	APPs grouping	Prob. of pattern	Prob. Value
0000	APP[0]APP[0]APP[0]APP[0]	APP[0]×APP[0]×APP[0]×APP[0]	P_1
0011	APP[0]APP[0]APP[1]APP[1]	APP[0]×APP[0]×APP[1]×APP[1]	P_2
0101	APP[0]APP[1]APP[0]APP[1]	APP[0]×APP[1]×APP[0]×APP[1]	P_3
0110	APP[0]APP[1]APP[1]APP[0]	APP[0]×APP[1]×APP[1]×APP[0]	P_4
1001	APP[1]APP[0]APP[0]APP[1]	APP[1]×APP[0]×APP[0]×APP[1]	P_5
1010	APP[1]APP[0]APP[1]APP[0]	APP[1]×APP[0]×APP[1]×APP[0]	P_6
1100	APP[1]APP[1]APP[0]APP[0]	APP[1]×APP[1]×APP[0]×APP[0]	P_7
1111	APP[1]APP[1]APP[1]APP[1]	APP[1]×APP[1]×APP[1]×APP[1]	P_8

For bit position one i.e. probability of the first bit in sequence the pattern:

$$\textit{Probability of a one};\ P(1) = \frac{P_5 + P_6 + P_7 + P_8}{P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7 + P_8} = \frac{P_5 + P_6 + P_7 + P_8}{P_T}$$

$$P_T = P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7 + P_8$$

$$\textit{Probability of a zero};\ P(0) = \frac{P_1 + P_2 + P_3 + P_4}{P_T}$$

For bit position two i.e. probability of the second bit in the sequence pattern:

$$\textit{Probability of a one};\ P(1) = \frac{P_3 + P_4 + P_7 + P_8}{P_T}$$

Probability of a zero; $P(0) = \frac{P_1 + P_2 + P_5 +_6}{P_T}$

For bit position three i.e. probability of the third bit in the sequence pattern:

Probability of a one; $P(1) = \frac{P_2 + P_4 + P_6 + P_8}{P_T}$

Probability of a zero; $P(0) = \frac{P_1 + P_3 + P_5 + P_7}{P_T}$

These computed probabilities are then used to make decision on the information data, and hence yield the saved data.

4.2.10 MLSD Decoding of First Even Parity Check Bit

In the MLSD decoding implementation for the even single parity check code, the same procedure of grouping for the APPs according to the possible valid data sequence pattern is followed. After grouping and finding the probabilities for each of the valid data sequence pattern as illustrated in table 4.1, the probabilities are compared, and the data sequence pattern with the maximum probability is taken to represent the three information bits, while the fourth bit which is the parity is discarded. That is to say:

if((P1 > P2)&(P1 > P3)&(P1 > P4)&(P1 > P5)&(P1 > P6)&(P1 > P7)&(P1 > P8))

{Put first bit = 0, second bit = 0, and third bit = 0}

Else if((P2 > P3)&(P2 > P4)&(P2 > P5)&(P2 > P6)&(P2 > P7)&(P2 > P8))

{Put first bit = 0, second bit = 0, and third bit = 1}

Else if((P3 > P4)&(P3 > P5)&(P3 > P6)&(P3 > P7)&(P3 > P8))

{Put first bit = 0, second bit = 1, and third bit = 0}

Else if ($(P_4 > P_5)$ & $(P4 > P_6)$ & $(P_4 > P_7)$ & $(P_4 > P_8)$)

{Put first bit = 0, second bit = 1, and third bit = 1}

Else if ($(P_5 > P_6)$ & $(P_5 > P_7)$ & $(P_5 > P_8)$)

{Put first bit = 1, second bit = 0, and third bit = 0}

Else if ($(P_6 > P_7)$ & $(P_6 > P_8)$)

{Put first bit = 1, second bit = 0, and third = 1}

Else if ($(P_7 > P_8)$

{Put first bit = 1, second bit = 1, and third bit = 0}

Else {Put first bit = 1, second bit = 1, and third bit = 1}

The same procedure is repeated for all the four-block data combination within the whole data until the last block is received and decoded. The bits for the three information bits positions are now taken as the outputted saved data, while the fourth bit representing the parity check bit is discarded.

4.3 Concatenated Matrix/Square-DRP System Model

In a bid to improve the randomisation of data bit positions in the data together with the parity bits, a concatenated Matrix/Square and DRP interleaving scheme is developed. The scheme is aimed at achieving good data spread and bit separation, which randomises the local error burst locations. Three single parity bits are added to the original data bits to form the coded data. The

first and second parities are separated by a Matrix/Square interleaver while the second and third parities are separated by a DRP interleaver.

Figure 4.3 shows the system block diagram for the serially concatenated Matrix/Square and DRP interleaving detection scheme for a single parity check coded data. This system was developed and implemented in order to study and evaluate the performance of the PMR system using the concatenated interleaved single parity coding scheme.

The first parity encoder adds a parity bit to a data block of 4 bits this time around to produce a single parity code of length 5. An even parity-check constraint is imposed by the code to satisfy the parity check equation. That is to say, for each 4 consecutive data bits, a single parity bit is added to the block, whose value is computed by taking the xor of the 4 consecutive bits. This reduced the date rate to 4/5. Initially, a total of 2048 data bit per track was generated before adding the parity bit to each block of 4 consecutive bits. After adding the parity bits, the total number of data bits per track now becomes 2560 bits. A matrix/square interleaver algorithm is then applied to randomise the 2560 bits row of data per track.

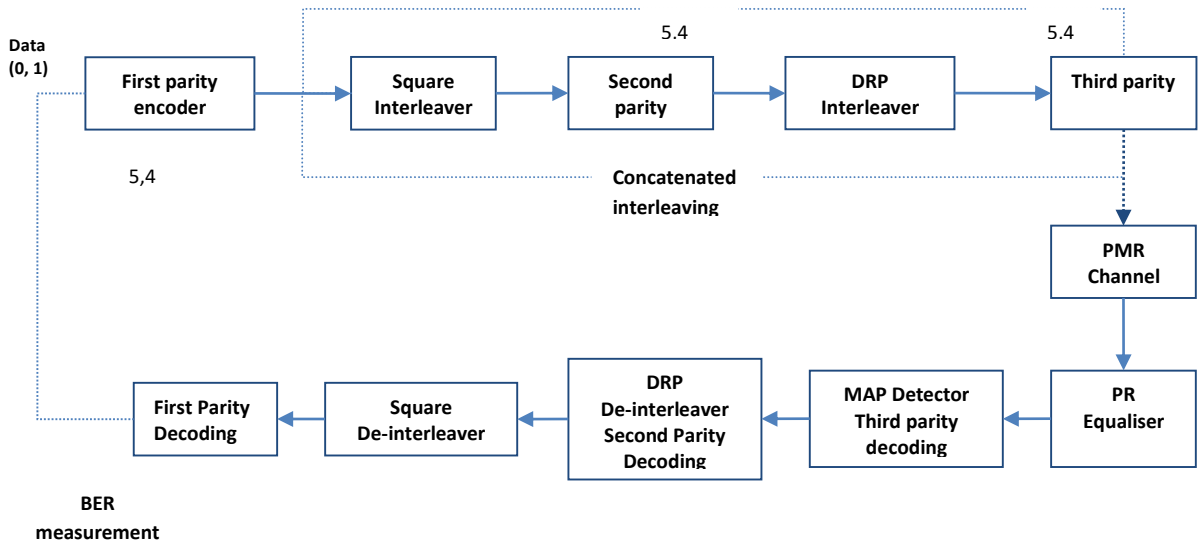


Figure 4.3: Block diagram for concatenated Square/Matrix-DRP interleaver system.

The Matrix/Square interleaver is implemented by first converting a row of 2560 bit representing the data bits per track into a matrix of 4 rows and 640 columns. The data is then read out column wise as the interleaved output. A second single parity bit is then added for each of the 4 column bits based on odd parity check constraint. This produced a total number of 3200 data bits per track. The row of 3200 data bits per track is then randomised again, but at this time with a DRP interleaver before adding the third parity checks bits.

The DRP interleaver is implemented by first dividing the row of data bits into smaller equal blocks and permute locally along the blocks using the read dither equation 4.2. Relative prime interleaving is the applied to randomise the data bits across the whole row length of the data according to equation 4.3. Finally, the row length is again divided into smaller block length and permuted locally across the lengths using the write dither equation 4.4. The procedure adopted is the same as described in the previous section, with the same value of integer constants utilised in section 4.2.2.

After interleaving, a third single parity bit is then added to the interleaved output of the DRP interleaver. Again, a single parity bit is added to each of 4 consecutive data bits block according to the odd parity check constraint. This amounts to a total of 4000 data bits per track that are to be stored on the PMR media. The same PMR media channel model was adopted as described above in the previous section.

Let the input to the second parity encoder be expressed as

$$v_s(i) = v_{in}(I_{sq}(i)) \tag{4.9}$$

where $I_{sq}(i)$ is the output obtained by reading out column wise data matrix 4×640 to produce a row data length and v_{in} is the output from the first parity encoder.

$$v_{sout}[5*i+4] = I_{sq}[5*i] \oplus I_{sq}[5*i+1] \oplus I_{sq}[5*i+2] \oplus I_{sq}[5*i+3] \oplus I_{sq}[5*i+4] \quad (4.10)$$

$v_{sout}(i)$ is the output of the second parity encoder. Therefore, the output of the combined concatenated Matrix/Square-DRP interleaver scheme is expressed as;

$$v_{sq-drp}(i) = v_{in}(I(i)) \quad (4.11)$$

where the interleaving system is completely defined by

$$I(i) = v_{sout}(I_{drp}(i)) \quad (4.12)$$

and,
$$I_{drp}(i) = I_r(I_{rp}(I_w(i))) \quad (4.13)$$

where I_r, I_{rp} and I_w are the read dithered, relative prime and write dithered interleaving functions of the DRP interleaver respectively. These are computed using equations 4.2, 4.3 and 4.4 respectively.

A PR equaliser with a target length 5 is used to equalise the readback signal from the channel output. The choice of target length 5 is due to the code length which is also 5, and to allow simultaneous signal detection and parity bit decoding on the same trellis using the BCJR algorithm. This also enables the MAP detector to satisfy the code constraint imposed by the parity check equation. Therefore, a PR target polynomial of the form given by equation 4.9 was employed.

$$T(D) = t_0 + t_1 D + t_2 D^2 + t_3 D^3 + t_4 D^4 \quad (4.14)$$

Where the parameters in the equation have the same definition given in equation 4.6

The channel readback signal is equalised to the desired signal response determined by the PR target $[t_0,\ t_1,\ t_2,\ t_3,\ t_4]$. The same procedure is followed for the equalisation process as described in the previous section for target length 4.

After equalisation, the equalised signal from the equaliser output is now ready for joint signal detection and third parity decoding. Since a target length 5 is used for the PR equaliser, the constraint length of the detector now becomes (*Target Length* – 1) which is 4. For a 1D signal, a trellis with 16 ($2^{1\times4}$) states and total of 32 (2×2^4) branch transition is needed for detection. However, due to the code constraint, the trellis is modified in such a way that whenever the third parity bit comes into the equalised signal, the total number of branch transition is reduced to 16 instead of 32. This is to allow only the branch transitions whose transition bits component satisfied the parity check equation. That is to say, at every fifth transition in the trellis, the valid bits component for branch transitions are; 00001, 00100, 01000, 00111, 01110, 01011, 01101, 00010, 10000, 10011, 11010, 10101, 11100, 11001, 10110, 11111. Only the branches with these bits component would be selected by the detector. The BCJR algorithm is used to simultaneously detect the signal and decode the third parity bits. The same methodology was adopted in determining the APP of the received data bits as described in section 4.2.7.

Once all the APPs across the whole trellis section are determined and saved in a register, the decoded third parity bits are then removed from the saved data. The data bits are then de-interleaved using the DRP de-interleaving function to restore the data bits positions. The same DRP de-interleaving process was followed as described in the previous section. The second parity bits are then decoded using the MAP-decoding criterion described above in section 4.2.9. Here, the data is divided is divided into 5 bits block length according to the parity check constraint. The first four bits represents the information bits and last bit is taken as the parity check bit. The probability of each valid data sequence is determined first, and then the

probability of each bit position in the data sequence given as 1 or 0 is determined. The same procedure is followed as in section 4.2.9 to decode the second parity bit. After all the data blocks are decoded, the second parity bits in the data are removed.

Matrix/Square de-interleaving algorithm is the applied to the remaining data to restore the original arrangement of the bits positions in the data. Then finally, the first parity bits are decoded to get the output of the saved data. The decoding is also done using the MAP-decoding criterion. The decoded first parity bits are the removed from the data and final decision is taken to give the saved data.

4.4 Results and Discussion

In this section, we are going to present the performance of the single parity-check coding scheme in the PMR media system. An equaliser target length 4 is used throughout for the joint signal detection and decoding of the single parity check-code. We used the MAP algorithm to perform joint signal detection and single parity bit decoding simultaneously in order to prove the performance of the detector. The performance of the PRML system with and without the single parity-check coding was first investigated, and the results obtained in both cases are compared and analysed.

As mentioned earlier in chapter 3, target selection is very important in analysing the performance of the ML detector. So therefore, in order to make sure that we based our analysis using the best possible result, we explore different options of the GPR targets of length 4. The performance of the MAP detector using various GPR targets under different channel conditions was determined through simulations in order to select the best target for the detector. This is necessary even before incorporating the coding scheme into the system in order to ensure that the code performance is analysed using the best result for the detector.

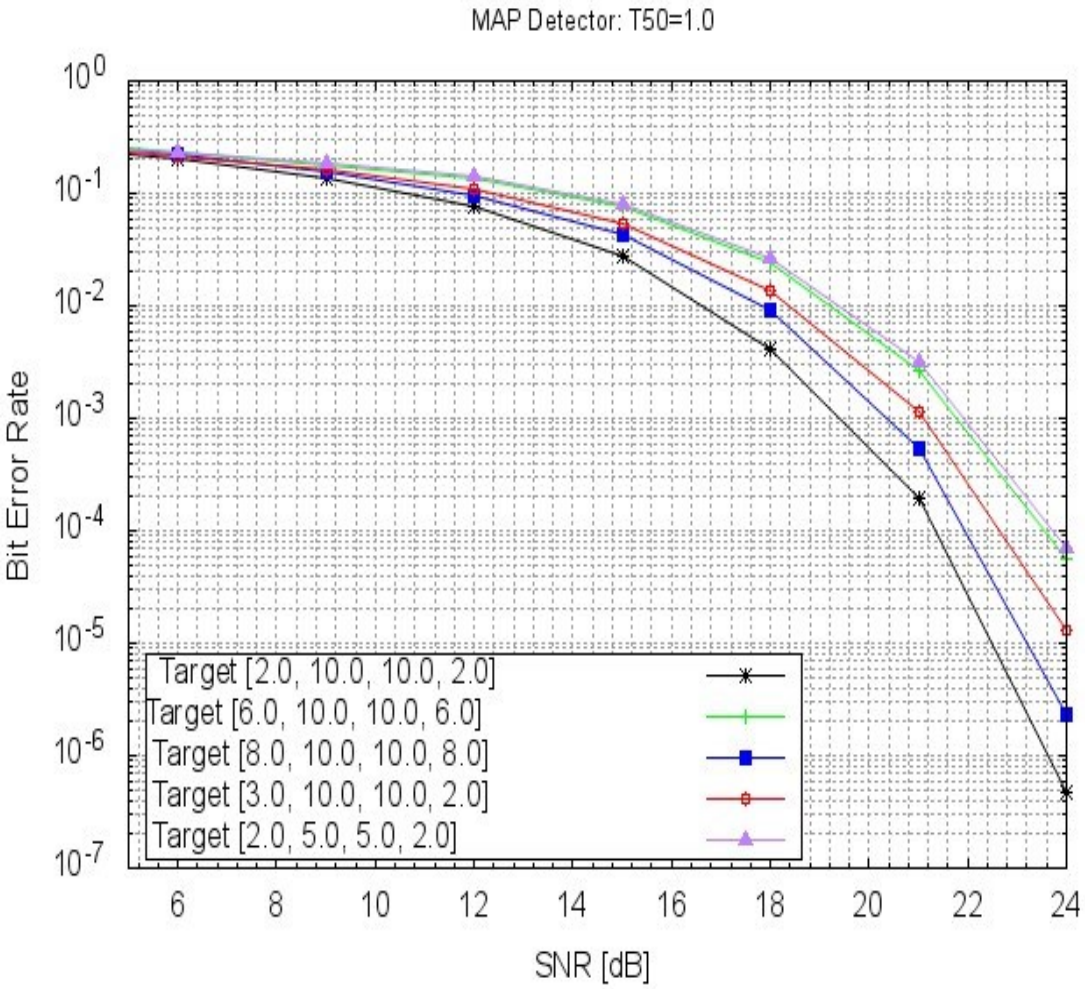


Figure 4.4: Performance of MAP detector with symmetric targets at $T_{50} = 1.0$.

Figure 4.4 shows the performance of the MAP detector with symmetric GPR targets of length 4 under a channel condition of low data density along the track ($T_{50} = 1.0$). As it can be seen from the figure, the target [2.0, 10.0, 10.0, 2.0] has the best performance at low ISI ($T_{50} = 1.0$) condition compared to the rest of the GPR symmetric targets. Targets [6.0, 10.0, 10.0, 6.0] and [2.0, 5.0, 5.0, 2.0] have the worst performances of under this channel condition. Target [2.0, 10.0, 10.0, 2.0] has a gain of about 3dB over target [6.0, 10.0, 10.0, 6.0] and target [2.0, 5.0, 5.0, 2.0]. But as the ISI increases, the performance shows that the target [3.0, 10.0, 10.0, 3] outperformed the rest of the targets having the best performance of all, which is the followed by the target [2.0, 5.0, 5.0, 2.0].

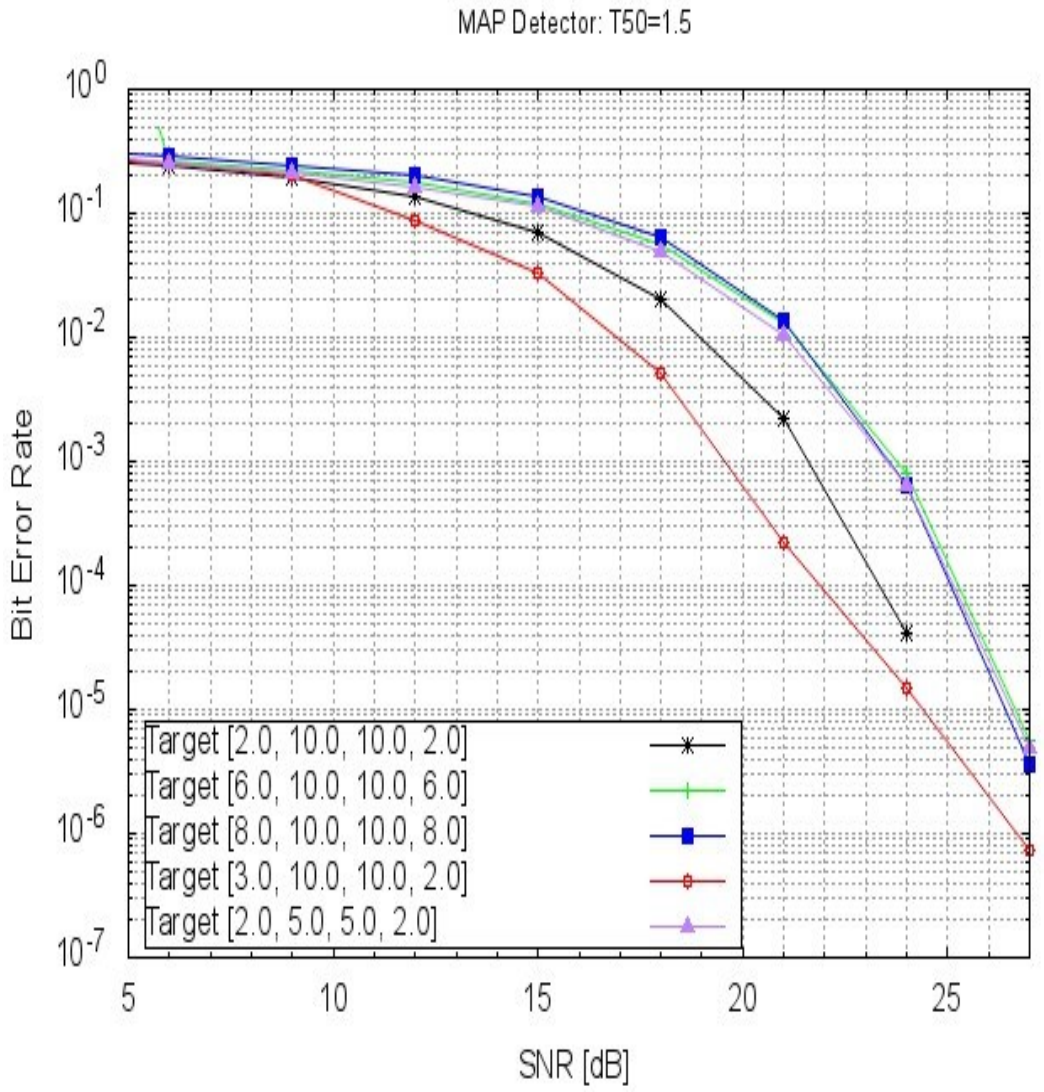


Figure 4.5: Performance of MAP detector with symmetric targets at $T_{50} = 1.5$.

The performance of the BCJR-MAP detector with the symmetric GPR targets at $T_{50} = 1.5$ is shown in Figure 4.5. At BER point10^{-3}, target [3.0, 10.0, 10.0, 3.0] has a gain of about 2.5dB over target [2.0, 10.0, 10.0, 2.0] and almost 4.5dB compared to other targets.

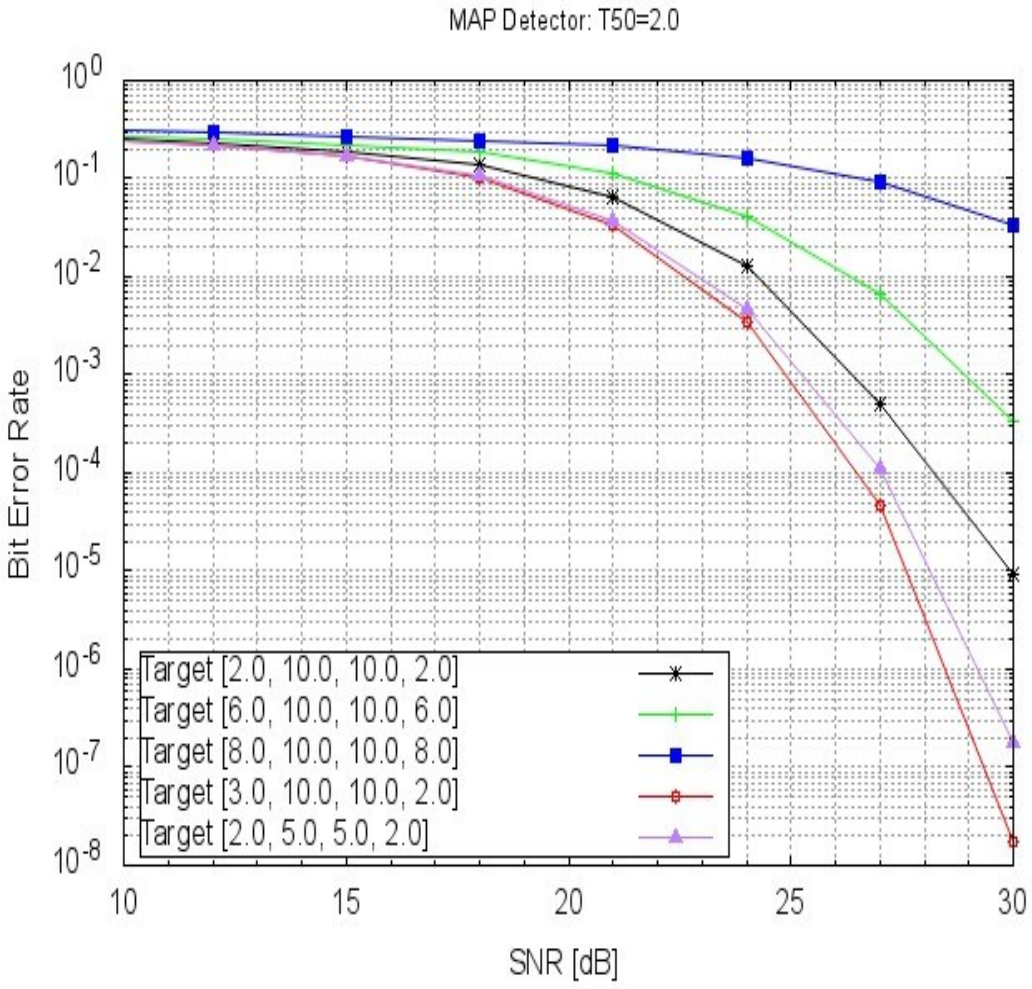


Figure 4.6: Performance of MAP detector with symmetric targets at $T_{50} = 2.0$.

However, at high ISI ($T_{50} = 2.0$), see Figure 4.6. The target [2.0, 5.0, 5.0, 2.0] shows an improvement in performance compared to other targets. The performance closely matched that of the target [3.0, 10.0, 10.0, 3.0] which have the best performance of all the targets. This means that for target length 4, target [2.0, 5.0, 5.0, 2.0] is best suited for channel conditions of high ISI ($T_{50} > 1.5$) than low ISI channel condition. Therefore, for high density recording applications such as in our channel of interest, both target [3.0, 10.0, 10.0, 3.0] and target [2.0, 5.0, 5.0, 2.0] can be used for better performance gain.

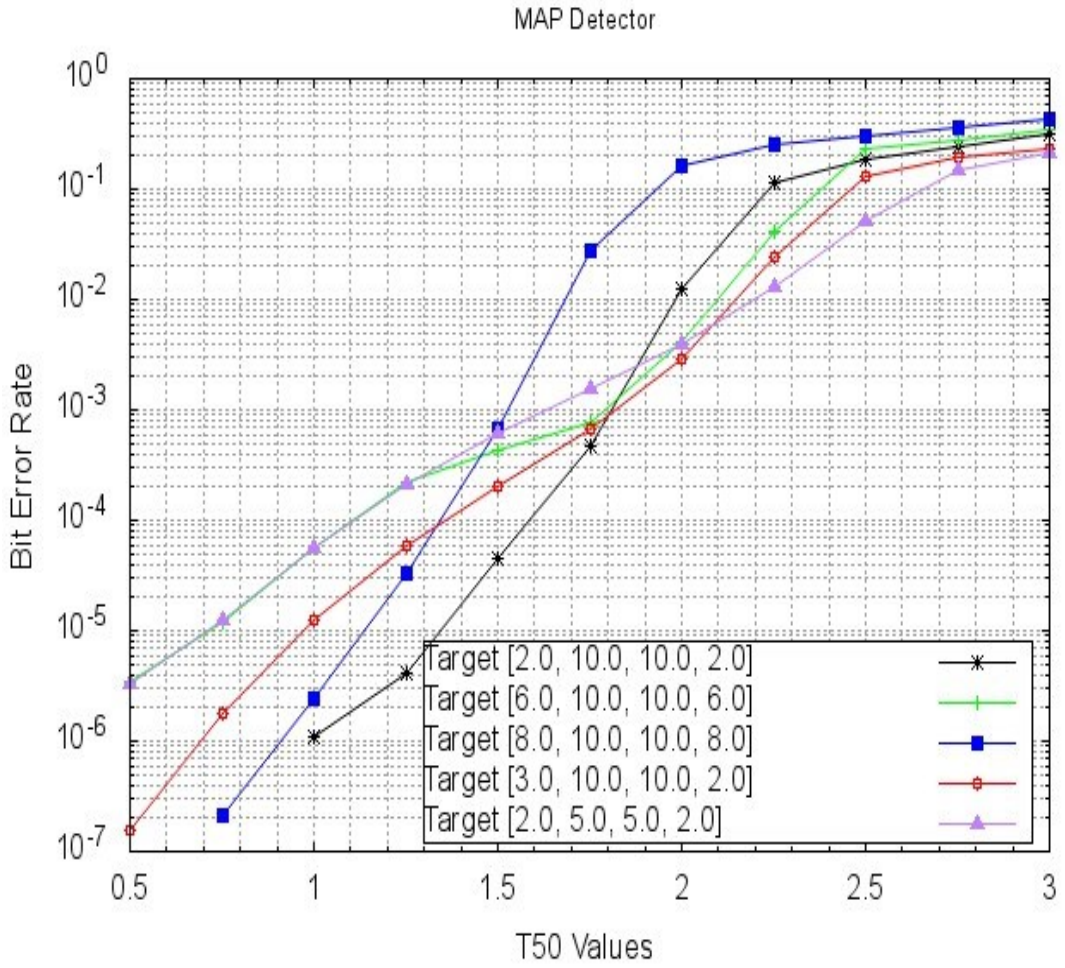


Figure 4.7: BER vs T_{50} performance of symmetric GPR target of length 4 at SNR=27 dB

Figure 4.7 shows the performance of the symmetric GPR targets of length 4 when the density values (T_{50}) are varied at a constant SNR value. It shows the variation of BER with respect to changing T_{50} values for the different targets. It is seen that at high ISI along-track $T_{50} \geq 2.0$, target [2.0, 5.0, 5.0, 2.0] has the best error performance of all target followed by target [3.0, 10.0, 10.0, 3.0]. Target [8.0, 10.0, 10.0, 8.0] has the worst performance of all targets at $T_{50} \geq 1.5$. Therefore, target [2.0, 5.0, 5.0, 2.0] is well suited for high density recording channel with severe ISI due its ability to have good symbol separation between the interfering bit symbols. It will give good result even when the interference in the channel is severe.

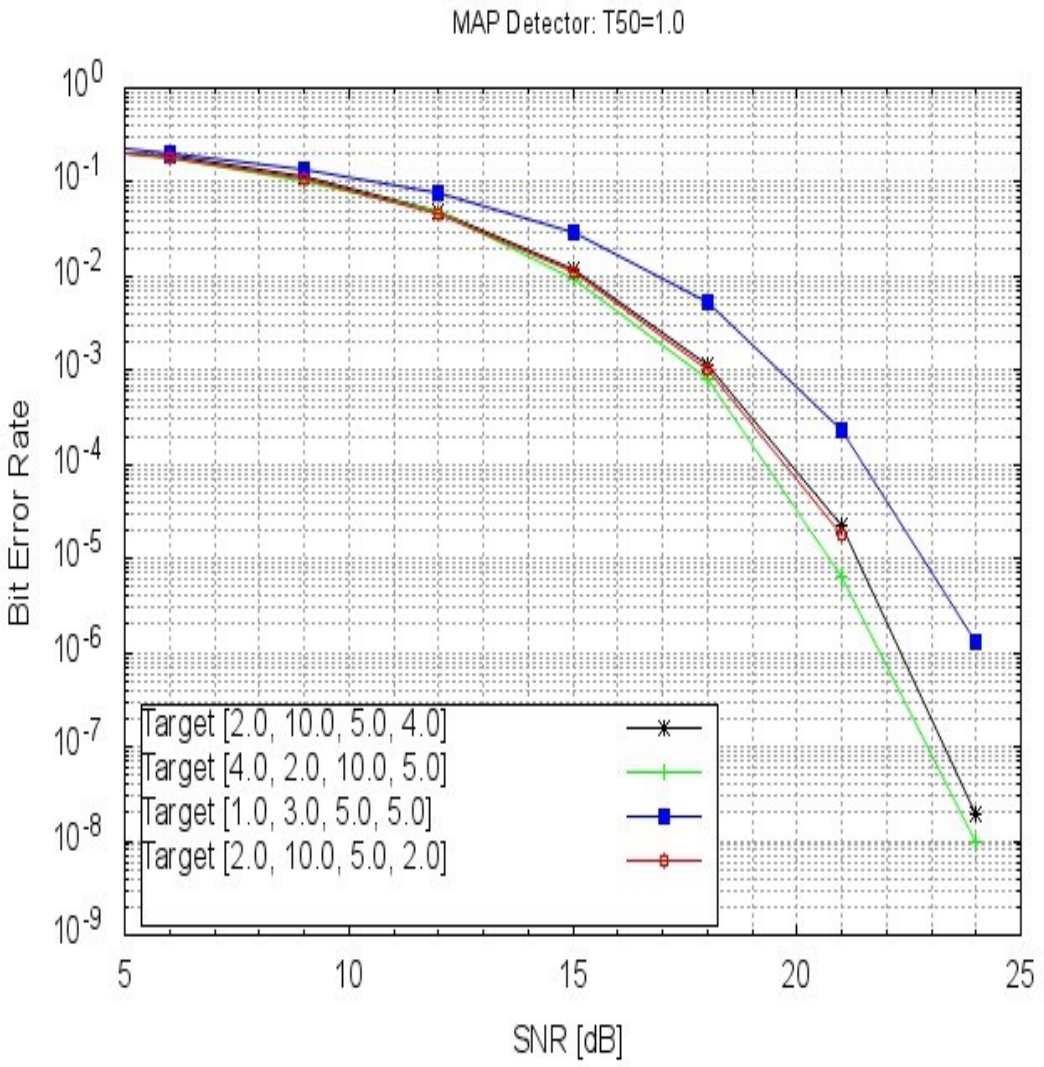


Figure 4.8: BER performance of non-symmetric GPR target of length 4 at $T_{50} = 1.0$.

Similarly, Figures 4.8, 4.9 and 4.10 show the performance of non-symmetric GRP targets for target length 4 at densities of $T_{50} = 1.0$, $T_{50} = 1.5$, and $T_{50} = 2.0$ respectively.

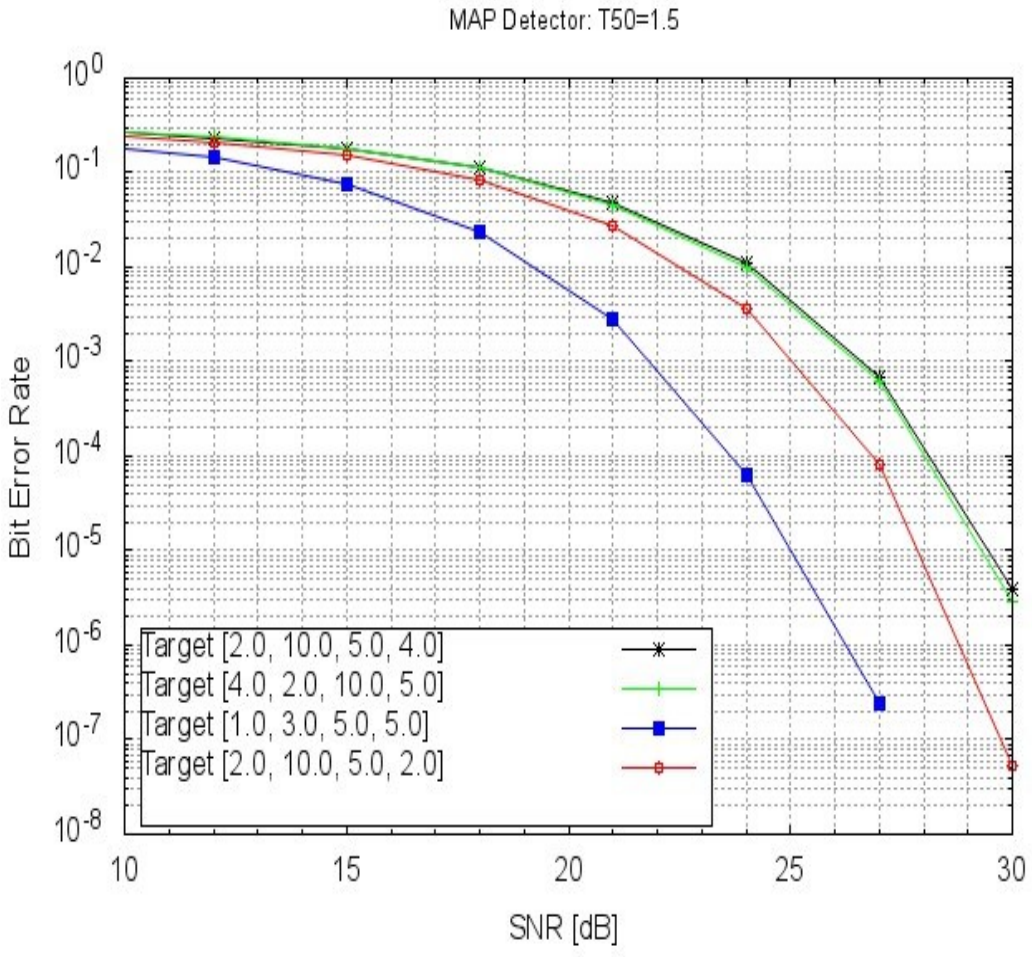


Figure 4.9: BER performance of non-symmetric GPR target of length 4 at $T_{50} = 1.5$.

There is a close match in the performances of the target [2.0, 10.0, 5.0, 4.0], target [2.0, 10.0, 5.0, 3.0] and target [4.0, 2.0, 10.0, 5.0] at $T_{50} = 1.0$ as shown in Figure 4.8. The target [1.0, 3.0, 5.0, 2.0] has the worst performance of all the non- symmetric GPR targets.

However, as the ISI increases, which corresponds to a more case of extreme interferences in the channel (that is to say $T_{50} \geq 1.5$), the target [1.0, 3.0, 5.0, 2.0] has a gain of about 3dB over [2.0, 10.0, 5.0, 3.0] and much higher gains over the other non-symmetric GRP targets at $T_{50} = 1.5$ (see Figure 4.9).

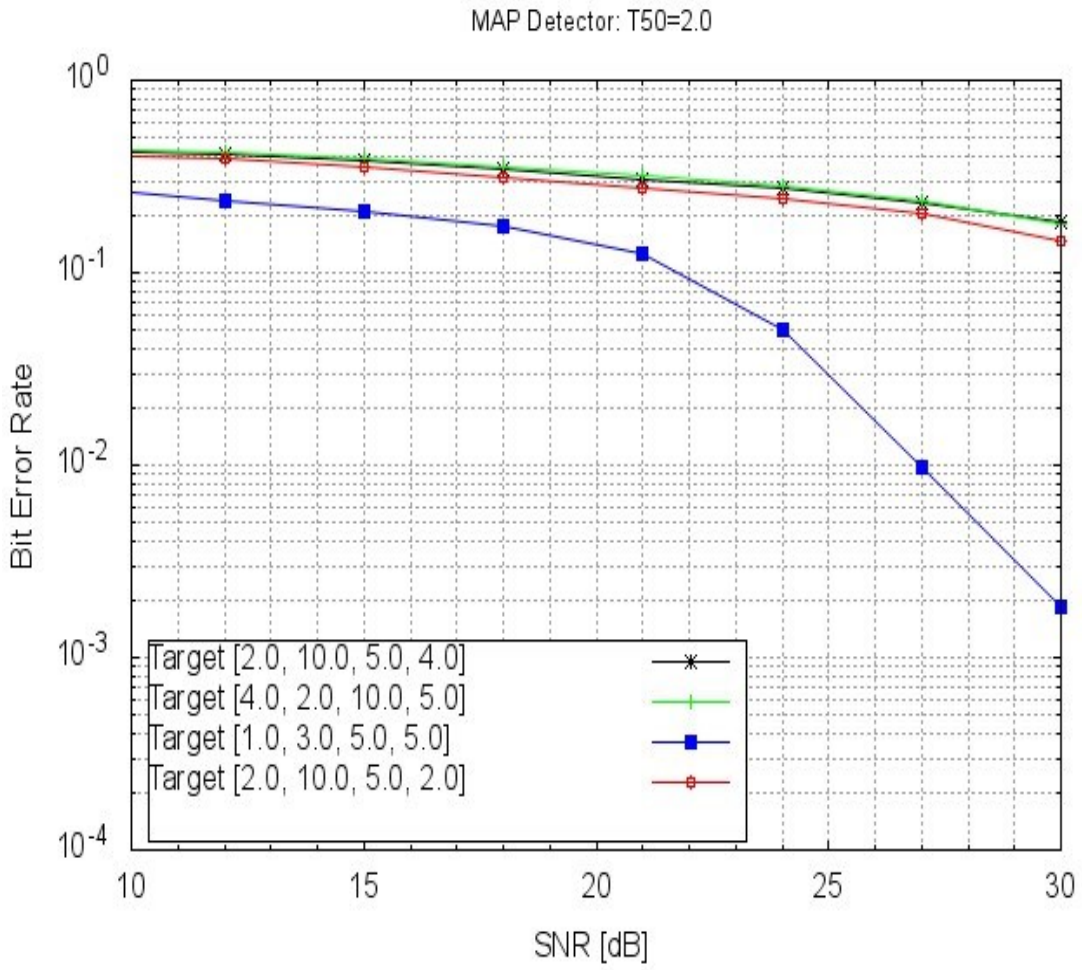


Figure 4.10: BER performance of non-symmetric GPR target of length 4 at $T_{50} = 2.0$.

The gain is more observed at $T_{50} = 2.0$ where the target [1.0, 3.0, 5.0, 2.0] significantly outperformed all other non-symmetric targets with very high margin (see Figure 4.10).

However, in comparison to symmetric targets presented before, the non-symmetric targets have inferior performances at extreme channel conditions when the ISI is high. This is evident as depicted by Figure 4.11 where the best symmetric targets are compared with the best performing non-symmetric target at $T_{50} = 2.0$ (high data density). The symmetric targets outperformed the non-symmetric due to the fact that the former produces minimum noise amplification level at high channel density than the latter. Therefore, symmetric targets will be

considered for the next analysis of the single parity coding scheme throughout the rest of this report unless it is otherwise stated.

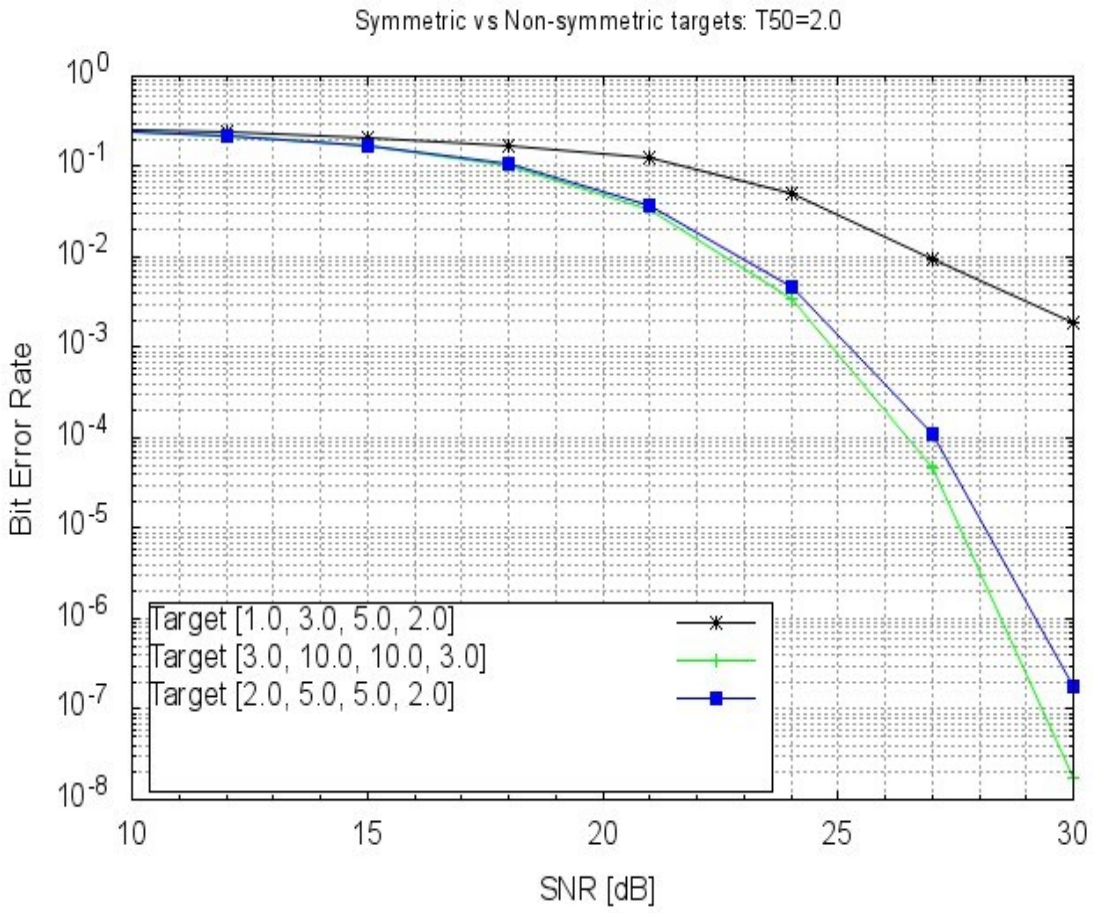


Figure 4.11: Performance comparison of best symmetric vs best non-symmetric target.

After analysing the performance of the MAP detector for the PRML read channel and selecting the desired target, the forward error correction (FEC) scheme is now introduced into the system. The FEC coding was implemented as described above in the beginning of this chapter using the single parity-check constraint. Two parity bits separated by an interleaver are applied to a data length of 2304 bit per track to produce a total of 4096 bits per track after all the parity bits are added. This reduced the data rate of the system to $\left(\frac{3}{4} \times \frac{3}{4} = \frac{9}{16}\right)$ after coding.

The MAP detector is utilised to handle the parity check constraint, while at the same time performing data detection. This decodes the second parity bits, and the APPs produced are de-interleaved after removing the second parity bits. The APPs are then subsequently passed to another decoder for first parity bits decoding to obtain the final data output.

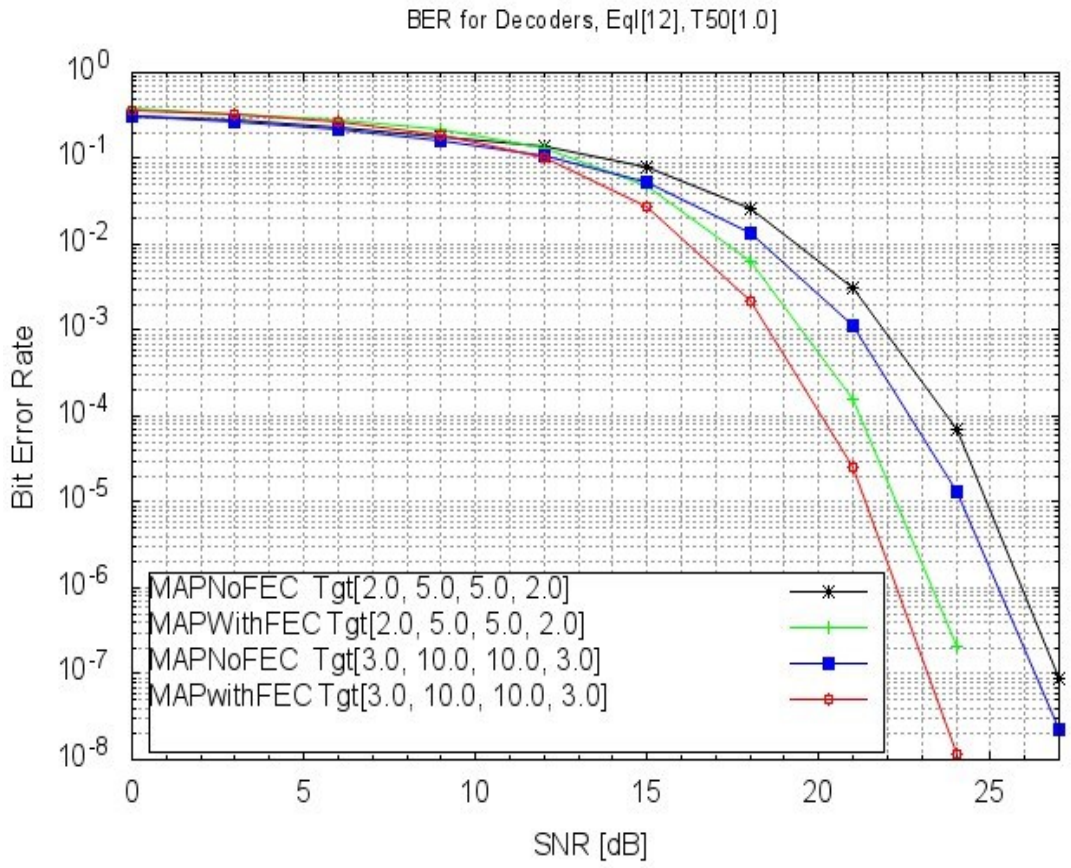


Figure 4.12: Performance of the detector with FEC and without FEC at $T_{50} = 1.0$.

Figure 4.12 shows the performances of the two selected targets of length 4 for the coded system with FEC coding and with an interleaver separating the parity bits. It is seen that at $T_{50} = 1.0$, similar performance for both targets [2.0. 5.0, 5.0, 2.0] and [3.0, 10.0, 10.0, 3.0] is recorded with target [3.0, 10.0, 10.0, 3.0] having a gain of around 1dB over target [2.0, 5.0, 5.0, 2.0]. There is a gain of about 3dB with the coded system (MAP with FEC) over the uncoded system (MAP without FEC) at $T_{50} = 1.0$ with both targets. This justifies the use of the single

parity check code and the interleaver as an error control mechanism to improve the performance of the PRML read channel. The performance gain due to FEC system can be explained in two folds; first is due to the code constraint, the number of edges in the trellis are reduced during detection which minimize the space of possible errors to be made during detection. The second factor is the interleaver which prevents the localisation of errors in a given position, and also provides adequate separation between symbols within the data.

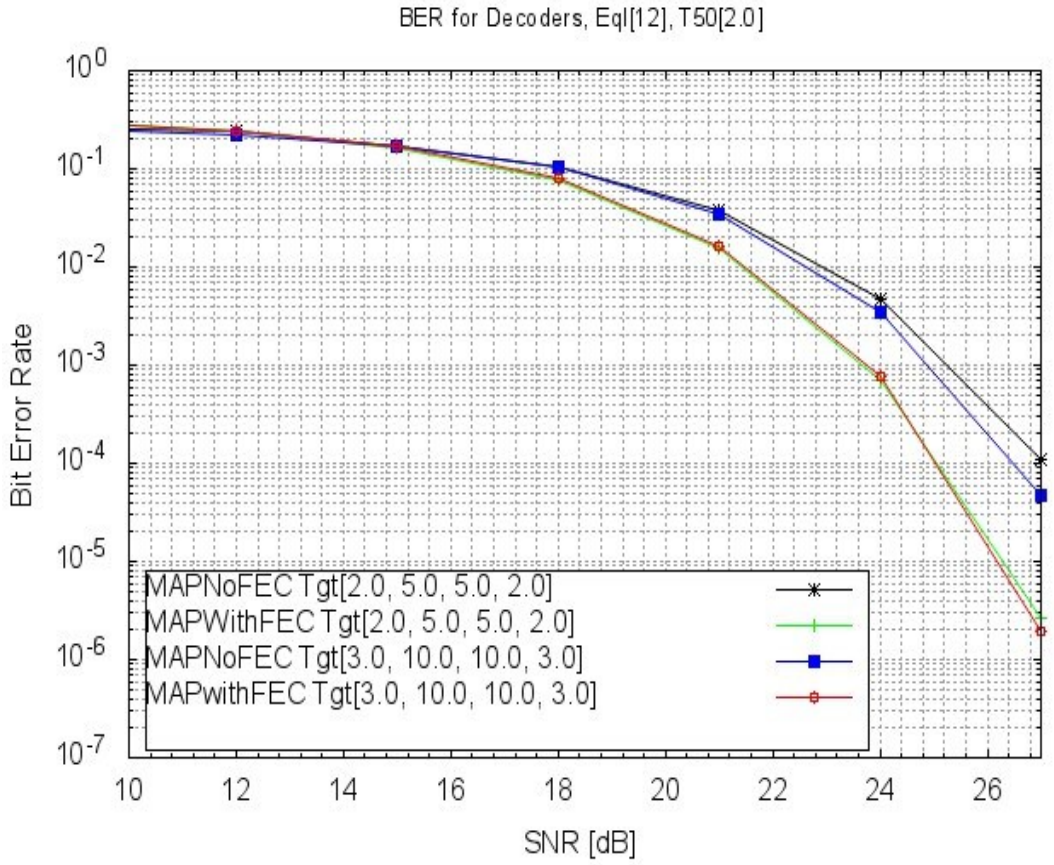


Figure 4.13: BER performance of the detector with FEC and without FEC at $T_{50} = 2.0$.

Figure 4.13 shows the performance of the coded system (with FEC and interleaver) and the uncoded system (without FEC and interleaver) for both targets at high ISI ($T_{50} = 2.0$). It shows a match in performance for both targets at high density along the track for the coded system.

There is also a gain of about 2.5 dB for the coded system in comparison to the system without FEC and the interleaver at BER point 10^{-4}.

In order to further our system study to establish good result, we analyse the performance of the coded system when different interleaving and decoding approaches are applied to the coded data. The performance of coded system with DRP and Matrix/Square interleaver was compared when first parity bit decoding is performed using both MLSD and MAP decoding techniques.

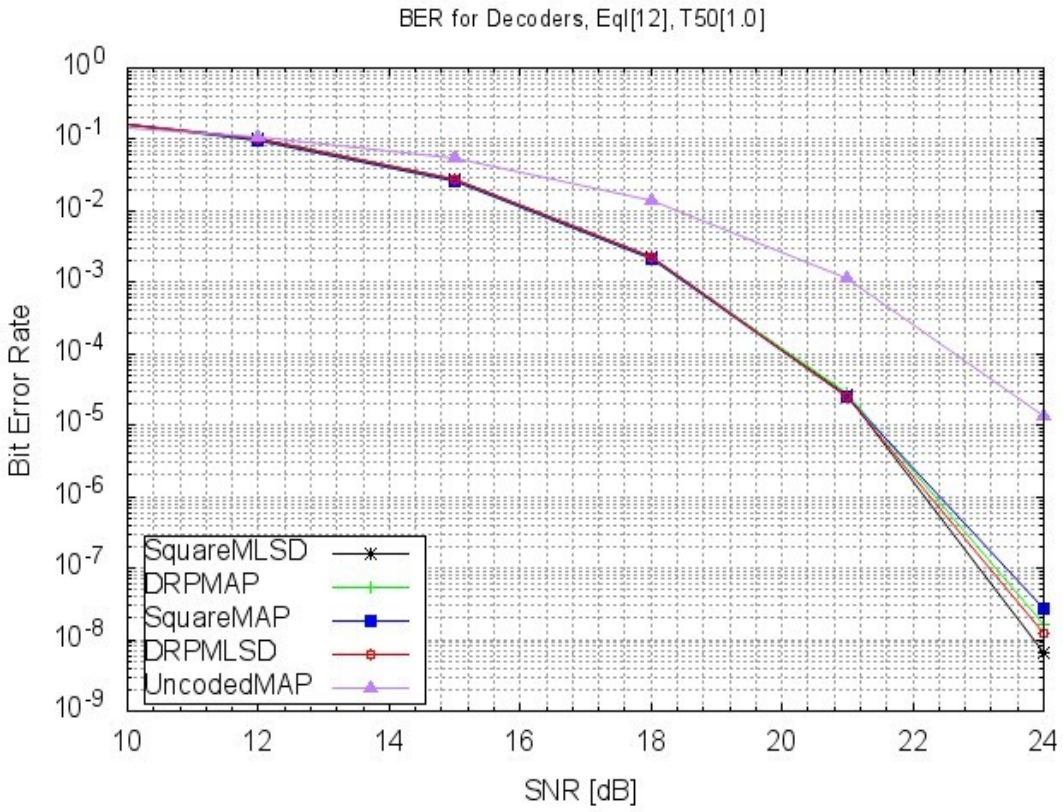


Figure 4.14: BER performance of decoders at $T_{50} = 1.0$.

Figure 4.14 shows the BER performance of the decoders under study for channel at T_{50}=1.0, an equaliser length 12 and target [3.0, 10.0, 10.0, 3.0]. T_{50}=1.0 represents a low ISI channel scenario. The plot '*UncodedBCJR*' means that neither single parity code nor an interleaver is applied to the user data. '*DRPMAP*' and '*DRPMLSD*' represents a situation where single parity encoding and DRP interleaver is applied to the user data with MAP and MLSD decoding

respectively. Likewise, the plot 'S*quareMAP*' and '*SqMLSD*' represents the scenario where, single parity encoding and Matrix/Square interleaver is applied to the user data with MAP and MLSD decoding respectively. The figure shows similar performance for all the schemes employing the single parity-check coding and interleaving, with the square-MLSD, performing a little better than all the rest at $T_{50} = 1.0$.

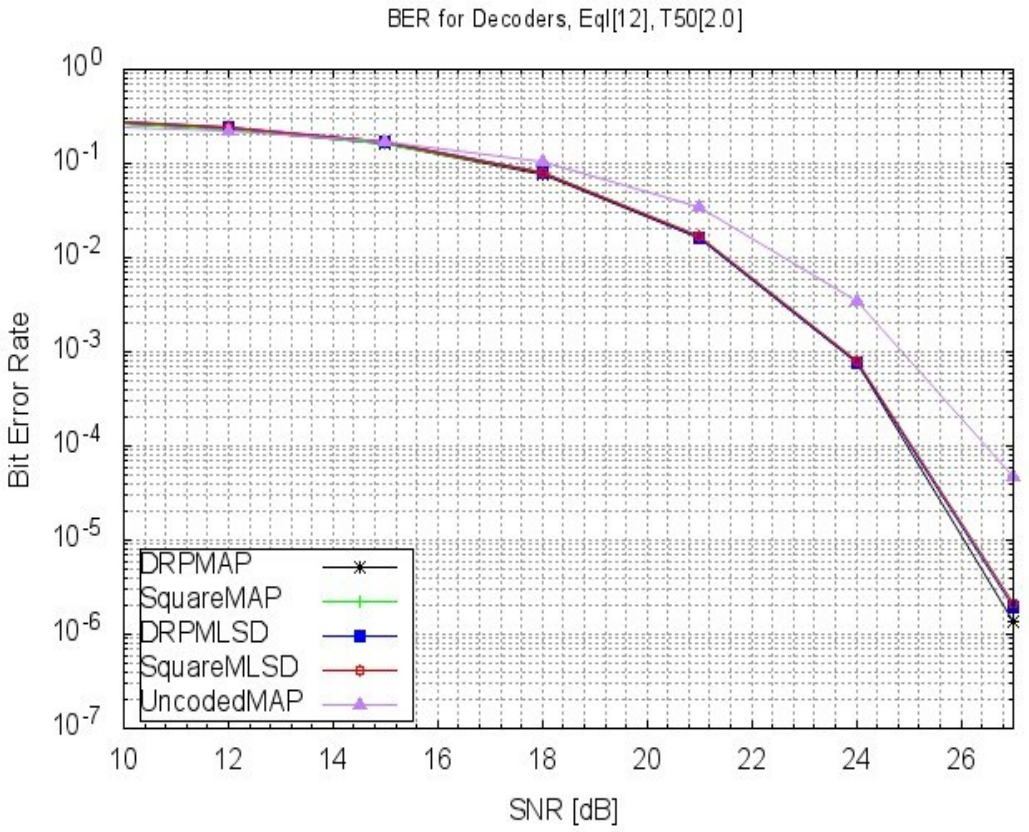


Figure 4.15: BER performance of decoders at $T_{50} = 2.0$.

The performances of the decoders at high ISI regime (T_{50}=2.0) is shown in Figure 4.15. At T_{50}=2.0, the channel is considered to possess a significant amount of ISI due to high areal density along the track. The schemes with single parity-check coding and interleaving outperformed the uncoded MAP case under high ISI channel conditions with about 2 to 2.5dB gain. Also, the Square-MAP outperformed all the other coding and interleaving schemes slightly under this channel condition. This is as expected because the MAP criterion always

tries to minimize the probability of a bit error unlike the ML which minimize the probability of symbol error.

Further comparison of the decoders is made by comparing the FER performance of the coded and the uncoded system under different data density condition of the channel. Figure 4.16 show the FER performance of the detector with the different interleavers and decoding schemes applied to the used data at $T_{50} = 1.0$.

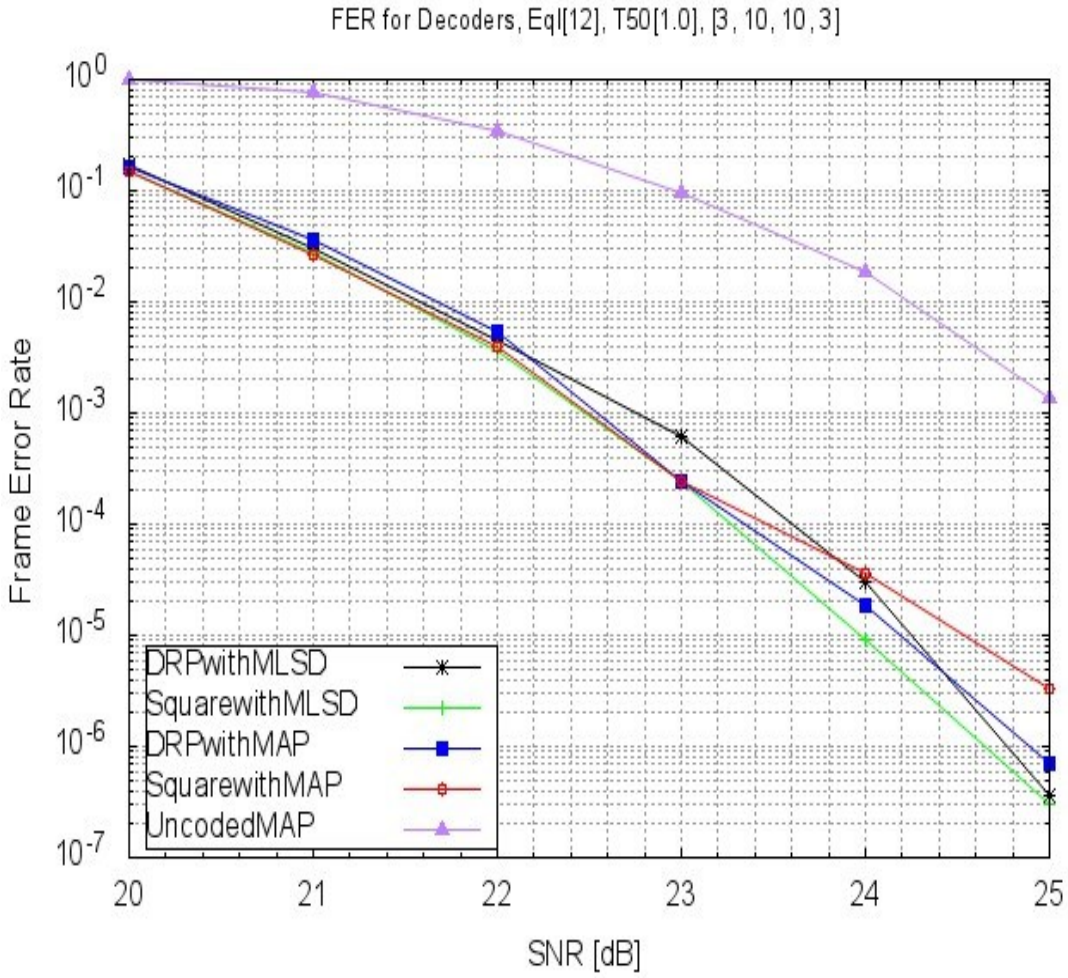


Figure 4.16: FER performance of decoders at $T_{50} = 1.0$.

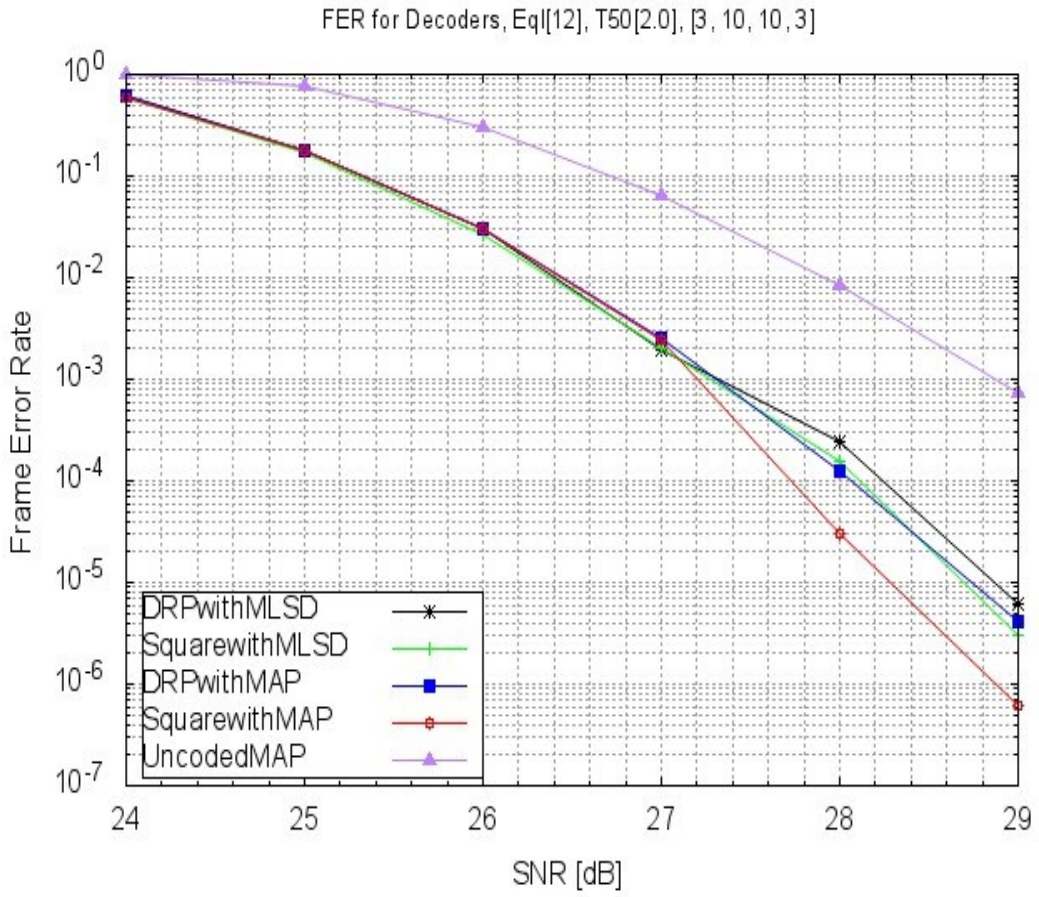


Figure 4.17: FER performance of decoders at $T_{50} = 2.0$.

It shows that the decoder with Matrix/Square interleaver and MLSD decoding outperformed the rest of the decoders with a gain of about 0.5dB or more at the FER point 10^{-5}. Similarly, Figure 4.17 depicts the FER performance of the decoders at T_{50}=2.0. At FER point 10^{-5}, the Square-MAP has a gain of about 0.5dB over DRP-MAP, Square-MLSD and DRP-MLSD, with the uncoded system having the worst performance of all.

The BER performance comparison of the concatenated Matrix/Square-DRP system with that of the Single Square or Single DRP and uncoded MAP system is presented in Figure 4.18. The concatenated Matrix/Square-DRP system called "MAP with Square-DRP" for short has three parity bits added to the user data to form a code with data rate $\frac{64}{125}$. In our implementation of

the MAP with Square-DRP scheme, the first and second parity bits are separated the Matrix/Square interleaver, while the second and the third parities are separated by the DRP interleaver. The comparison is done here to determine the gain that could be achieve by adding extra parity bit with Square-DRP spreading mechanism, while at the same exploiting the simplicity of decoding single parity bit. As against using single DRP or Square system with 3 parity bits, which requires 2 parity bits to be added to the first parity encoder. This violet the single parity bit concept and would increase the decoding complexity of the outer MAP decoder.

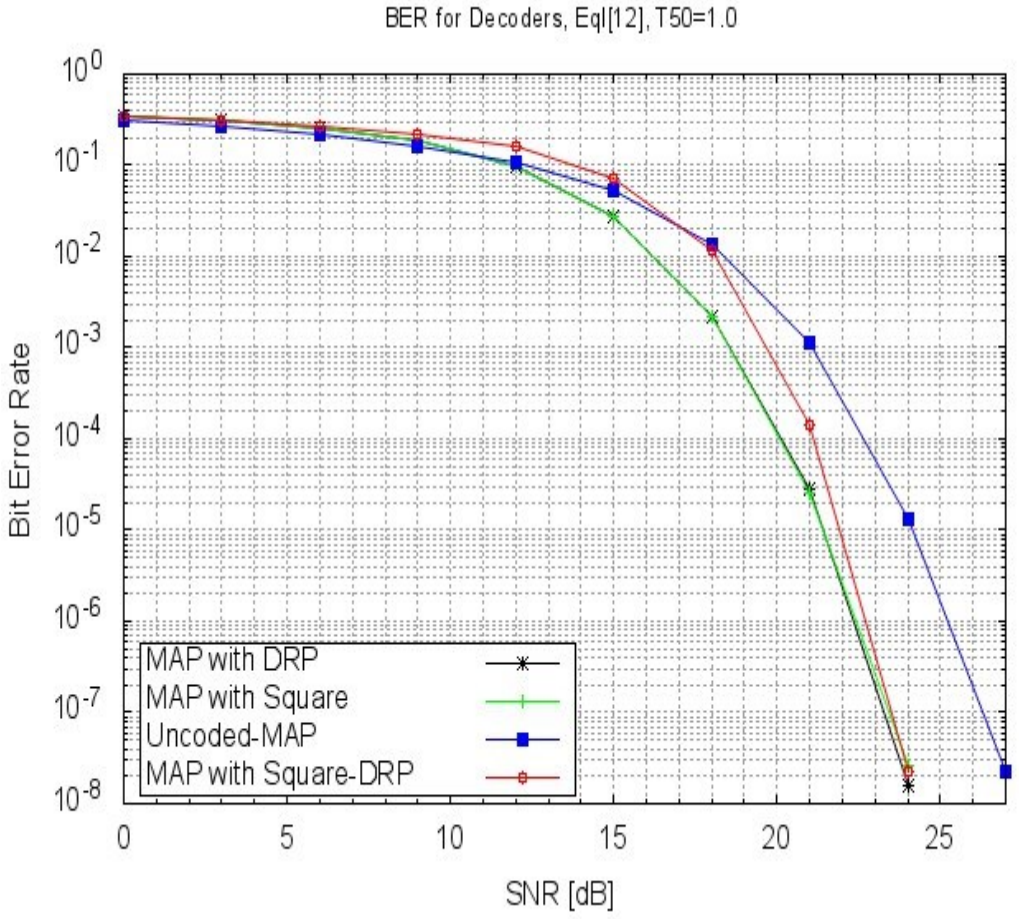


Figure 4.18: BER comparison of single and two concatenated interleaver system at $T_{50} = 1.0$.

An equaliser target length [1 3 4 3 1] was used for the concatenated MAP with Square-DRP scheme along track. As depicted by the Figure 4.17, the Un-concatenated scheme (scheme with single interleaver Square or DRP) has a better performance at low SNR values in comparison with the concatenated system. But as the SNR values increases, the performances almost become similar in both cases. This due to the fact that at $T_{50} = 1.0$, the amount of ISI introduce into the system is minimal and therefore, little amount of coding and signal processing is needed to mitigate the channel interferences.

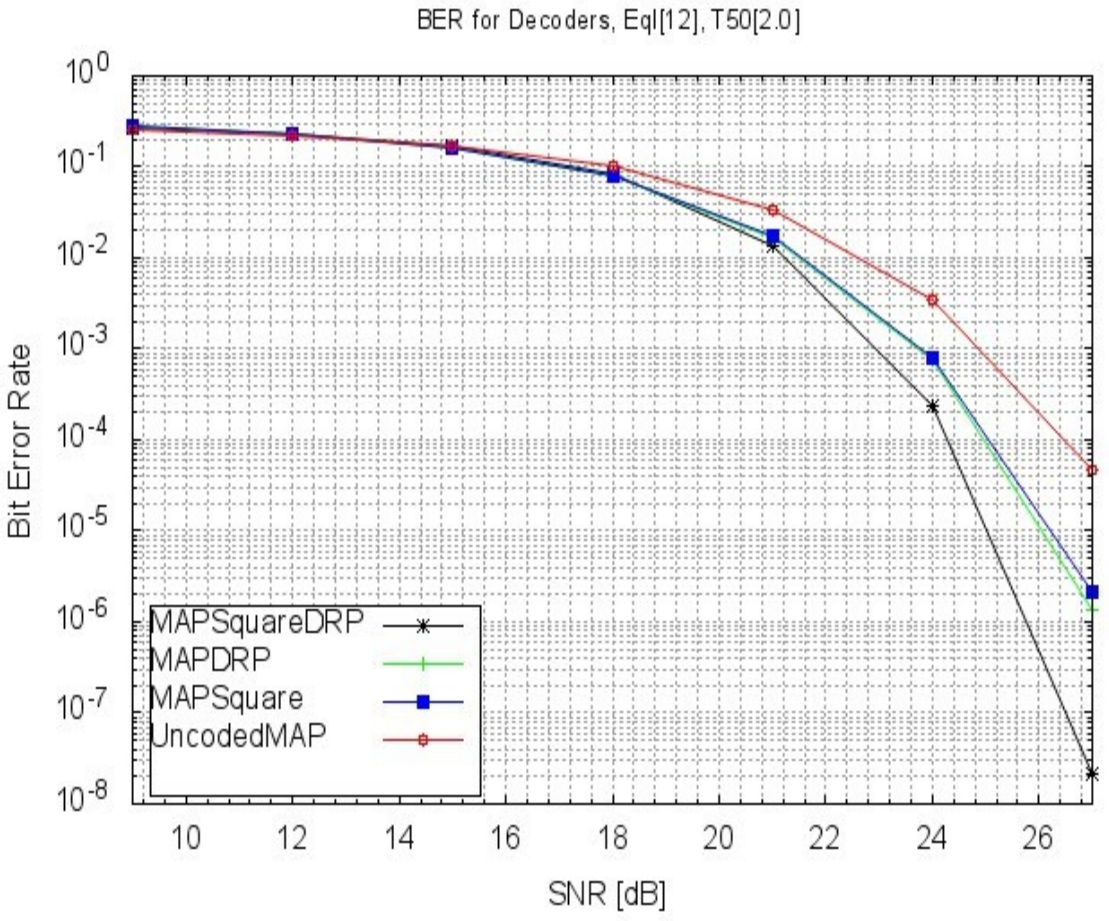


Figure 4.19: BER comparison of single and two concatenated interleaver system at $T_{50} = 2.0$.

However, at high channel density ($T_{50} = 2.0$), even though there was a slight loss in the overall code rate, there is an improvement in the performance of the overall system as depicted by

Figure 4.19. The concatenated Square-DRP scheme outperformed the ones with single interleaver scheme by around 1.5dB gain margin. This means that the concatenated interleaved system is superior to the single interleaved system in channels with high areal density. The SNR gain is expected to rise further as data density increases along track. Therefore, a compromise is presented here in terms the additional decoding complexity incurred due to the extra third parity bits added to the system, and the gain in performance achieved due to its addition.

4.5 Summary

- In a bid to improve the performance of PMR channel, a novel joint detection decoding scheme with single parity check coding and a constrained MAP detector for joint detection/decoding of user data from PMR channel has been presented.

- Design and implementation of single parity encoders and interleavers (DRP and Matrix/square) have been presented. The single parity encoders apply two single parity bits systems, to the user data. With first parity code satisfying the even parity constraint and the second parity code based on odd parity constraint, the two single parity systems are separated by DRP or Matrix/square interleaver.

- A constrained MAP detector with modified trellis structure developed to detect and decode the last single parity bits in the system has been described in detailed and implemented. The constrained MAP detector performs joint detection and decoding of the last parity bits, by selecting the branch transitions whose branch symbols satisfied the parity check equations, at the point where the parity bit comes into the signal. This simplify the detection process and at the same times improve the system performance.

- Performance of the PRML read channel with a PMR media, using MAP detector for different GPR targets of length 4 have been simulated in software using C-programming codes. The results show that symmetric GPR targets performed better than un-symmetric targets at high ISI channel condition. Target [2.0 10.0 10.0 2.0] performs better for low ISI situation ($T_{50} \leq 1.0$), while for larger values of T_{50} targets [3.0 10.0 10.0 3.0] and [2.0 5.0 5.0 2.0] performs better.

- The performance of the PRML system with forward error correction (FEC) of two single parity systems and joint MAP detector decoder has been simulated and compared with that of PRML MAP detector system without FEC. It is shown that the joint detector decoder scheme with FEC of two single parity systems has a gain of about 3 dB over the PRML MAP detector system with no FEC.

- BER/FER performance comparison of the joint detector decoder FEC system using different interleaver configuration and decoding of first parity bits using either MAP or MLSD criterion has been undertaken. The results show that joint detector decoder FEC system with Matrix/Square interleaver and MLSD decoding of first parity bits performs better for low ISI channel $T_{50} \leq 1.0$, while for larger values of T_{50} the system with Matrix/Square interleaver and MAP decoding of first parity bits performs better.

- It is shown that further improvement in performance was achieved when the two interleavers (Matrix/Square interleaver and DRP interleaver) are serially concatenated together. Three single parity bits systems are involved, where the first and second parity bits are separated by Matrix/Square interleaver while the second and third parity bits separated by DRP interleaver. A gain of 1.5 dB is achieved with the concatenated interleavers over single DRP or Matrix/Square interleaver scheme.

Chapter 5

2D Equalisation and Detection for Two-Dimensional Magnetic Recording channel

Parts of this chapter appear in the proceedings of the following conference: Mohammed D. Almustapha, Mohammed Z. Ahmed, Marcel A. Ambroze, & Muhammad B. Abdulrazaq. 2D BCJR along track and across tracks detection for shingled magnetic recording media. In *Telecommunications and signal processing (TSP), 2017 40th International Conference on* (pp. 515-519). IEEE.

5.1 Introduction

TDMR is a promising technology for future magnetic recording systems. It is among the candidate technologies proposed for increasing the areal density of magnetic recording systems. TDMR uses a combination of the SMR technique and 2D readback equalisation and detection techniques. Unlike in the conventional magnetic recording system where interference is only along the down track direction (that is ISI only); in TDMR system, the interferences are present in both along track (ISI) and across tracks (ITI) directions. Therefore, it is important to note that, for the signal to be fully recovered in the TDMR system, both the ISI and ITI contributions

to the signal must be considered in the equalisation and detection processes. This allow for higher areal density to be attained with improved performance in signal detection. However, this also results in an increase in complexity of the detector.

In a multi-track TDMR system, joint-track detection is carried out by either applying a linear equaliser to cancel the interference in one direction and partial response maximum likelihood (PRML) detection in the other direction (Abdulrazaq, Ahmed and Davey, 2015b), or full 2D SOVA (Zheng et al., 2014), (Zheng and Zhang, 2015). While using a linear equaliser reduces the detection complexity, there is a loss of performance incurred at extreme ISI and ITI conditions. The full 2D SOVA provides better detection performance but have higher complexity compared to the former.

The complexity of the full 2D detectors for joint-track detection is in an exponential order of 2^{wk} where, w represents the number of tracks and k represents number of bits involved. This limits their deployment especially when more tracks are involved. Besides the computational complexity, most 2D detectors especially ML detectors applied in along track direction do not fully utilize the information available from the other direction, since the detector is applied only along one of the directions. This degrades the detection performance when the interference from the other direction is high. An optimum detection strategy is therefore needed.

An optimal 2D detector carries out multi-track joint 2D detection across all tracks to fully exploit the 2D interferences present in both directions (Zheng et al., 2014). Although it suffers from high implementation cost, its implementation seems increasingly feasible in future recording systems with the current improvement in CMOS technology deployment (Kim, 2012).

A multi-track 2D SOVA for joint track detection of SMR media was proposed by (Zheng et al., 2014). The 2D SOVA detects data jointly from multiple tracks in the presence of 2D

interference. In (Zheng and Zhang, 2015) a low-complexity 2D SOVA designed to reduce the complexity of the multi-track 2D SOVA was presented. However, in both detectors, 2D SOVA is applied in the down track direction only, since multiple tracks were considered jointly. This results in performance degradation when the ITI across tracks is high. Meanwhile, in (Abdulrazaq, Ahmed and Davey, 2015a), 2D SOVA concatenated with a regular Viterbi detector was proposed for detection of data from SMR media. Although the detection complexity was reduced, the 2D SOVA and the Viterbi detectors employed do not fully exploit the trellis structure completely in determining the reliability of the decoded bits. A better result and performance can be achieved with optimal 2D MAP and regular MAP detector that exploit the trellis structure by incorporating all the branch metric probabilities in its computations. This ensures that no valuable information on a bit position apriori or aposteriori is discarded, unlike the former case, where a selected few information bits after the given bit position are utilized and the rest are discarded.

The next sections discuss the application of 2D equalisation and detection technique in TDMR system. The approach involves the use of 2D multi-level MAP detector to cancel the ISI along the down track direction and a regular MAP detector across the tracks for ITI cancellation. It performs multi-track joint detection of multiple tracks to extract information from a TDMR system using the SMR media.

5.2 TDMR Channel Modelling

The channel model developed and implemented in both chapters 3, 4 is a 1D PMR based on the assumption that, there is no ITI and ISI is the only interference affecting the data symbols. However, in TDMR system where SMR is employed, but ISI and ITI from adjacent tracks are of major concern. Therefore, ITI need to be incorporated into the channel model to account for the interferences contributed from the neighbouring tracks. Since SMR is envisioned to retain

the existing conventional PMR media structure without media redesign, then the model developed already in section 3.3 can easily be modified to include ITI in order to convert it to a TDMR channel.

The signal output from the conventional PMR media channel as expressed by Equation 3.9 is given as;

$$y(t) = \sum_i x_i h(t - iB) + \sum_i d_i a_i s'(t - iB) \tag{3.9}$$

To include ITI into the PMR channel model in order to convert the channel to 2D SMR, equation 3.9 is modified to include a portion of the data component from the preceding track and the succeeding track that is read when reading the main track. Therefore, the read data (y) of track N will have components from the preceding and succeeding tracks. That is for any bit position "*i*"

$$y_j(i) = \sum_{j=N-n_1}^{N+n_2} w_j Z_j(i) \tag{5.1}$$

Where w_j is the fraction of the adjacent channels contributed to the signal $y_j(i)$, n_1 and n_2 are the number of tracks preceding and succeeding the read track respectively. Also,

$$Z(t) = \sum_i x_i h(t - iB) + \sum_i d_i a_i s'(t - iB) \tag{5.2}$$

Electronic noise, noise from the Read head and other noises that have significant contribution to the signal are modelled as AWGN and added to the read back signal. Therefore, the final read signal can be written by substituting (5.2) in (5.1) and representing the channel response as $h_{i,j} = w_j h(t - iB)$ and the jitter response as $s'_{i,j} = w_j s'(t - iB)$.

The received noisy signal from the TDMR channel output is now expressed given by the expression in equation 5.3 as,

$$y_{i,j} = \sum_j \sum_i x_{i,j} h_{i,j} + \sum_j \sum_i d_{i,j} a_{i,j} s'_{i,j} + n_{i,j} \tag{5.3}$$

Where "*i*" and "*j*" are indexes indicating the position of the bit in the along-track and across-tacks direction respectively. With this modification in place, we have now converted the 1D PMR channel into a 2D interference channel for SMR/TDMR.

5.2.1 TDMR Channel Implementation

The TDMR channel model was developed and implemented using the C programming environment. SMR writing was used as writing process to record the data on the magnetic media. The procedure for implementing the 2D channel is similar to the 1D channel described in section 3.3.5, although, with some modifications to include the ITI from other tracks.

The initialisation phase begins by evaluating the channel isolated channel response $h(t)$ and the jitter response (s') using the set values of T_{50} and V_{max} as described in section 3.3.5. Due to the ITI introduced into the system, the factor for modifying the amplitude of the jitter response (equation 3.14) is modified in order to include the ITI response. Therefore, the factor modifying the jitter response amplitude for 2D channel application is given by the equation 5.4 as,

$$J = \sqrt{0.5 \sum (s')^2 \sum (\rho)^2} \tag{5.4}$$

Where (s') is the jitter response of the channel and ρ represent the ITI response.

Information data to be recorded on the media were assumed to be written in sectors of 8 tracks with 4096 bits per track. A guard band containing -1's (0s) all through is placed between sector separations during the write process. The SMR channel is considered to have ITI of two tracks.

That is to say, $\rho = [\alpha_1, \alpha_2]$.

Where $\alpha_1$and α_2 represent the fraction of the total amplitude read by the Read head from the two tracks. Figure 5.1 shows the SMR channel model with sector dimension used for this work and how ITI from the side track is read by the Read head. Hence, ITI is incorporated into equation 5.4 to account for the signal read by the Read head from the side track.

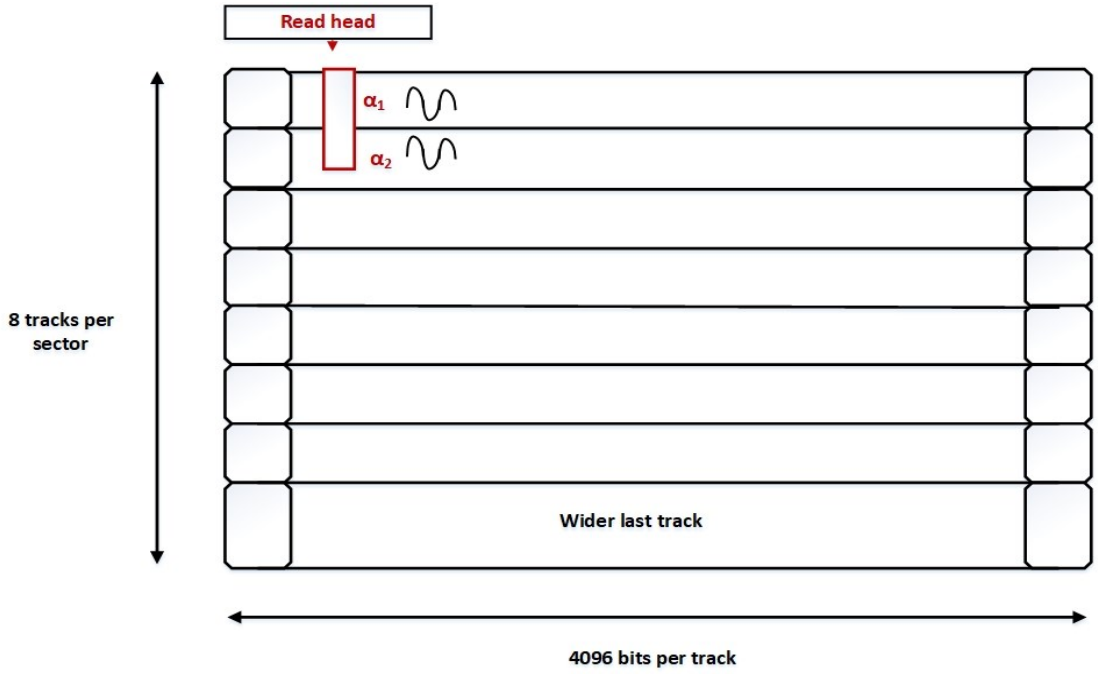


Figure 5.1: SMR channel model with ITI and sector dimension

Due to the shingled writing process, a portion of the first track is assumed to contain -1s written all through and the last track of a sector is assumed to be two times larger than the other tracks. This is to ensure that succeeding tracks do not overwrite the extra width of the last track. Jitter noise power was set to constitute 80% of the total signal noise power while AWGN constitutes the remaining 20% of the total signal noise power. The SNR definition used is the same as that described in section 3.3.5.

For each track, transitions are determined using "$x_{i,j}$" and saved as "$d_{i,j}$". An AWGN with variance σ_j^2 is generated, and multiplied, term by term to the transitions $d_{i,j}$. The result is then convolved with the jitter response $s'(t)$ to generate the jitter noise for each bit position. The

saved data $x_{i,j}$ is also convolved with the channel isolated response $h(t)$ along the track to generate the ISI data of each track. The resulting ISI data generated is then added to the jitter noise that was already determined above. This gives a signal containing ISI and 1D jitter noise. The signal is then convolved across tracks with the ITI response to produce a 2D interference signal with ISI along the track and ITI across the tracks. The final 2D signal from the channel $y_{i,j}$ is determined by adding AWGN of variance σ_w^2 to the resulting 2D signal above, as demonstrated by equation 5.3. Figure 5.2 shows the block diagram representing the processes involved in generating the 2D signal for the SMR/TDMR channel model.

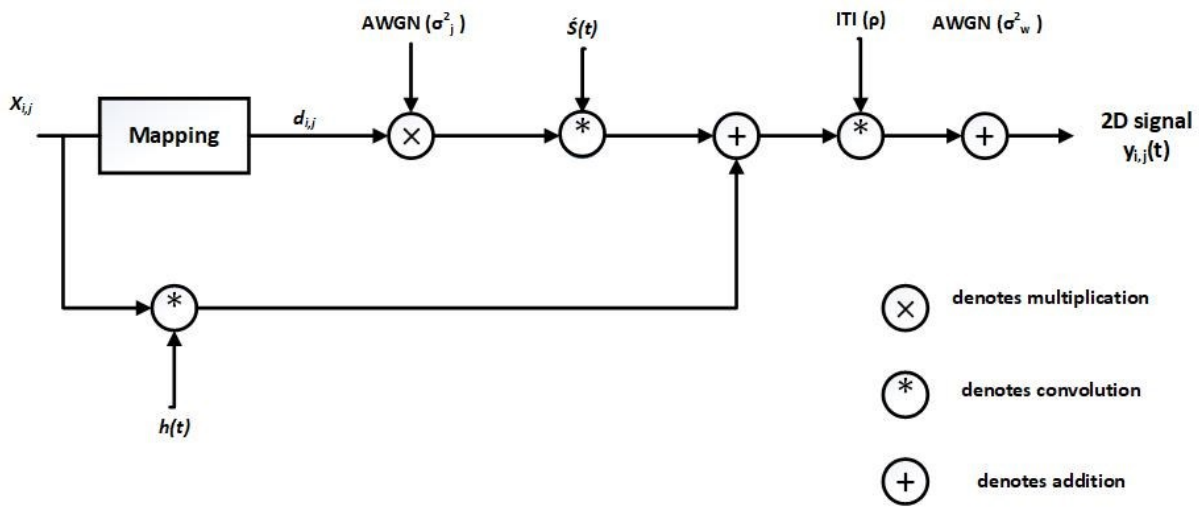


Figure 5.2: Block diagram of 2D signal generation for the SMR/TDMR channel

5.3 Equalisation

After reading the signal from the 2D channel, the data is shaped to the desired 2D target before detection in order to reduce the complexity of the detector. In the 2D system, because of the interferences from both sides (along track ISI and across tracks ITI), two equalisers are used in turns for both directions in order to shape the data into the desired 2D target response. The equaliser applied along the track is a PR equaliser in which the coefficients needed to shape the

data to the required target are derived by evaluating the matrix equation as expressed in equation 5.5.

$$E = H^{-1}T \tag{5.5}$$

Where E gives the equaliser coefficients required to transform the signal shape to that of the desired target response, while H is the matrix approximation of the channel response. T is a column matrix formed by a target vector of equaliser size padded with zeros on both sides.

The same procedure that was previously described in section 3.4 was followed in determining the equaliser coefficients and in shaping the data. The ITI response represents the other target response across the tracks.

5.4 Multi-Bits Full 2D Joint-Track Detection

Full 2D joint-track ML detectors did not gain much attention over the years due to their high complexity until recently in (Zheng et al., 2014), (Losuwan et al., 2012), and (Zheng and Zhang, 2015). The joint-track full 2D detector performs 2D signal detection of multiple tracks simultaneously using a single full 2D ML detector. Data bits from all tracks are jointly combined in order to utilise the information available across all tracks in taking decision about the data. This however, results in an exponential complexity of the detector. Therefore, a new detection strategy is needed in order to reduce the detection complexity to an appreciable limit in which the 2D detection can be implemented for multi-track systems.

A method of reducing the complexity of the 2D detection process by concatenating 2D SOVA with a regular Viterbi detector was proposed in (Abdulrazaq, Ahmed and Davey, 2015a). The 2D SOVA was applied in the down track direction to cancel the ISI and the regular Viterbi in

the across track direction to cancel out the ITI. This reduced the 2D detection complexity from an exponential order to linear with the number of tracks involved.

In our implementation of 2D detection, we use a similar approach to that proposed in (Abdulrazaq, Ahmed and Davey, 2015a) with some modification in the detectors used. We used an optimal 2D multi-track MAP detector along the track for joint track detection to cancel the effect of ISI instead of 2D SOVA. Across the tracks, we used a regular soft output MAP detector to cancel the effect of ITI against the hard decision Viterbi detector. This is to achieve better BER performance of the system because the MAP-BCJR detector, gives a superior BER performance compared to SOVA or VA detector as demonstrated in chapter 3 (Figures 3.13, 3.14) in the PMR channel, although with some additional complexity incurred.

5.4.1 Multi-Level/Multi-Track MAP Along track

After equalisation, a multi-track 2D non-binary BCJR detector is applied along the track for ISI cancellation. This removes the ISI present in the received data with ITI remaining which will be handled later by the regular MAP detector across tracks. The output of the 2D MAP detector along track is used by the MAP detector across tracks as branch metric probabilities. Initially, the branch metric probabilities for all branch transitions is computed and used along with the trellis structure to determine the APP of receiving all possible adjacent bits across tracks, depending on the number of interfering tracks involved. These APPs are then saved in history as the branch metric probabilities for the next MAP detector across tracks. The detailed explanation of the multi-track 2D MAP detector is discussed in the next paragraph of this subsection.

In a single track/binary level MAP detector with target length 3, there are four states in the trellis with two incoming and outgoing branches per state. However, for multilevel MAP

detector where more than one bit is received, the number of transition per branch is 2^k and the number of states is $2^{m\times k}$, where "m" is the constraint length ($Target - 1$) of the detector, and "k" represents the number of bits (interfering tracks) involved. For instance, if two tracks are considered (ITI of two tracks), there are 4 branches per state and 16 of states in the trellis for a target length 3. Similarly, when ITI from three tracks is considered, there will be 8 branches per state and 64 states (for target length 3) in the trellis.

In our implementation, we consider ITI from two tracks and a target length 4. Therefore, a trellis with 64 states and 4 branches transiting from each state was used for the detector along track direction for ISI cancellation. Figure 5.3 shows the trellis diagram for the 2D MAP detector along track.

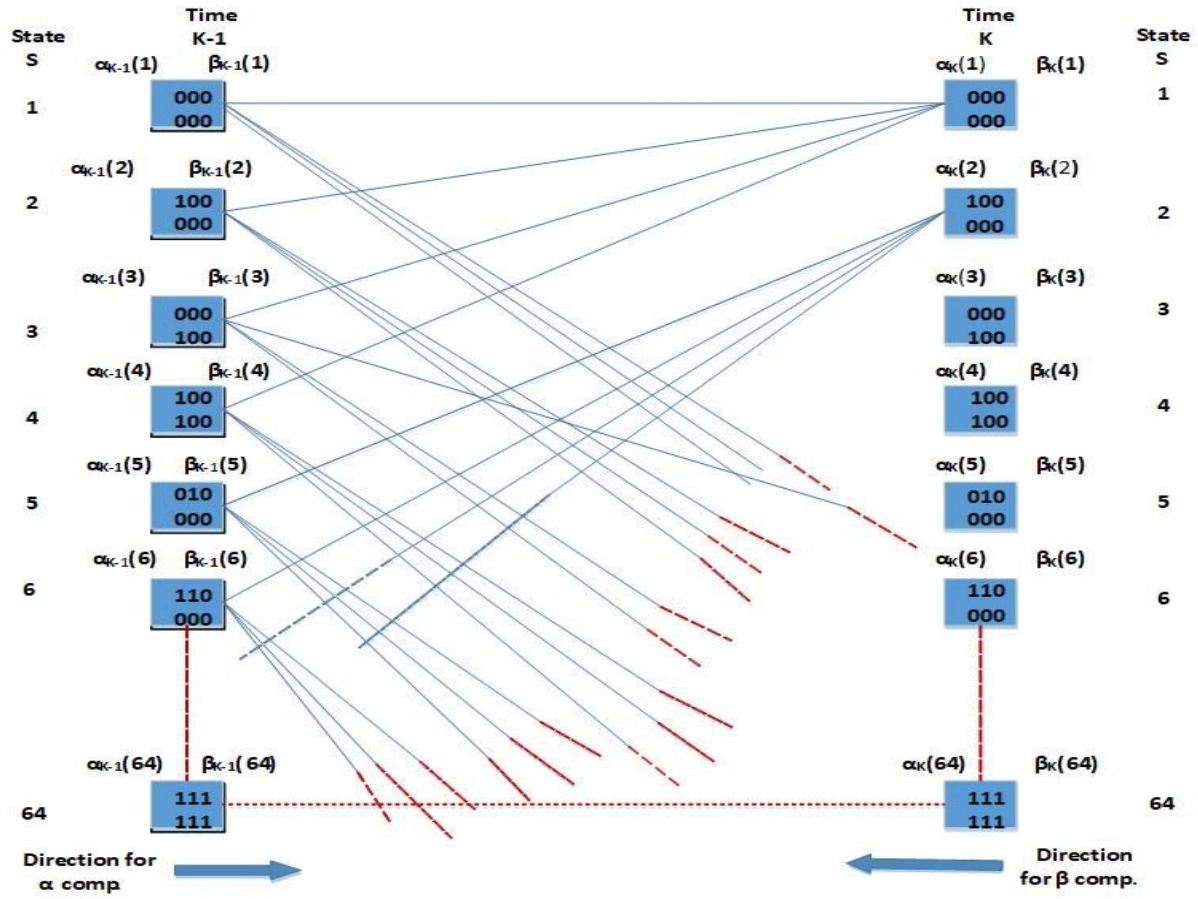


Figure 5.3: Trellis diagram for the 2D detector along-track with target length 4 and two-track ITI.

To implement the detector, the branch transition probability (γ) for each branch is determined using equation 4.7 across the whole trellis. The values of γ are normalised by diving each and every value of γ by the total of the γ's. The normalised γ for each branch now corresponds to the dibit response for that branch. After all the γ's are determined, the next stage is to initialise the forward recursive probability (α) for all states, for the first received symbols. In our Implementation, α for the first state is given a value of 1, while 0 is assigned to the α's for other states. The α's for the next state transition are determined by multiplying γ with the α of the state from which the branch originates to get the branch transition probability. The branch transition probabilities that terminates at the same state are then summed up to give the α of the new state for the next symbols. The α values determined at each instance are normalised to prevent having all zero values. All the α's determined for each time instance are saved up to the last data of the track.

When all the α's are determined and saved, the backward recursion then begins by initialising the backward recursive probability (β) for all states, for the last received symbols at the end of the trellis. The first state is given β of 1, while the rest are assigned β of 0. The β's for all states at each time interval are determined using the same procedure used in determining α's except it is started backward from the end to the beginning of the trellis.

After all the γ, α, β, are determined across the whole trellis, the APP of each pairs of the received symbols being [0, 0], [0, 1], [1, 0], and [1, 1] is determined. The α for each state is multiplied by the γ of the branches originating from that state, and then multiplied to the β of the state to which the branches transited to. This produces the branch APPs probabilities for each branch transition. All branch APPs that emanates from states having their state-symbols ending with $\begin{matrix}0\\0\end{matrix}$ are added as the APP of [0, 0], those ending with $\begin{matrix}0\\1\end{matrix}$ are added as the APP of [0, 1], those ending

with $\begin{matrix}1\\0\end{matrix}$ are added as the APP of [1, 0], and finally those ending with $\begin{matrix}1\\1\end{matrix}$ are added as the APP of [1, 1]. The APPs are then normalised to prevent the occurrence of all zero values.

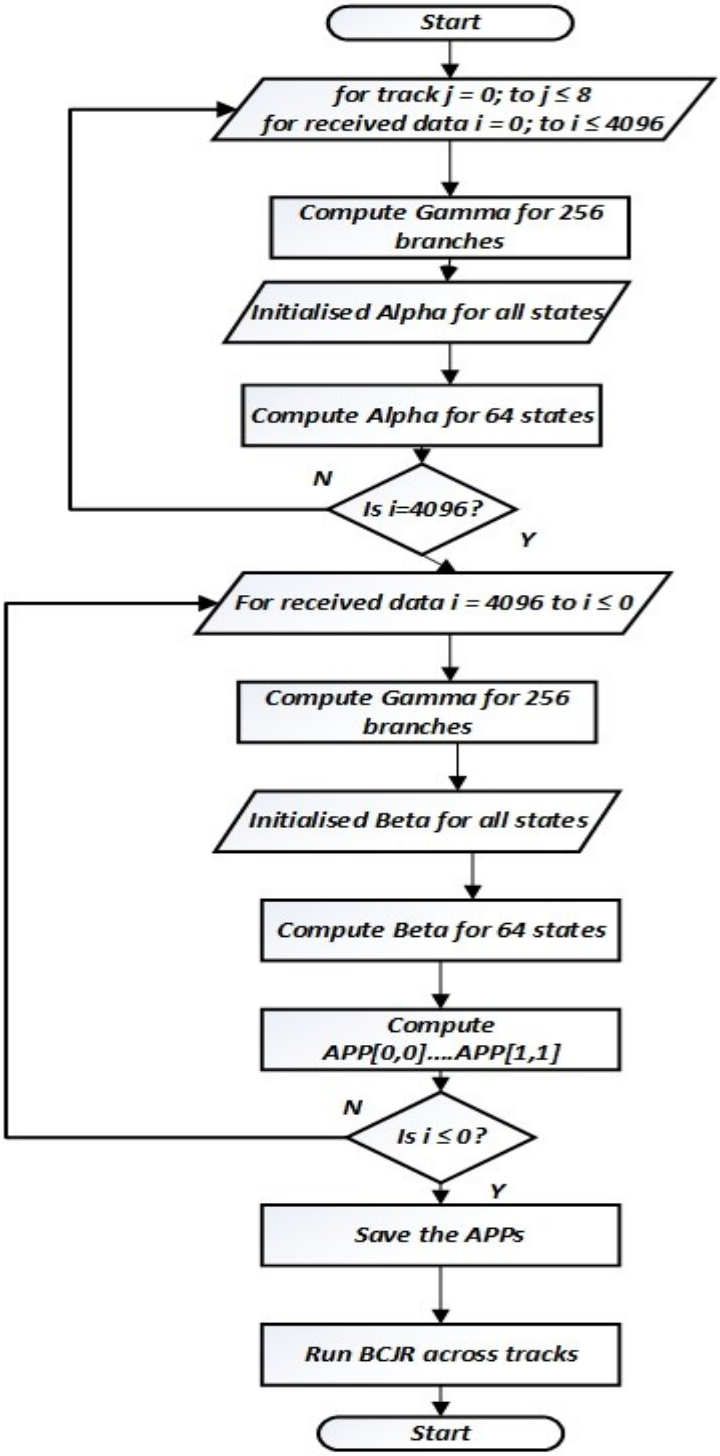


Figure 5.4: Flow chart for 2D MAP joint track detection along track.

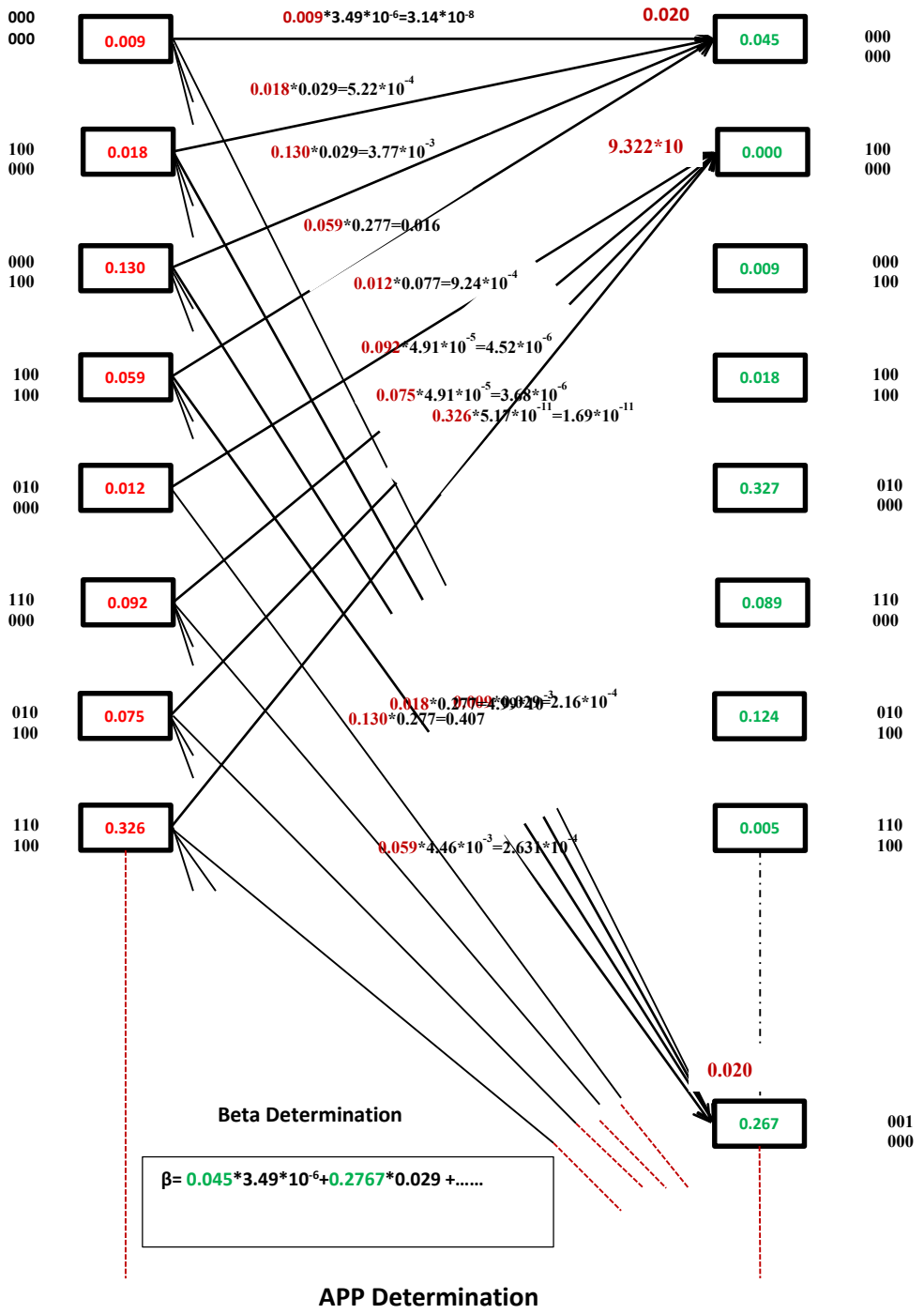
When all the tracks are processed, the APPs are stored in history register to be used as the branch metrics for the MAP detector across tracks for ITI cancellation. Figure 5.4 depicts the flow chart generated for the 2D MAP detection process along track for joint detection of two-track ITI system.

5.4.2 Example of Multi-level 2D MAP Implementation

In this example, we assumed a two-track interference system with ITI from both tracks and target [0.4, 1.0, 1.0, 0.4] along the track. The interference contribution from both tracks is set as (ITI= [1, 1]), that is same interference level (full ITI) from both tracks. If at an SNR of 10 dB, the received signal at that instance is assumed to be (-4.12). Then, the γ for each branch transition is determined using equation 2.25 as shown in Table 5.1. The first column of Table 5.1 represents the branch symbols responsible for the states transitions within the trellis.

Table 5.1: Branch metric (Gamma) determination.

Branch symbols	Dibit	Gamma (γ)	Normalised (γ)
0000 0000	-5.6	$e^{(-\frac{(-5.6+4.12)^2}{2\times0.1}}=1.75\times10^{-5}$	3.49×10^{-6}
1000 0000	-4.8	$e^{(-\frac{(-4.8+4.12)^2}{2\times0.1}}=0.099$	0.029
0000 1000	-4.8	$e^{(-\frac{(-4.8+4.12)^2}{2\times0.1}}=0.099$	0.029
1000 1000	-4.0	$e^{(-\frac{(-4.0+4.12)^2}{2\times0.1}}=0.931$	0.277
0100 0000	-3.6	$e^{(-\frac{(-3.6+4.12)^2}{2\times0.1}}=0.258$	0.077
1100 0000	-2.8	$e^{(-\frac{(-2.8+4.12)^2}{2\times0.1}}=1.65\times10^{-4}$	4.91×10^{-5}
0100 1000	-2.8	$e^{(-\frac{(-2.8+4.12)^2}{2\times0.1}}=1.65\times10^{-4}$	4.91×10^{-5}
1100 1000	-2.0	$e^{(-\frac{(-2.0+4.12)^2}{2\times0.1}}=1.74\times10^{-10}$	5.17×10^{-11}
0001 0000	-4.8	$e^{(-\frac{(-4.8+4.12)^2}{2\times0.1}}=0.099$	0.029
1001 0000	-4.0	$e^{(-\frac{(-4.0+4.12)^2}{2\times0.1}}=0.931$	0.277
0001 1000	-4.0	$e^{(-\frac{(-4.0+4.12)^2}{2\times0.1}}=0.931$	0.277
1001 1000	-3.2	$e^{(-\frac{(-3.2+4.12)^2}{2\times0.1}}=0.015$	4.46×10^{-3}



APP(00)=0.009*3.49*10-6*0.045+0.018*0.029*0.045+0.130*0.029*0.045+0.059*0.277*0.045+0.012*0.077*0.000+0.092*4.91*10-5*0.000+0.075*4.91*10-5*0.000+0.326*5.17*10-11*0.000+.....

APP (01) =0.009*0.029*0.267+0.018*0.277*0.267+0.130*0.277*0.267+0.059*4.46*10-4*0.267+.....

APP (10) =.....

APP (11) =.....

Alpha: Red **Gamma: Black** **Beta: Green**

Figure 5.5: Example of 2D MAP implementation.

For instance, the branch symbols $\begin{matrix}0000\\0000\end{matrix}$ are responsible for transition from state $\begin{matrix}000\\000\end{matrix}$ to the state $\begin{matrix}000\\000\end{matrix}$. Similarly, $\begin{matrix}1001\\0000\end{matrix}$ are for transition from state $\begin{matrix}100\\000\end{matrix}$ to state $\begin{matrix}001\\000\end{matrix}$ and so on. The computed γ values are normalised by dividing γ with the total γ's as shown in Table 5.1.

The α and β calculations for this example are shown in Figure 5.5. The values in red are for α's, those in green are for β's, while the γ's are in black. We assumed that at the instance of receiving the signal, the α for all states are: (0.009, 0.018, 0.130, 0.059, 0.012, 0.092, 0.075, 0.326,… etc.). And also, the β for all states at the instance of receiving the signal are: (0.045, 0.000, 0.009, 0.018, 0.327, 0.089, 0.124, 0.005,….0.267,….. etc.). To determine the next state α, the γ for each branch is multiplied with the α of the state from which the branch emanates from to get the branch probability, as shown in Figure 5.5. All branches terminating to a new state will have their branch probabilities added to give the new γ for the next state. Similarly, approach is applied for determination of γ for the next state both in the reverse direction.

After all the α's and β's for all the states are determined, the APP of symbols being 00, 01, 10 and 11 are determined. This is done as illustrated in Figure 5.5 by taking each α of a state, multiplied it with the γ of the branch that originate from that state, and then multiplied again with the β of the next state to which the branch terminates. All paths that have their transition due incoming symbols 00 are summed up to get the APP [00]. Those that are produced due incoming symbols 01 are summed up to give APP [01] and so on.

5.4.3 MAP Detector Across-Tracks for ITI Cancellation

Once all the tracks are processed, the saved APPs from the output of the multi-level 2D MAP detector along the track are now used as the branch metrics for detector used across tracks for the ITI cancellation. The first bits of all the tracks are now considered in a sequential manner. That is to say, the first bit on track one is considered as the first data bit, then followed by the

first bit on track two as the second data bit, and so on until all the data bits on the tracks are processed.

The MAP detector across tracks has a reduced trellis structure with two states and two branches per state as shown in Figure 5.6. The saved APPs representing the four possible probabilities now serve as the total number of branch metrics. The α's and β's are determined using the initial conditions, and the saved APPs from the 2D MAP detector along track as the new branch metrics (γ).

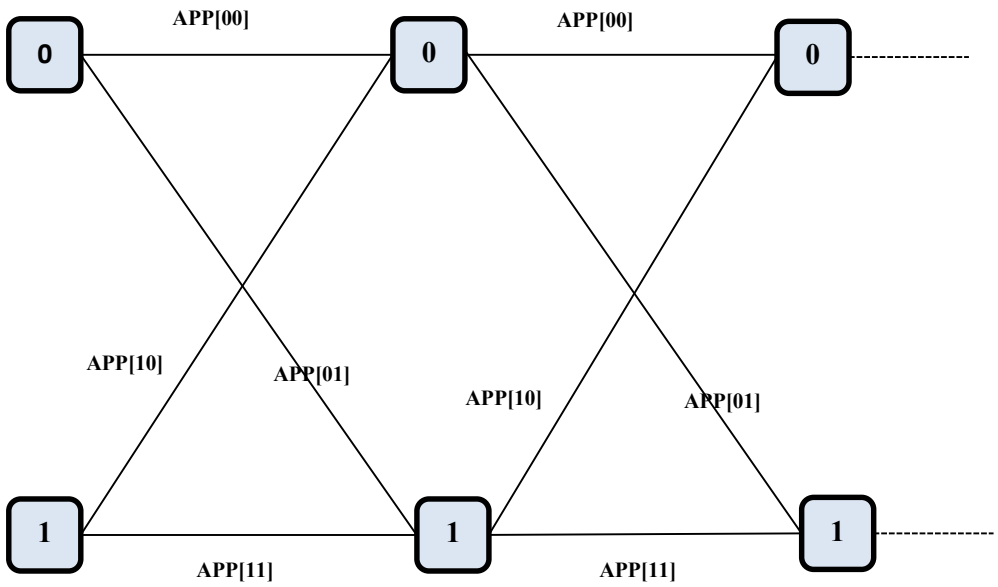


Figure 5.6: Trellis diagram of MAP detector across-track.

After all the α's and β's determined, the APP of each symbol being either a 1 or a 0 is determined across the tracks. This is done by taking the α for each state, multiply it by the saved APPs representing the branch metrics of the branches that originate from that state, and then to the β of the state to which the branches terminate. This process is continued until all the data from all the tracks are detected sequentially. This again produces the branch APPs for the ITI detector across tracks. The APP of 0 is obtained by adding up the branch APPs whose transition is produced due to the bit 0, and the APP of 1 is produced by adding up those due to the bit 1.

The final output data across tracks is decided based on the highest APP value. This detects the data out of ITI.

5.5 Results and Discussion

The performance of the multi-track detector with target [0.4 1.0 1.0 0.4], ITI [1.0 1.0] (full ITI for both tracks), for varying densities along track (different values of T_{50}) is shown in Figure 5.7. Note that, finding suitable PR target for detection depends on the data density of the channel. Therefore, changing the PR target can affect the performances result of Figure 5.7 because different PR targets gives different performances for various channel density.

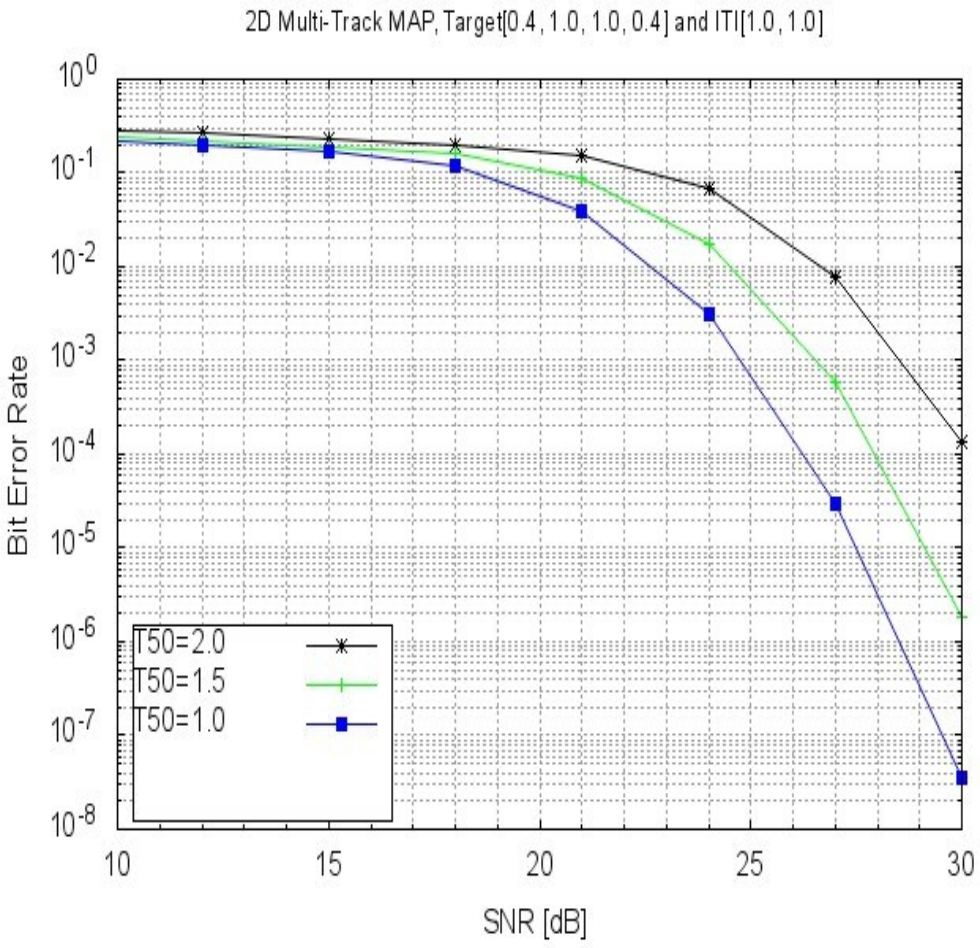


Figure 5.7: Performance comparison for different data density at ITI [1.0 1.0].

PR target [0.4, 1.0, 1.0, 0.4] which is equivalent to [2.0, 5.0, 5.0, 2.0] was used here because it had the best performance compared to any other target of length 4 at high data density (see Figure 4.7). It is seen that the performance of the detector is best when ISI along track is low ($T_{50} = 1.0$). $T_{50} = 1.0$ has a gain of about 2dB over $T_{50} = 1.5$ and almost 6dB compared to $T_{50} = 2.0$ at BER point 10^{-3}. This is as expected because increasing the data density results in more ISI with generally degrades the performance of the system as also was shown in the previous chapter for 1D system.

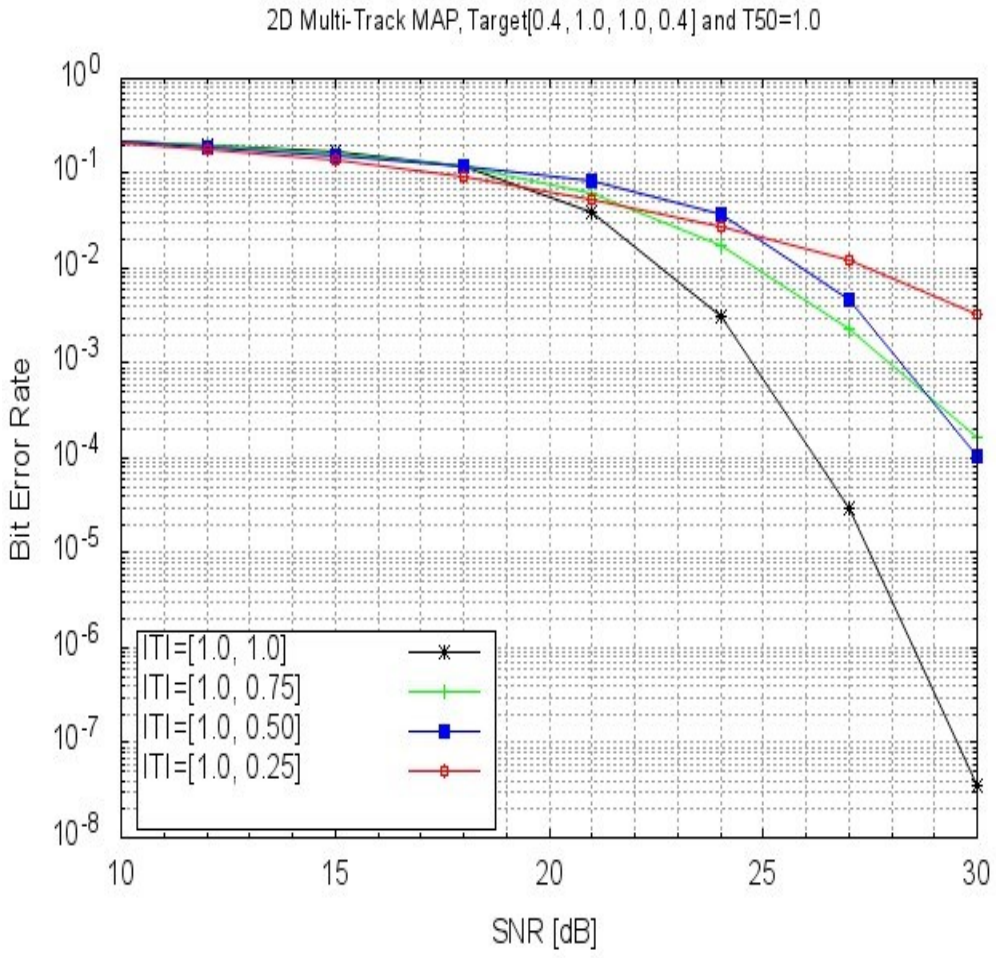


Figure 5.8: Performance comparison for different ITI levels at $T_{50} = 1.0$.

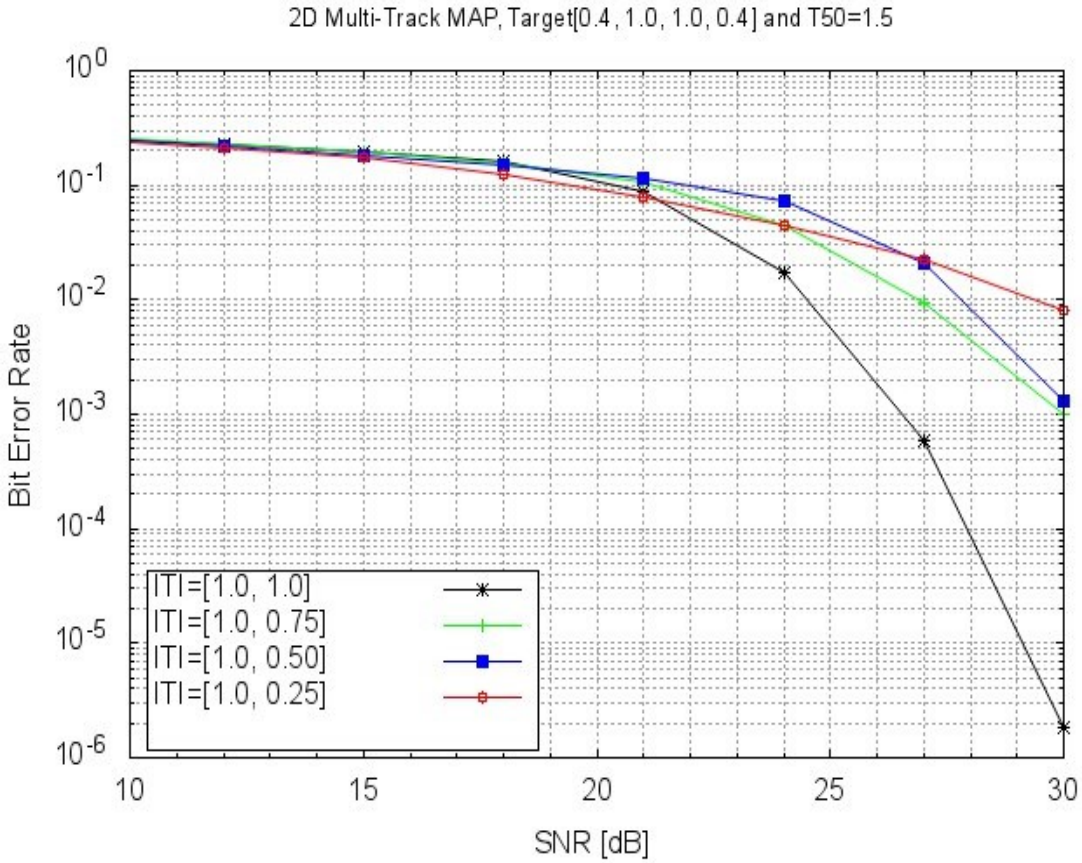


Figure 5.9: Performance comparison for different ITI levels at $T_{50} = 1.5$.

Figures 5.8, 5.9, and 5.10 show the performance of the multi-track detector at $T_{50} = 1.0$, $T_{50} = 1.5$, and $T_{50} = 2.0$ respectively with varying ITI levels. ITI [1.0 1.0], [1.0 0.75], [1.0 5.0] and [1.0 0.25] gives the contribution of the main track and side track to the overall signal and also, represent the extent to which the side track data interferes with the main track data. In all the three cases ($T_{50} = 1.0$, $T_{50} = 1.5$, and $T_{50} = 2.0$), it is observed that different ITI levels have different effect on the performance of the detector. The performance of the detector is best when the ITI is high ([1.0 1.0]) for all ISI condition. In Figure 5.8, ITI [1.0 1.0] has a gain of about 4dB over ITI [1.0 0.75] and almost 6dB compared to ITI [1.0 0.25]. The ITIs [1.0 0.75] and [1.0 0.50] show performances that are very close to each other at $T_{50} = 1.0$.

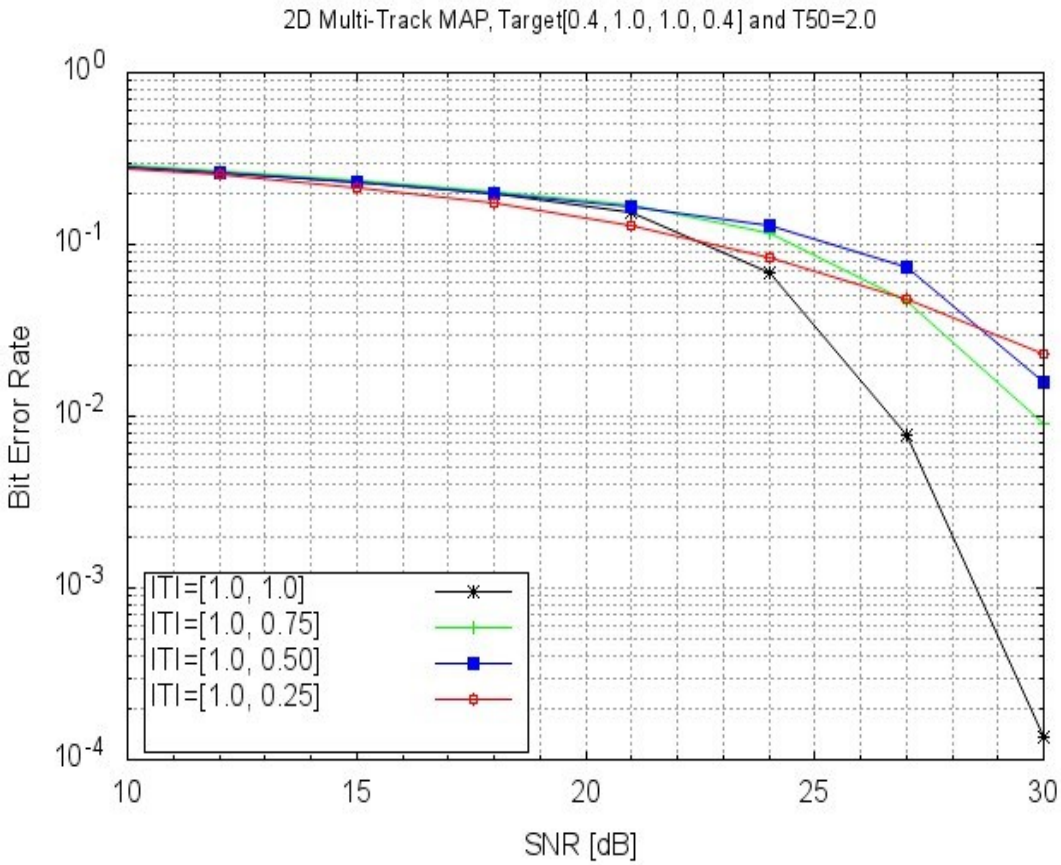


Figure 5.10: Performance comparison for different ITI levels at $T_{50} = 2.0$.

Figure 5.9 shows that the gain recorded for ITI [1.0 1.0] over the other ITIs slightly reduces as the T_{50} value is increased to $T_{50} = 1.5$. The gain reduced to about 4dB for ITI [1.0 1.0] over ITI [1.0 0.75] and 5dB compared to other ITIs. Similar trend is observed in Figure 5.10 at $T_{50} = 2.0$, the gain is reduced to around 3dB and 4dB respectively. The ITI [1.0 1.0] outperformed all the other ITIs due to the fact that, it has the highest minimum separation distance between the different possible symbols of all (see Table 5.2). This improves the SNR of the captured signal from both tracks by making it higher. Also, the ITI [1.0 1.0] here means that the Read head covers all portion of both tracks capturing more signal energy of the side track, which is beneficial for the 2D detector. However, in practice it is impossible to get all the signal energy of the side track without exceeding into other adjacent tracks. The assumption is made here for analysis purpose.

Table 5.2: Minimum distance separation of ITI targets

ITI	Possible symbol levels	Minimum distance	Ratio to peak level
[1.0 0.25]	1.25, 0.75, -0.75, -1.25	0.5 (1.25 – 0.75)	0.4
[1.0 0.50]	1.50, 0.50, -0.50, -1.50	1 (1.50 – 0.50)	0.66
[1.0 0.75]	1.75, 0.25, -0.25, -1.75	1.5 (1.75 – 0.25)	0.86
[1.0 1.0]	2.0, 0.0, 0.0, -2.0	2 (2.0 – 0.0)	1.0

5.6 Evaluation of the Design

A linear equaliser of length 12 and target [0.4, 1.0, 1.0, 0.4] is employed for shaping the received data along the track. The ITI of the two tracks is used as the target in the across-track direction. The data output from the channel is directly passed into the equaliser along track for shaping and then immediately used for joint track 2D MAP detector to produce 4 metrics (APPs). The resulting 4 metrics are then immediately used for the MAP detector across tracks.

The BCJR algorithm for MAP detection requires separate calculations for α, β, and APP determination before an output is produced. α, β, and γ values needed to be computed first before the APPs are determined. Therefore, these values need to be saved before APPs are calculated which means a form of memory storage is needed to store α, β, and γ with some extra latency incurred in the process. For the 2D MAP, once a data is received after shaping, the γ's and α's for each symbol is determined and saved in memory until the last bit on the track is processed. Then the β's calculation is started immediately the last bit is received and then immediately used to determine the APPs. This process continues until all the 8 tracks are processed and all the APPs stored in memory as metrics. Therefore, at the end of the 2D detection, a memory capable of storing 4 metrics (APPs) for each of all symbols of a track is required to store the metrics for use by next MAP detector across tracks.

The APPs of the symbols ([0,0], [0,1], [1,0] and [1,1]) represent the metrics of the main track bit of the target along track, with ITI from the succeeding track. In the SMR model, a portion

of the first track is assumed to contain -1's written all through. But in actual practice, it is impossible to get -1's written all through due to the random-access nature of the HDDs. It is, however, presented here to ease the detection process. This therefore, reduced the number of possible states of the 2D MAP detector to 8 with 2 branches per state on the first track. This resulted in complexity reduction and provided an improved detection performance (Almustapha et al., 2017). Similar numbers are obtained for the last track in terms of possible states and branches per state since the last track is considered to be wider than the rest. Which means the same data is read on both sides of the main and the interfering track.

For the MAP detector across tracks, when all tracks are processed by the 2D MAP along track, the saved APPs for each state across the trellis section are used as branch metrics for the MAP detector across tracks to cancel ITI. The MAP across tracks starts from one possible state with two branches originating from it. It then diverges into a 2-state trellis with 2 branches per state and finally terminates into one state at the end of the trellis. The computed APP of the MAP detector across track is taken as the outputted data across the tracks. This data is outputted in groups of 8 bits at a time across tracks and so on until all data bits are outputted.

The latency of a system is an important variable used in evaluating the design of a system. It is the measure of time delay incurred on a system or process between the received of an input to the time when an output is produced. For our own design, the latency incurred is due to the delay produced by the shaping equaliser, delay for metrics determination of the 2D MAP along track and the computational overhead from of MAP detector. The latency is about 2 times the size of a whole sector. This means we have to go first a whole sector size to determine the 4 metrics and go additional sector size before an output is produced across tracks.

5.7 Computational Complexity

The computational complexity of an algorithm is the measure of the number of arithmetic operations performed per symbol detection or decoding (Vasic and Kurtas, 2004). The computational operations involved include basic arithmetic operators such as multiplication, addition, subtraction as well as complex arithmetic operations such as exponentiation and comparison operation. In our system implementation, the complexity of the system is analysed in three folds as per producing an output is concerned immediately after a symbol is received. First is the complexity of the shaping equaliser used in transforming the data to the desired form. There is also the complexity of the multi-track 2D MAP detector along track for ISI cancellation, and last is the complexity of the regular MAP detector across tracks for ITI cancellation.

For the shaping equaliser, in shaping the data, all the coefficients of the equaliser are multiplied by the data. This means that the number of multiplication operations performed is equal to the number of the equaliser length employed. The result of the multiplication is then added together to give the output of the shaping equaliser. This implied that the number of additions performed will be one less than the number of multiplications involved. In our implementation, an equaliser of length 12 is used for shaping the data. Therefore, 12 multiplications and 11 additions are needed for shaping the data.

For the multi-track 2D MAP detector, the computational complexity depends on the design of the detector and the target, plus the ITI involved. For target [0.4, 1.0, 1.0, 0.4] and ITI [1, 1] used in this work, the number of possible reference levels obtained is 29 (from -5.6 to 5.6 at steps of 0.4 unit). Therefore, for the branch metric calculations (γ determination) using equation 4.7, 2 multiplications, 1 addition, and 1exponentiation is required for each reference level to

determine the branch metric. This means that a total of 58 multiplications, 29 additions and 29 exponentiations are required for γ's determination.

To determine α for the next state, γ is multiplied by the initial α of the previous state to get the branch probability. The branch probabilities terminating to the next state are then added to produce the α for that state. In our multi-track 2D MAP detector, there are four incoming and outgoing branches per state. This means that in determining α for a state, there are 4 multiplications and 3 additions involved per state. Therefore, a total of 256 (4*64, for the 64 states) multiplications and 192 (3*64, for 64 states) additions are need for α's determination per symbol processing. Similar numbers (256 multiplications and 192 additions) are also needed for β determination.

The APP is determined by multiplication of α and γ and then β to get the branch transitional probabilities which are the then added up base on symbols that produced the transition to the various states accordingly. This involves 128 (2*64) multiplications and 63 additions for each APP determination. For our two-track ITI model, there are 4 APP levels possible (APP [0, 0], APP [0, 1], APP [1, 0] and APP [1, 1]). This means that in total, there are 512 multiplications and 252 additions involved per symbol processing.

When all tracks are processed, the 4 APP levels from the multi-track 2D MAP detector are saved and used as the metrics for the regular MAP detector across tracks. The detector across tracks has 2 states with 2 incoming and outgoing branches per state. That means 2 multiplications and 1 addition per state is needed for both α and β determination. This is equivalent to 4 multiplications and 2 additions per symbol processing. The APP of the detector has 2 possible either APP of the symbol received being 0 or 1. Therefore, a total of 8 multiplications and 2 additions are needed per symbol processing for the detector across tracks.

Table 5.3 shows the summary of the complexity per symbol/bit processed (without simplification) of the entire detection scheme proposed for the TDMR channel with two-track ITI and target length 4. In the table, "M" is used as a unit to indicate multiplication operation, "A" is represent the addition operation, while "E" is used for exponentiation.

Table 5.3: Computational Complexity

Shaping	12M, 11A
2D BCJR along track	1082M, 665A, 29E
BCJR across tracks	8M, 2A
Total	1102M, 678A, 29E

As comparison with the method presented in (Zheng et al., 2014), (Lousuwan, Warisan and Kovintavewat, 2012) and (Zheng and Zhang, 2015), where a single full-2D detector is used for joint-track detection, our approach offers significant reduction in the complexity order of the detector. For 8 tracks with a target length of 4, the complexity order of the single full-2D detector is $2^{8\times4} = 4{,}294{,}967{,}296$. But using the method presented in this work, with ITI of two-tracks and target length of 4, the complexity order of the detector is reduced to $8 * (2^{2\times4}) = 2{,}048$.

5.8 Comparison to results from other works

In order to determine the viability of our results, we compared the results of our proposed 2D MAP along track and regular MAP detector across track to some results on 2D detection algorithms that were published recently. Results of concatenated 2D SOVA with Viterbi ML detector was presented in (Abdulrazaq, Ahmed and Davey, 2015a). These results are similar to our results presented in this chapter, despite some variations on the ITI channel implementation.

A three track-track channel interference and target length of three bits (3 by 3) was used in (Abdulrazaq, Ahmed and Davey, 2015a) while in our implementation, we used a two-track and target length of four bits (2 by4) channel model.

Zheng et al., 2014 presented the BER performance result for the full 2D detector using SOVA on SMR media (see Fig. 4 of (Zheng et al., 2014)). For comparison, given by the 2D Read head sensitivity function used in the paper, we compare the result to our 2D BCJR situations of $T_{50} = 1.0$ and $T_{50} = 1.5$. The result presented in (Zheng et al., 2014) achieved a BER of 10^{-3} at SNR of 30 dB. Our result achieved the same BER at SNR of 24.5 dB when $T_{50} = 1.0$ is considered and 26.5 dB for $T_{50} = 1.5$. This is despite error floors in the performances and only AWGN noise variance was considered in the SNR definition in their work.

Similar performance comparison is made to the results presented in (Lousuwan, Warisarn, and Kovintavewat, 2012) for 2D SOVA detector. The channel model used for implementing the 2D SOVA detector was a four-grain rectangular model which is less complex and does not put into consideration the effect of timing jitter and other imperfections due to irregular grain sizes/boundaries. Despite these under estimation of channel impairments, the results presented in the paper (Fig. 7 of (Lousuwan, Warisarn, and Kovintavewat, 2012)) achieved a BER of 10^{-4} at over 30 dB. This is less in performance compared to our result that achieved the same BER at less than 30 dB (28 dB shown in Figure 5.5, for $T_{50} = 1.5$). Again, their performance results have error floors throughout similar to (Zheng et al., 2014) at high SNRs.

5.9 Summary

- A low complexity 2D detection technique for SMR/TDMR channel has been presented. The technique employed the use of multi-level 2D BCJR detector along track for ISI cancellation and regular BCJR detector across track for ITI cancellation.

- The modelling and Implementation of TDMR channel with SMR media, using the jitter noise model for two-track interference channel system has been presented.

- The concept of multi-bits full 2D joint-track detection for SMR and TDMR channel has been introduced.

- Multi-level/Multi-track 2D MAP detector along track for two-track interference channel and target length 4 have been fully described. It is used in this work along track for ISI cancellation. An example of 2D MAP implementation for two-track ITI with target [0.4 1.0 1.0 0.4] has also been given.

- A regular MAP detector across track that uses the A-priori probabilities produced by the 2D MAP detector as branch metrics has been described. This detector is used across track for ITI cancellation.

- Simulation performance of the low complexity 2D MAP along track and MAP across track detection scheme on SMR media channel has been presented. The performances results are summarized as follows:

    - It has been shown that the ITI level influences the performance of the detector. The performance of the detector is best when the ITI of the side track is 100%.

    - ITI target [1.0 1.0] outperformed all the other ITI targets due to it high minimum separation distance between possible symbols.

    - Using the concatenated 2D MAP with regular MAP detection scheme, track density can be increased while at the same time achieving improve detection performance with limited complexity.

- Design evaluation and computational complexity of the proposed detection scheme for TDMR channel has been presented. It is shown that for detection of data on an eight track SMR media, the proposed detection method has significantly less detection complexity when compared to full 2D joint-track detection.

- Performance comparisons of the results to other results presented for full 2D detectors have been given.

Chapter 6

Joint Signal Detection and Decoding of TDMR Channel with Single Parity Coding

In this chapter, a FEC system using two single parity-check codes and a 2D multi-track joint detector decoder scheme for simultaneous detection/decoding of data for TDMR systems with SMR media is presented. The joint detector decoder is developed using the BCJR-MAP detection algorithm. Parts of this chapter appear in the proceedings of the following conference: Almustapha Mohammed D., Ahmed Mohammed Z., Ambroze Marcel A., & Abdulrazaq Muhammad B. Multi-track 2D joint signal detection and decoding for TDMR system using single parity-check coding. In *IEEE 30th Canadian Conference on Electrical and Computer Engineering* (*CCEC 2017*) on (pp. 151-156), April 30 to May 3, 2017, Windsor, Canada.

6.1 Introduction

The success toward achieving high areal density storage using TDMR relies heavily on the development of advanced coding and signal processing techniques. These include detection and decoding schemes used in various communication receivers to detect and decode the transmitted data bits.

Iterative detection and decoding is a popularly known detection/decoding technique used in most communications channels and recording systems to improve the system error performance. The iterative detector/decoder (Koetter and Tuchler, 2004) system is functionally divided into two parts. The first part is the soft output detector such as the SOVA (Hagenauer and Hoeher, 1989) detector or the BCJR algorithm (Bahl et al., 1974) detector that runs over a trellis, while the second part comprised of a sum product algorithm (SPA) (Song and Kumar, 2004) or belief propagation decoder (Colavolpe and Germi, 2005) that operates on a factor graph (FG). Prior knowledge of the channel is available at the decoder while the detector has prior knowledge of the code. As such, soft information is exchanged between the detector and the decoder iteratively until the desired (best result) performance is achieved. Although the iterative detector/decoder gives good performance over a long codeword length when certain iteration cycles are attained, the overall performance is suboptimal due to two factors. Firstly, the SPA is suboptimal due to the presence of short cycles in the decoders FG. The decoder performed poorly whenever there are short cycles (4-cycles below) in the coding FG. Therefore, more effort and time need to be invested to make sure short cycles are removed from the code. Secondly, the iterative process itself is another source of sub-optimality induced into the system. This is evident due to the fact that addition iterations in the decoder yield improve performance, implying that at the end of each iteration, the performance is suboptimal. Iterations are carried out both within the SPA decoder and between the soft-output detector and the SPA decoder.

Consequently, in order to avoid the iterative process and the sub-optimality of the SPA decoder, an alternative detection/decoding approach was proposed in (Chan et al., 2014) termed the Joint Viterbi Detector Decoder (JVDD). The JVDD detector/decoder evades the SPA decoder by combining both detection and decoding operations on a single trellis structure. It achieved that through *metric thresholding* and *parity checking* on survivor paths simultaneously, in an

attempt to return the sequence in the trellis with the minimum metric legal codeword (MMLC) (Shafiee, Sann and Liang, 2014). Viterbi algorithm is executed during the metric thresholding part of the JVDD algorithm to compute the survivor metric for a node. Survivors with metrics close to the predefine threshold are saved while those with metric exceeding the threshold metric are discarded. Parity checking function is executed on the incoming survivor path to a given node when enough bits have been detected. This usually occurs at the tail end of the trellis when the last "1" of a row in the parity check matrix is reached (Chan et al., 2014). As a result, the number of survivor paths to be retained grows quickly as the JVDD algorithm progresses, leading to high computation complexity especially for longer codeword lengths.

In Chapter 4, we presented the MAP joint detector decoder with single parity check coding and interleaving. The BCJR algorithm was utilised for MAP joint detection and decoding of the parity bit using the trellis structure by selecting only the branches whose branch transition symbols satisfied the parity check equation. This reduces the number of valid branch transitions to half whenever the parity bit entered the received signal thereby, reducing the detector complexity. However, in chapter 5, a 2D multi-track detection strategy for TDMR channel with both ISI along track, and ITI across-tracks was presented. The strategy involves concatenating 2D multilevel MAP detector with a regular MAP detector in order to reduce the detection complexity of the 2D detector from exponential order to linear with total number of tracks.

In this chapter, the application of 1D MAP joint detector decoder with single parity check constraint presented in chapter 4 is extended to a 2D interference channel. A new constrained multi-track 2D MAP detector/decoder for joint track detection and decoding of multi-track TDMR system is proposed. It is used to extract information from a two-dimensional magnetic recorder with shingled magnetic recording media. The multi-track 2D MAP detector/decoder performs joint track detection and decoding of parity bit on a single trellis structure running the

same BCJR algorithm. Output from the 2D MAP detector applied along track is used as metrics for another MAP detector running across tracks for ITI cancellation.

Two coding approaches to single parity check coding are proposed. The first approach is similar to that used in chapter 4. Two single parity check bits separated by a DRP interleaver are applied in the along-track direction only. The interleaver here is used to provide adequate spreading of the data as well as the parity bits in order to avoid localisation of cluster error within the data sequence. In the second approach, one parity bit is applied along track and the other parity bit is applied across track, as against applying them all along track as in the former approach. This is to reduce the complexity burden associated with the interleaving and de-interleaving process involved as in the former case.

Finally, investigations into the performance of the multi-track 2D MAP joint detector decoder system under different ITI and density levels along track are undertaken. The performance of the two coded systems are simulated under different channel scenarios and analysed using the BER and FER plots vs SNR for all the systems. BER performance comparison of the coded and uncoded system is carried out to highlight the coding gain achieved due to the coding system.

6.2 System Model

Figure 6.1 and Figure 6.2 depict the block diagrams of the systems under study using the two parity coding approaches. In Figure 6.1, the two parity bits are applied in the along track direction and are separated by a DRP interleaver. The information bits to be saved on the disk are first encoded by adding a single parity bit to the data and then interleaved using the DRP interleaving algorithm (see chapter 2&4 for DRP interleaver discussion). After interleaving, a second single parity bit is added to the interleaved data before passing to the SMR channel.

Note that, all the two parity bits used here are applied along track direction only as shown in Figure 6.1. The data bits are recorded on the media using the shingle write magnetic recording technology. The same SMR channel model developed in chapter 5 is adopted in this chapter for the SMR channel implementation. See chapter 5 for SMR channel model and implementation.

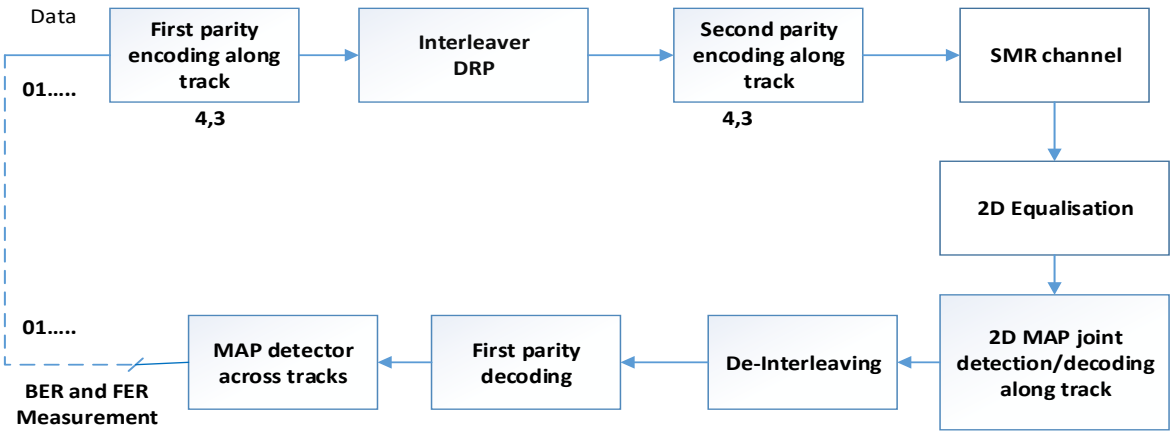


Figure 6.1: 2D multi-track MAP joint detector decoder with parity bits along track only.

After passing the data into the channel, the data output from the channel is equalised along track before passing into the 2D multi-track MAP detector for joint detection and second single parity decoding. The decoded parity bits are removed and the APP probabilities representing the symbol on the main track and the interfering track are de-interleaved. The resulting APPs are passed through a single parity bit 2D MAP decoder to decode the first parity bit. The decoder produces results with ITI from other tracks. Finally, another MAP detector is used across tracks to get the information bits out of ITI. Alternatively, the ITI detector across track can be implemented before the first parity decoding as used in (Greaves, Muraoka and Kanai, 2008). That means the first parity bit decoder would be 1D MAP decoder if the ITI has been removed from the data before decoding. Both procedures give same results.

Figure 6.2 shows the system block diagram of the scheme when both parity bits are used in along track and across track directions unlike using them in one direction as in Figure 6.1. First a single parity bit is added to the information bits along track to produce a code constraint along

track, and then another single parity bit is added across tracks to give the constraint across tracks. The resulting coded data is then passed onto the SMR channel for recording. Data read from the channel is equalised and passed to the multi-track 2D MAP detector decoder for joint detection and single parity coding along track. The decoded parity bits along track are then removed and the resulting APP probabilities now with ITI are passed to the detector across tracks for ITI cancellation. A 1D MAP decoder is used across track to decode the parity bit across track and output the final decoded information bits across track.

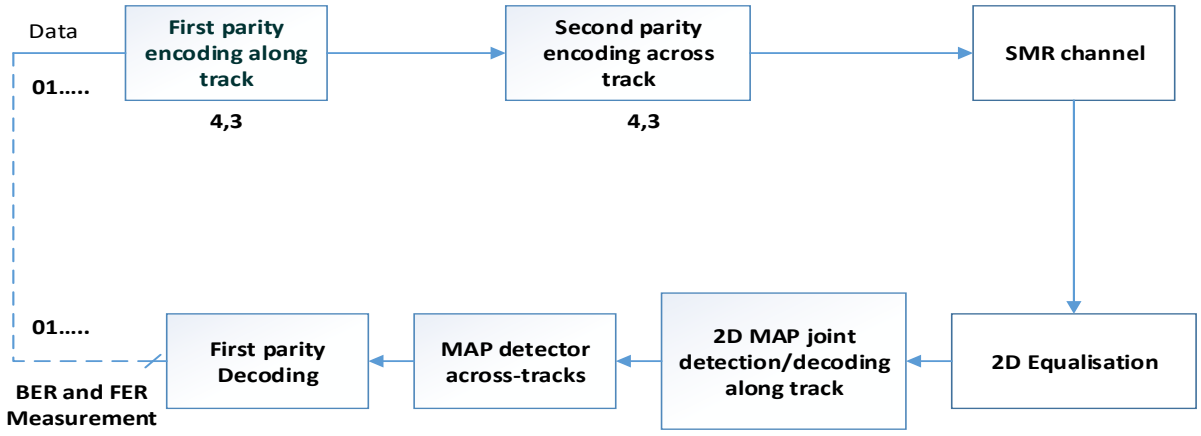


Figure 6.2: 2D multi-track MAP joint detector decoder with parity bits along and across track.

6.3 Parity Bits Along track

In the first implementation (see Figure 6.1), an odd parity bit is added to a data of length 3 bits to form a single parity code with even parity-check constraint along track. A total of 2304 bit per track was initially generated before adding the first parity bit. This result in a total of 3072 bits per track after the first parities are added along track. The row of 3072 data bits is randomised using the DRP interleaver as implemented in section 4.2.2. The same procedure is followed in this section to interleave the coded data along track.

After interleaving, another single parity bit is added to a data block length of 3 along track again, using odd parity check constraint. This produced a total of 4096 bits of data per track which will be recorded on the SMR media. The SMR channel used is the same as that proposed in chapter 5 (see section 5.2 for the SMR/TDMR channel modelling and implementation). Data output from the SMR channel is equalised along track before being passed to the 2D multi-track joint detector decoder used along track, which detects the signal by removing the ISI while performing parity bit decoding at the same instance. Once the decoded parity bits are removed, the resulting 3072 row length of APPs representing the probabilities of receiving all possible adjacent bits across tracks are re-arranged back to the original data bits positions using the DRP de-interleaver. A single parity bit 2D MAP decoder is then used to decode the first parity bit and the decoded parities are subsequently removed. The result is now a 1D data with ITI from adjacent track and the total data bits per track reduced is reduced to 2304. This is equal to initial number of data bits per track before any parity bit addition. Finally, a regular MAP detector is used across tracks to detect the information out of ITI.

6.4 Parity Bits Along and Across Tracks

In the second implementation (see Figure 6.2), an odd parity bit is first added to data length 3 bits along track to form the single parity check code along track. The total data bits per track were initially 3074 bits before the first parity bits are added along track. After adding the first parities, a second parity bit is then added across tracks using the same odd single parity check constraint to form the single parity code across tracks. No interleaver is needed here because the single parity codes are used in the different directions, unlike in the first case where the single parity codes are used in the same direction (along track only). Initially, the number of tracks on the sector was 6 before adding the second parity bit across track. When the parity bits are added across tracks, the total number of tracks of the sector now becomes 8. A sector of the

SMR channel model used in this work has 8 tracks and 4096 bits per track as earlier stated in chapter 4 and 5.

When all the parity bits are added in both directions, the coded data is passed to the SMR channel for data recording on the media. Shingled write-magnetic recording technique is employed to write the data on the magnetic media. The readback data from the SMR channel is first equalised along track before being passed to the Multi-track 2D MAP joint detector decoder for joint detection and single parity decoding. The decoded parity bits are then removed, and the APPs of the detected bits are passed to the MAP detector across tracks for ITI cancellation. A single parity MAP decoder is applied across track to decode the single parity bits across tracks and outputted the final information bits across tracks.

6.5 2D MAP for Joint Signal Detection and Decoding

BCJR algorithm is run on a single trellis to perform joint detection and parity decoding of the equalised signal from the SMR channel. In this implementation, the SMR channel model is considered to have ITI of two tracks, meaning that ITI contribution is from the main track and the side track. Due to the nature of the code used (code length 4); a target length of at least 4 is needed in order to perform joint detection and decoding of the parity bit from the equalised data. Therefore, our multi-track 2D MAP joint detector-decoder will have a trellis with 64 ($2^{3\times2}$) states and 4 (2^2) incoming and outgoing branches per state. Figure 6.2 depicts the trellis structure of the multi-track 2D MAP joint detector decoder proposed in this work.

The parity bit added to the data modifies the detector/decoder trellis such that, at the point where the parity bit enters the signal, the parity bit constraint reduces the number of branches from 4 per state to 1 branch per state in order to satisfy the parity check equation. This is because only

branches whose branch transition symbols satisfy the parity check equation are valid and selected at that instance.

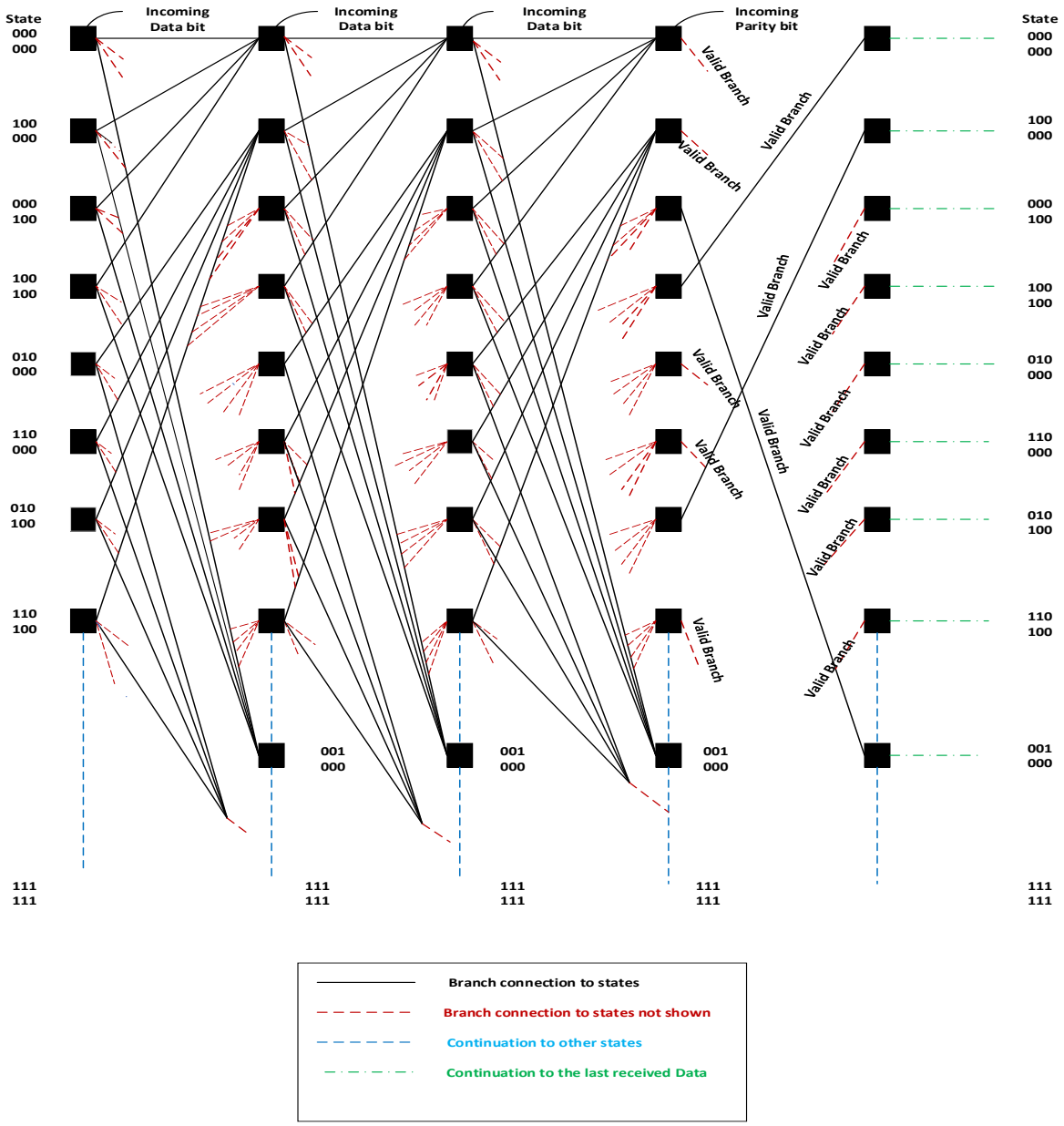


Figure 6.3: Trellis diagram of the 2D multi-track MAP joint detector decoder with two-track ITI.

As depicted by the Figure 6.3, the incoming parity of the signal corresponds to the bit at every fourth transition point of the trellis. For instance, it can be seen that at the fourth transition the only valid transition from state $\begin{matrix}100\\100\end{matrix}$ is to state $\begin{matrix}000\\000\end{matrix}$. This means the component bits of the valid branch are $\begin{matrix}1000\\1000\end{matrix}$, which satisfy the odd parity check equation. The transition from $\begin{matrix}000\\000\end{matrix}$

to $\begin{matrix}000\\000\end{matrix}$ is not valid because, the branch component bits is $\begin{matrix}0000\\0000\end{matrix}$, which do not satisfy the odd parity check equation. The APP probabilities of 00, 01, 10 and 11 are determined as the output of the multi-track 2D MAP joint detector decoder. This presents a convolved soft information data across tracks with ITI from the side track. The decoded parity bits are then removed, de-interleaved and saved for the remaining signal processing process to be described in the next sections.

6.6 Across Track ITI Cancellation

In the first scenario implementation as shown in Figure 6.1, where both parity bits are used along track separated by the DRP interleaver, the across track MAP detector is employed after de-interleaving and decoding of the first parity bits. The decoder across track used saved the APP probabilities of 00, 01, 10, and 11 as its branch metric for computation. This APPs represents the received convoluted data across tracks with ITI from the side track. The detector runs the BCJR algorithm on a 2-state trellis with total of 4 branch transitions (2 branches per state) given by the saved APPs. The APP of the received bit being either 0 or 1 is determined to detect the data out of ITI to get the final information bits across tracks.

However, for the second implementation as shown in Figure 6.2 which uses one parity bit along track and the other one across tracks, the across track MAP detector is employed immediately after the multi-track 2D MAP joint detector decoder. The output of the multi-track 2D MAP joint detector decoder (APP of 00, 01, 10, and 11) is fed into the across track MAP detector and is used by the detector as branch metrics. The detector across track removes the ITI from the data and the output is passed to the MAP decoder across track to decode the parity bits used across tracks. The same trellis structure is used for across track MAP detector in both the first and second scenario implementation.

6.7 Decoding of First Parity Bit

In the scheme of Figure 6.1, the first parity bits along track are decoded after de-interleaving the output of the multi-track 2D MAP detector decoder. The convolved output as mentioned earlier is the APP probabilities of 00, 01, 10, and 11, representing the received data on the main track with ITI of the side track. These probabilities are then used in the single parity 2D MAP decoder along track, by utilising the first applied parities, which are decoded last. In implementing this decoder, the probabilities of any four blocks of 2D convolved data are multiplied according to the valid sequence, considering the odd parity-check constraint. For example, the probability of sequence $\begin{array}{|c|c|c|c|}\hline 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ \hline \end{array}$ is found by multiplying the APP[11] for the first, APP[00] for the second, third and fourth bit. The probability of $\begin{array}{|c|c|c|c|}\hline 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 \\ \hline \end{array}$ is found by multiplying the APP[00] for the first, and the APP[11] for second, third and fourth bit. This continues until all the probabilities of the four-bit combination satisfying the odd parity equation are determined. There are 64 valid sequence combinations in this implementation that satisfied the odd parity check constraint for the two track ITI model. After computing the probabilities of the valid four-bit combinations, the probability of the first bits being 00 (APP[00] at the first bit position) is determined by adding the probability of sequences having 00 as first bit and dividing it with the total probabilities of all valid sequence. The same goes for 01, 10 and 11, and all the other bit positions second and third. The fourth bit position is the parity bit and is therefore ignored. This process is applied all through the data up to the end. When all tracks are processed, the parity bits are discarded and the new APPs (APP[00], APP[01], APP[10] and APP[11]) serving as the data are saved for used by across track BCJR detector for ITI cancellation.

However, in the second implementation (Figure 6.2), a single parity 1D MAP decoder is used across track to decode the first parity bits in the data. The output of the MAP ITI detector is

passed to the decoder for decoding the parity bits. The MAP detector across track produced a soft information output which gives the APP of the detected bit being either 1 or 0. This APP is used by the decoder as data input to decode the parity bit. The 1D MAP decoder operates on the same principle described in section 4.2.9, but this time the possible data sequences are arranged according to odd parity check constraint. That is to say, the valid data sequences are 0001, 0010, 0100, 0111, 1000, 1011, 1101 and 1110.

6.8 Results and Discussions

In this section, we are going to present the performance of the 2D multi-track MAP joint detector decoder with the coding configurations giving by Figure 6.1 and Figure 6.2. The BER results obtained through computer simulation are used to analyse and compare the performance of the 2D multi-track MAP joint detector decoder to the uncoded 2D multi-track MAP detector presented earlier in chapter 5.

Finally, performance comparison of the two coding implementation of the 2D multi-track MAP joint detector decoder is undertaken to determine the scheme with the best performance under different varying channel conditions.

6.8.1 Parity bits along track with DRP interleaver

Figure 6.4 shows the performance of the multi-track 2D MAP joint detector decoder coded using both parity bits along track separated by DRP interleaver ("coded" as indicated in plot) and multi-track 2D MAP detector without coding ("uncoded" as indicated in plot). The ITI level is set 100% for both tracks (ITI [1.0 1.0]) with density varied along track for values of $T_{50} = 1.0$, $T_{50} = 1.5$, and $T_{50} = 2.0$. As expected, there is performance degradation in both systems (coded and uncoded) as the density along track increases due to increase in ISI present in the

system. The coded scheme has a gain of about 2.5 dB to 4.5 dB over uncoded scheme at densities of $T_{50} = 1.0/T_{50} = 1.5$ and $T_{50} = 2.0$ respectively. It is observed that the coding gain is more significant at high ISI ($T_{50} = 2.0$). This can be attributed to the fact that the DRP interleaver is able to provide good symbol spreading, thereby minimising the ISI effect at high density.

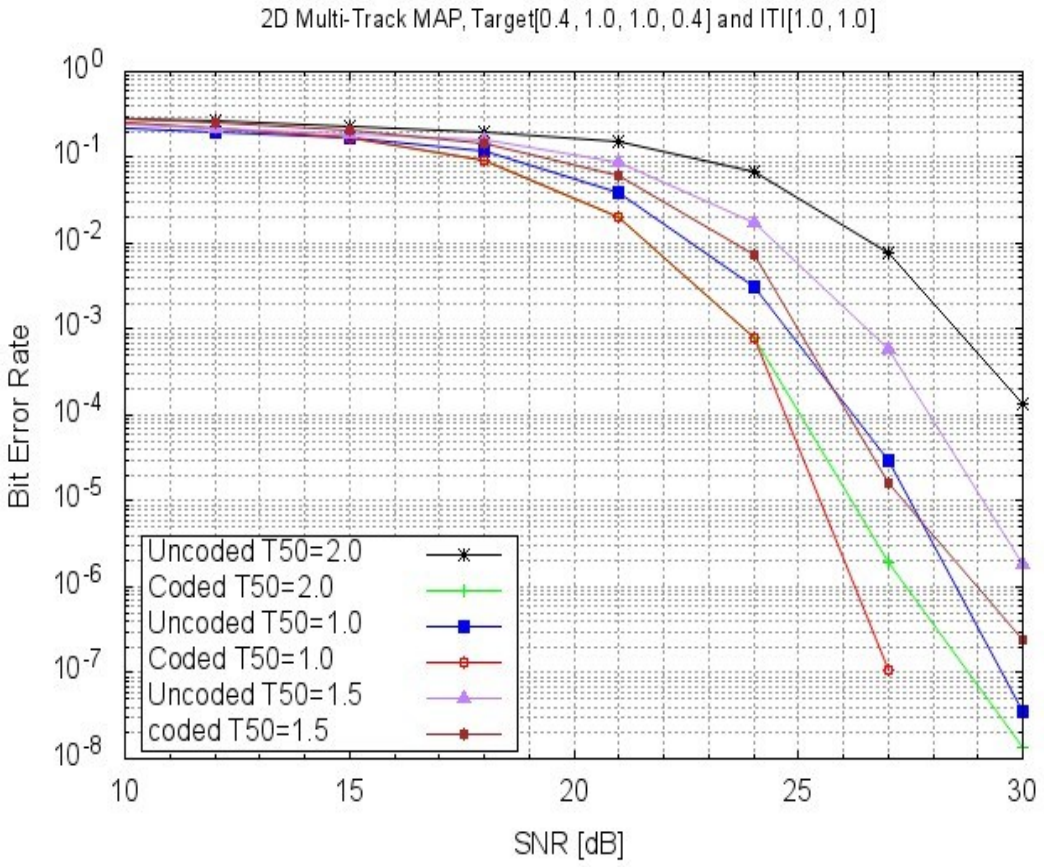


Figure 6.4: Performance comparison of different T_{50} values at ITI [1.0 1.0].

Figures 6.5, 6.6 and 6.7 show the performance of the coded and uncoded schemes at densities of $T_{50} = 1.0$, $T_{50} = 1.5$, and $T_{50} = 2.0$ respectively with varying ITI levels. The ITI level here is a function of the Read head width or size. That is to say, the wider the Read head, the more the signal captured from the interfering side track and the higher the ITI.

Figure 6.5 shows that the performance of both schemes is at the best when the ITI level is high (ITI [1.0 1.0]). This is partly attributed to the advantage of high minimum separation between symbols inherent to the ITI [1.0 1.0] compared to the other ITIs as explained in the previous chapter (Chapter 5; section 5.5).

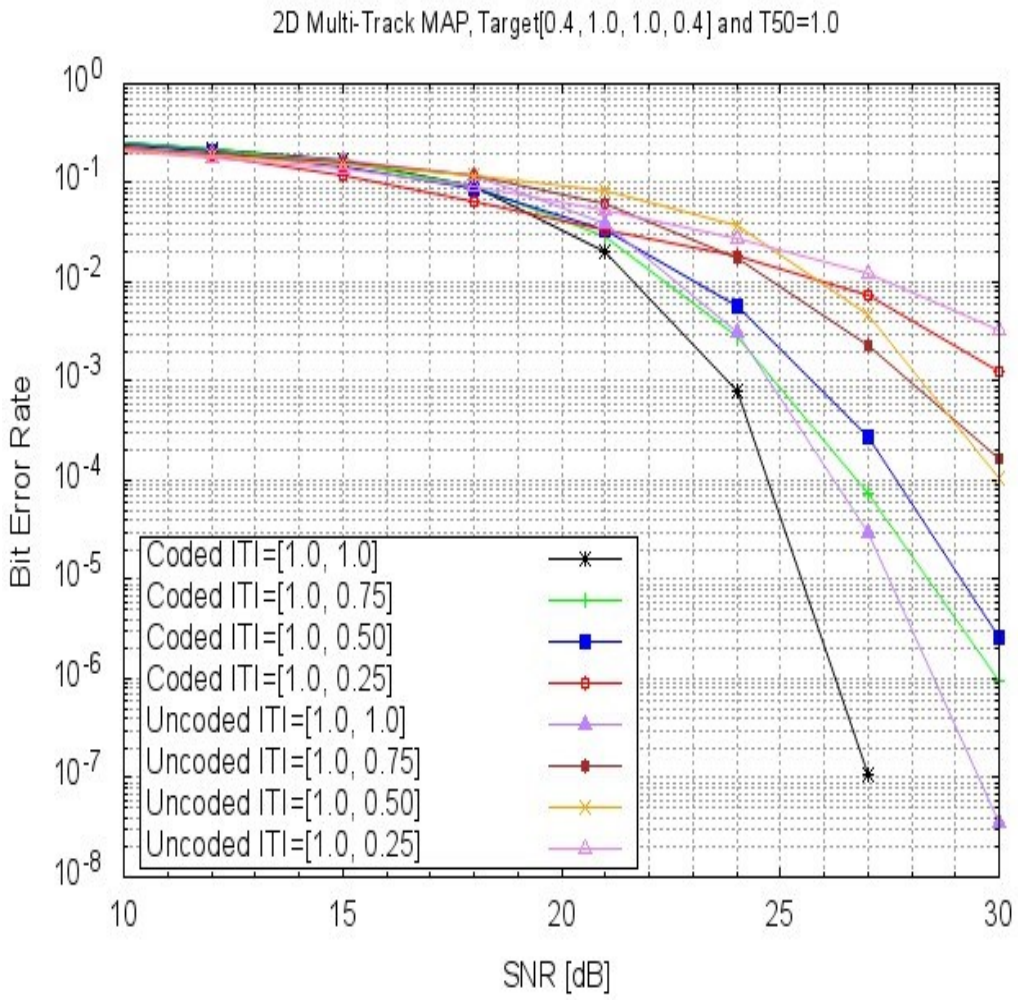


Figure 6.5: Performance comparison of different ITI levels at $T_{50} = 1.0$.

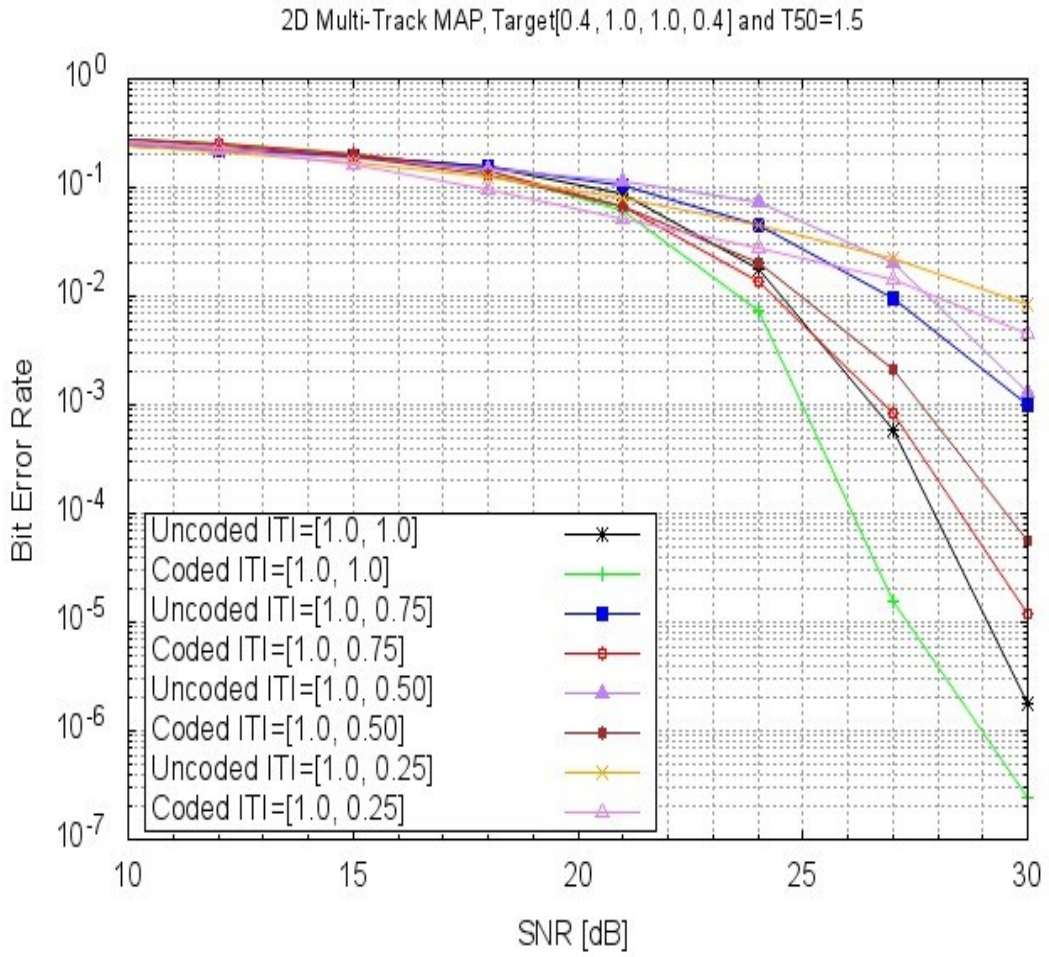


Figure 6.6: Performance comparison of different ITI levels at $T_{50} = 1.5$.

It is also observed that coding gain observed is low at low ITI [1.0 0.25] which is less than 1.5 dB compared to what was obtained at higher ITIs of [1.0 0.50], [1.0 0.75] and [1.0 1.0], which averages around 3 dB. Similar trend is observed in Figure 6.6 at density of $T_{50} = 1.5$, when the ISI is moderate. But as ISI increases, the performance of the coded scheme improves, and the highest coding gain is achieved when the ITI is 100% of the side track. The gain is around 4.5 dB to 5 dB at $T_{50} = 2.0$ for ITI [1.0 1.0] compared to the 3 dB of $T_{50} = 1.0$ and $T_{50} = 1.5$ for the same ITI. The other ITIs shows relatively lower gain compared to ITI [1.0 1.0] as shown in Figure 6.7.

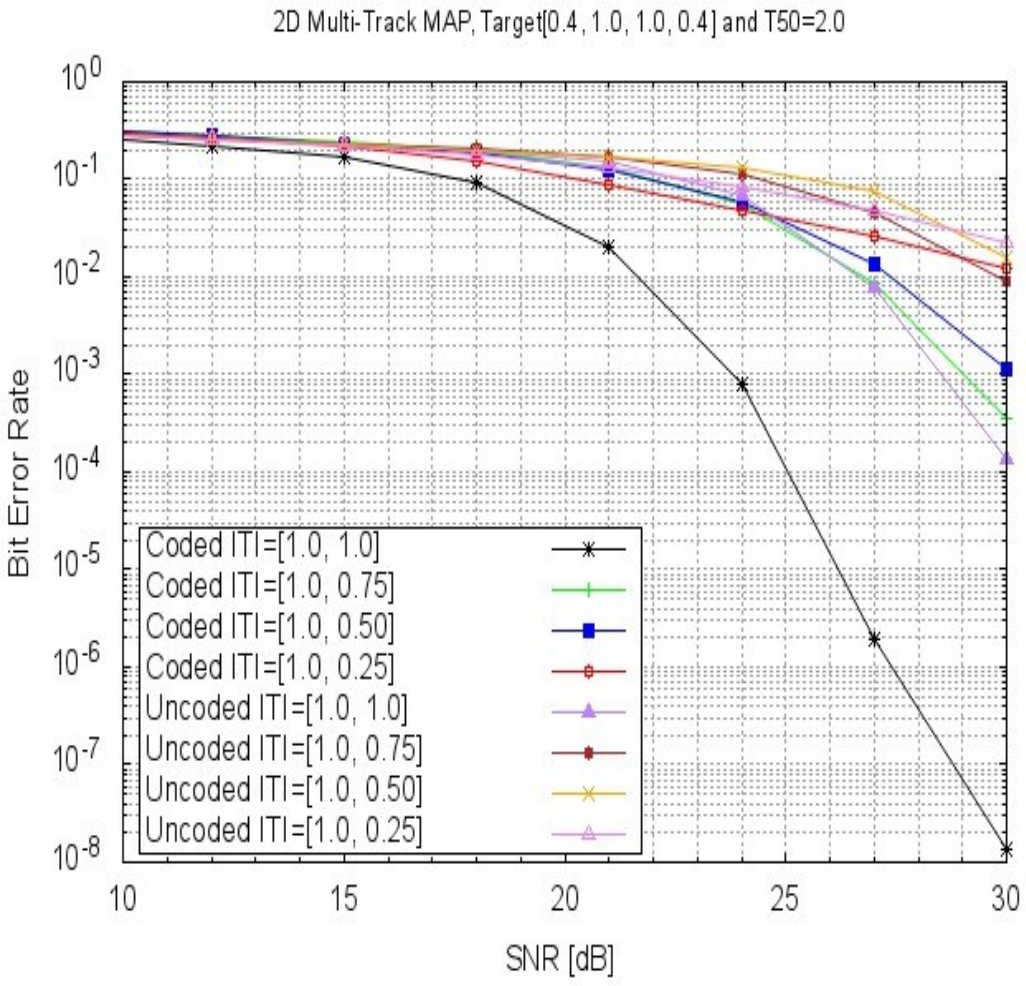


Figure 6.7: Performance comparison of different ITI levels at $T_{50} = 2.0$.

6.8.2 Parity bits along track and across track

In this implementation, the 2D multi-track MAP joint detector decoder system is coded with parity bits applied both along track and across track without using the DRP interleaver. This in effect reduced the additional complexity incurred on the system due to interleaving and de-interleaving processes and also improve performance under certain channel conditions. The simulation results obtained using this coding scheme under various channel conditions are presented below.

Figure 6.8 shows the performances of the coded joint detector decoder with parities on both directions and the uncoded detector at $T_{50} = 1.0$ (low ISI) with varying ITI levels. In this low ISI condition, the coding gain is highest when the ITI is low (ITI [1.0 0.25]) which is about 6 dB in gain over the uncoded system.

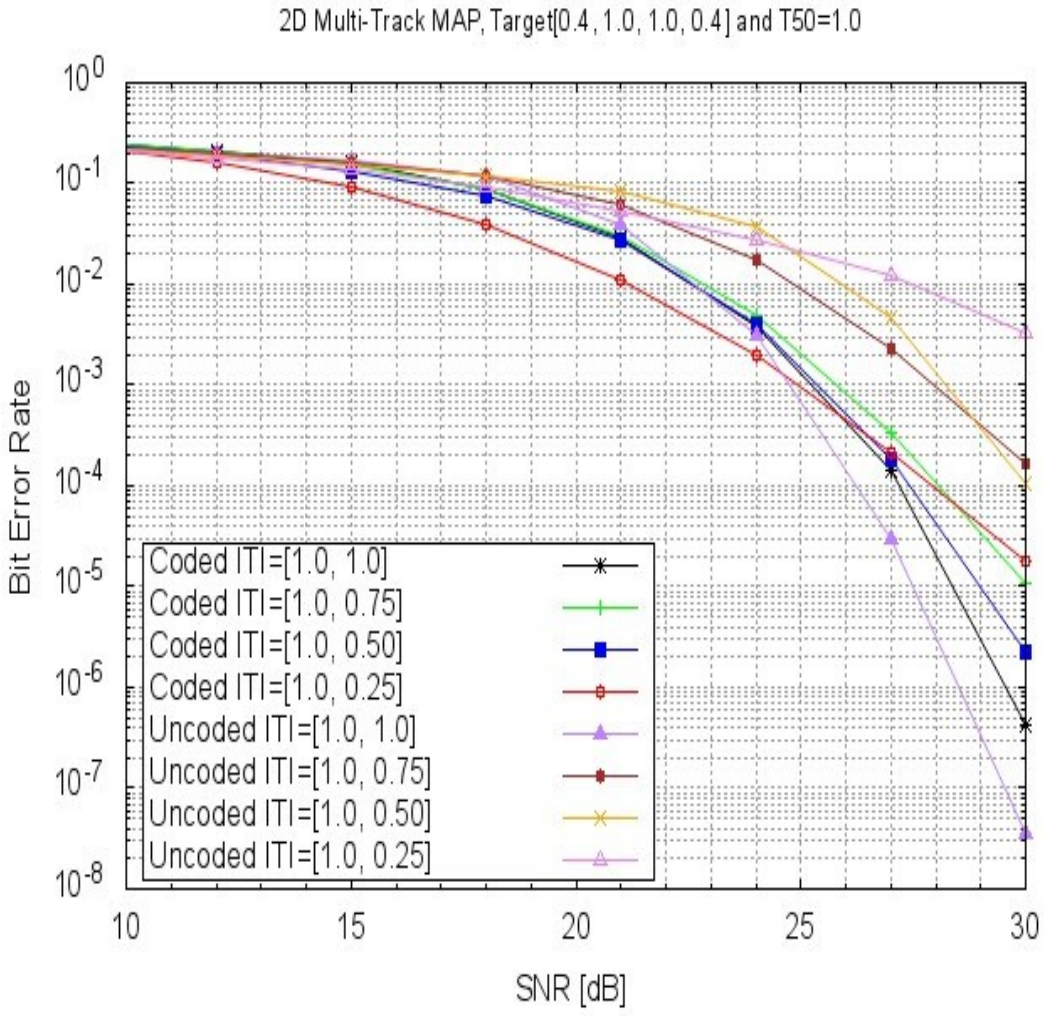


Figure 6.8: BER performance comparison of different ITI levels at $T_{50} = 1.0$.

There is no gain in performance over the uncoded system when the ITI is high (ITI [1.0 1.0]) in this situation of low ISI. In fact, a negative gain in coding is achieved as the performance without coding is much better. This can be attributed due to the fact that joint detection-decoding is performed along track which leaves the detector across track weakened by not

exploiting the parity bit applied across track. Interchanging the joint detector-decoder direction to across track may strengthen the detector across track and improve the system performance. This is suggested as a direction for future work. However, ITI [1.0 0.75] and ITI [1.0 0.50] have moderate gain of 2 dB and 3 dB compared to the uncoded system.

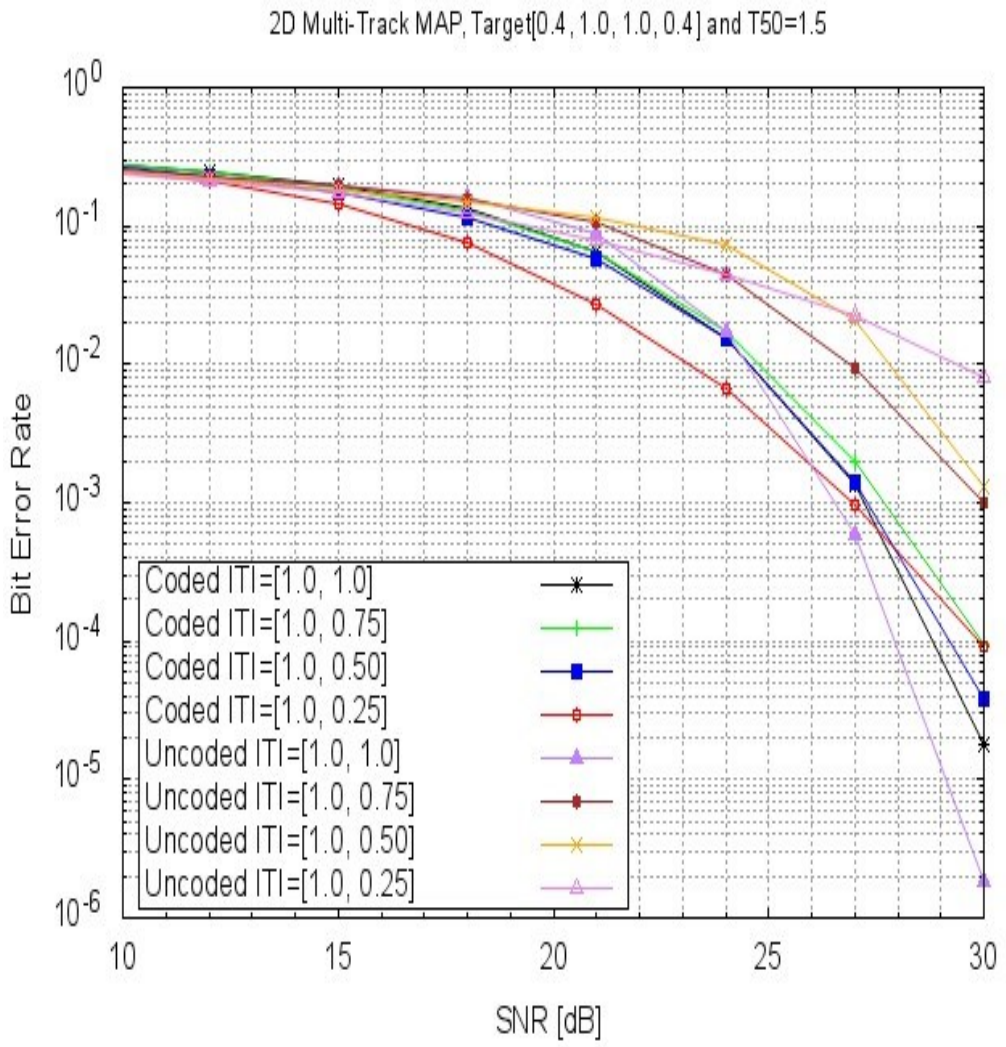


Figure 6.9: BER performance of different ITI levels at $T_{50} = 1.5$.

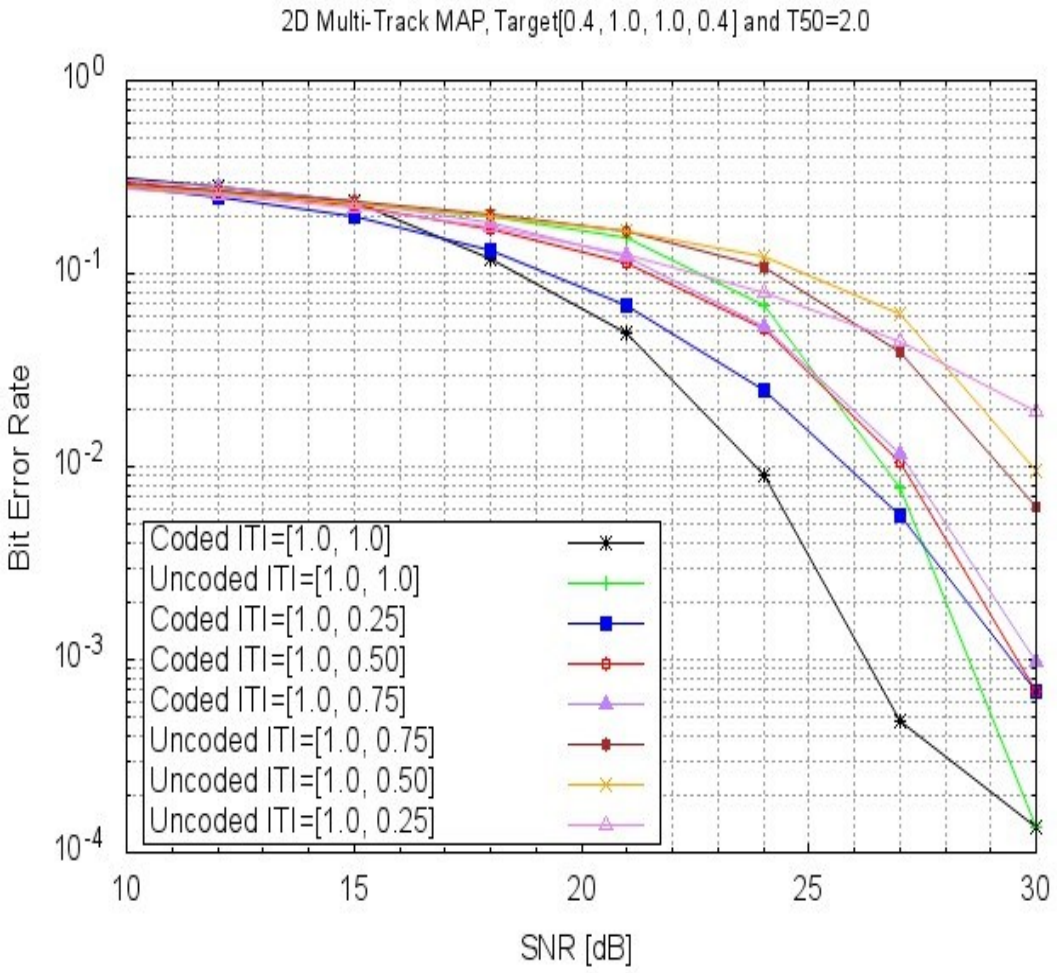


Figure 6.10: BER performance comparison of different ITI levels at $T_{50} = 2.0$.

Similar performances and gains are observed at $T_{50} = 1.5$ for all the ITI levels as shown in Figure 6.9. However, when the ISI is high ($T_{50} = 2.0$), the coded system with ITI [1.0 1.0] has the best performance of all as shown in Figure 6.10. The coding gain is improved to a level of about 3 dB (at BER point 10^{-3}) for ITI [1.0 1.0] at $T_{50} = 2.0$ compared to the negative observed at $T_{50} = 1.0$ and $T_{50} = 1.5$. But this gain in performance diminishes at the end with high SNR values due to effect of error floor in the system at SNR values above 27 dB.

In Figure 6.11, the performances of the coded scheme using parity bits on both directions without DRP interleaver and the uncoded scheme at ITI [1.0 1.0] with varying densities (different T_{50} values) is shown. It is seen that at low ISI ($T_{50} = 1.0$), the coding gain is negative.

But as ISI increases ($T_{50} > 1.5$), the coding gain begins to improve and is about 3 dB for $T_{50} = 2.0$ at BER point 10^{-3}. However, the gain in performance of the coded system diminishes at higher SNR above 27 dB due to error floor. The error could be avoided if the direction of the joint detector-decoder is interchanged. Meaning, after equalisation, joint detection-decoding should be done first across tracks to cancel ITI then followed by detection along track to cancel ISI not the other way presented here. This is suggested as a future work.

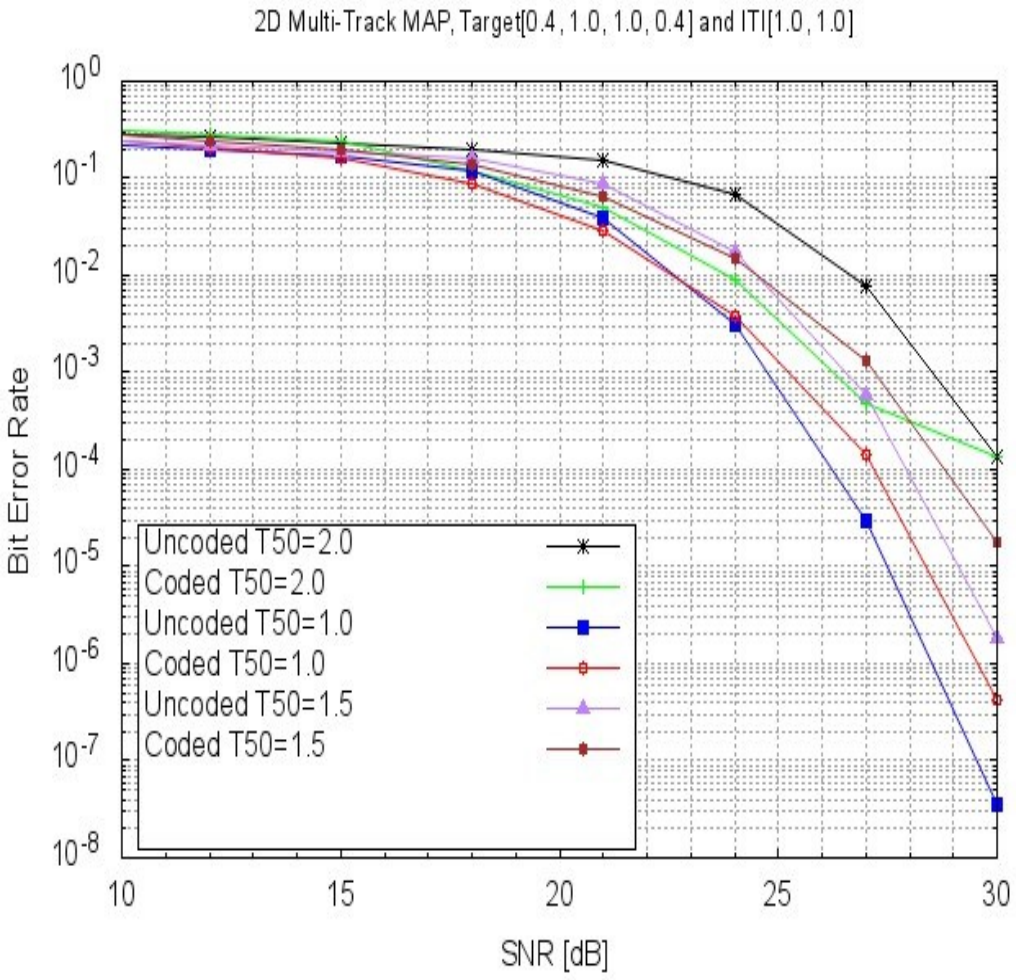


Figure 6.11: BER performance comparison of different T_{50} values at ITI [1.0 1.0].

6.8.3 Comparison of Single Parity Coding Schemes

The aim of parity coding is to improve the performance of the system by detecting and possibly correcting any form of error introduced into the system. A comparison of the two parity coding approach use for the implementation of the multi-track 2D MAP joint detector decoder developed in this research is presented as follows.

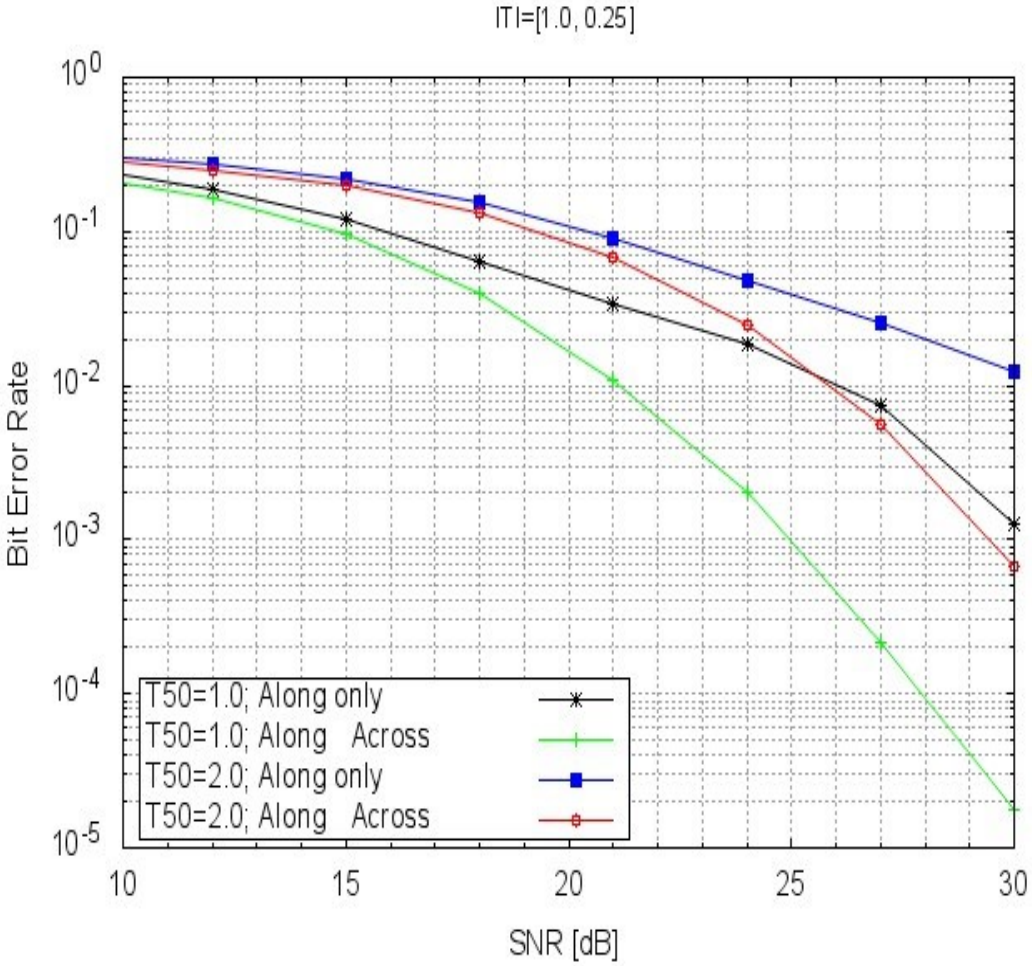


Figure 6.12: Comparison of joint detector decoder parity schemes at ITI [1.0 0.25].

Figure 6.12 shows the performance of joint detector decoder with parity bits along track only separated by DRP interleaver, and joint detector decoder using parity bits in both along track and across tracks without DRP interleaver. The ITI is low (ITI [1.0. 0.25]) for data densities of

$T_{50} = 1.0$ and $T_{50} = 2.0$ along track. The results show that for low ITI, the joint detector decoder with parity coding both along and across track outperformed that with parity coding along track only at both low and high ISI. Applying the parity bits both along and across track provides a gain about 5 dB and 4 dB for low ISI and high ISI respectively, over using the parity bits along track only separated by DRP interleaver at low ITI. Therefore, for low ITI, it is not beneficial to use joint detector decoder with parity bits along track separated by DRP interleaver, rather use the joint detector decoder with parity bits in both directions without DRP interleaver. This gives better performance in addition to reduction in system complexity as interleaving and de-interleaving stages of the DRP interleaver is avoided.

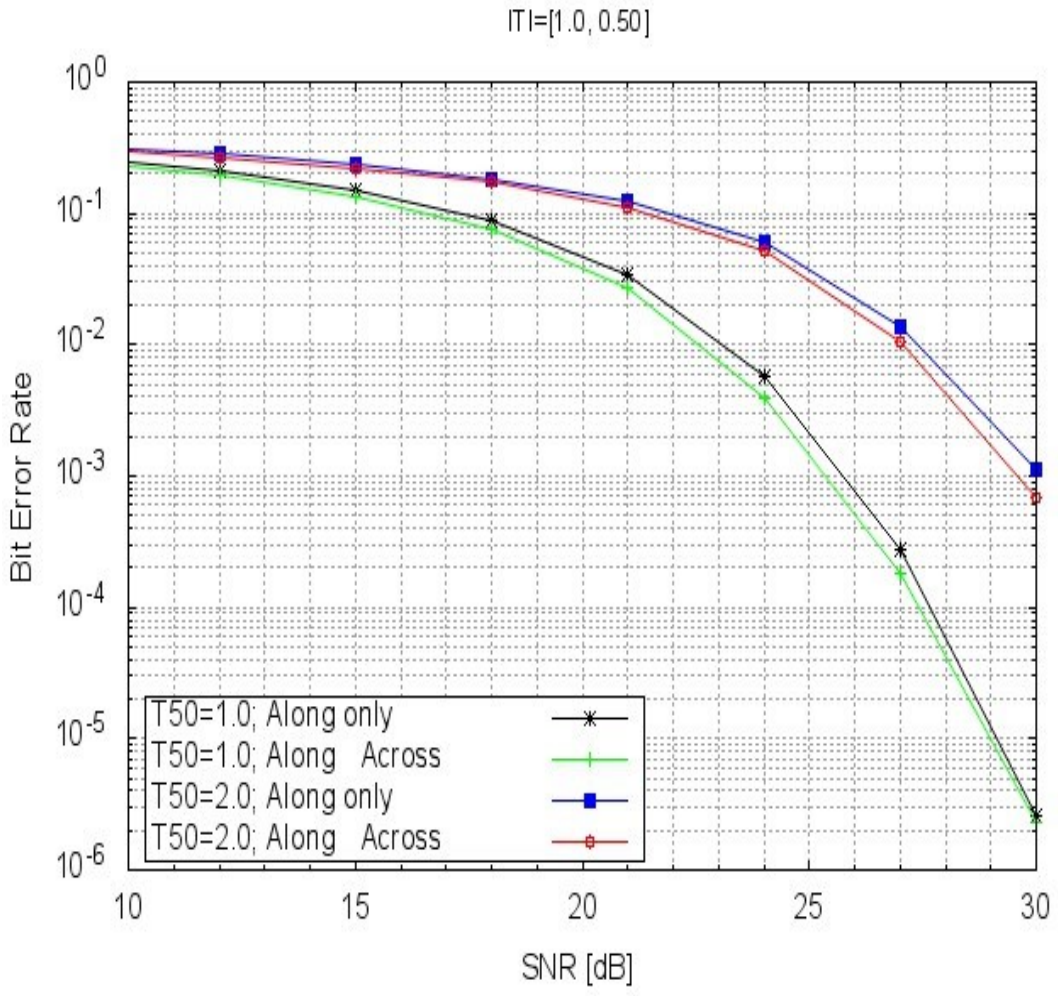


Figure 6.13: Comparison of joint detector decoder parity schemes at ITI [1.0 0.50].

However, when the ITI is increased to 50% of the side track ITI [1.0 0.50] (Figure 6.13), the performance of the joint detector decoder with parity bits along track only improves and closely matches that of parity bits both along track and across tracks. Still the latter outperformed the former slightly at high density ($T_{50} = 2.0$). Hence, it is not equally beneficial to use the both the parity bits along track only when ITI is [1.0 0.50] due to the same reason stated earlier.

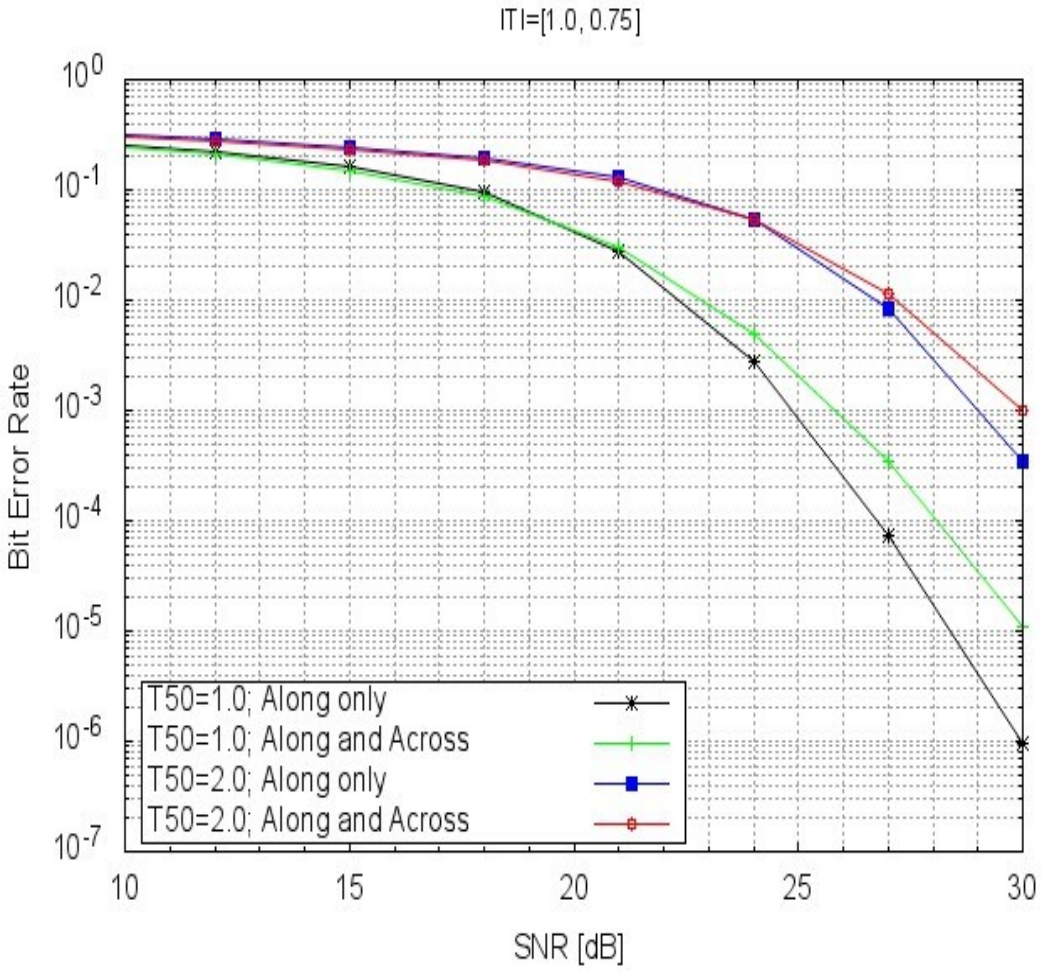


Figure 6.14: Comparison of joint detector decoder parity schemes at ITI [1.0 0.75].

Figure 6.14 shows the performance comparison of the two coded schemes when the ITI reaches 75% of the side track (ITI [1.0 0.75]). It is seen that in this situation, the joint detector decoder scheme with parity bits along track separated by DRP interleaver provides better performance than the scheme with parity bit applied along track and across tracks without DRP interleaver.

A gain of about 1.9 dB and 1 dB is achieved at $T_{50} = 2.0$ and $T_{50} = 1.0$ respectively when using the former over the latter. This means that it is beneficial to use parity bits in along track only separated by DRP interleaver when the ITI level is more than 50% of the side track.

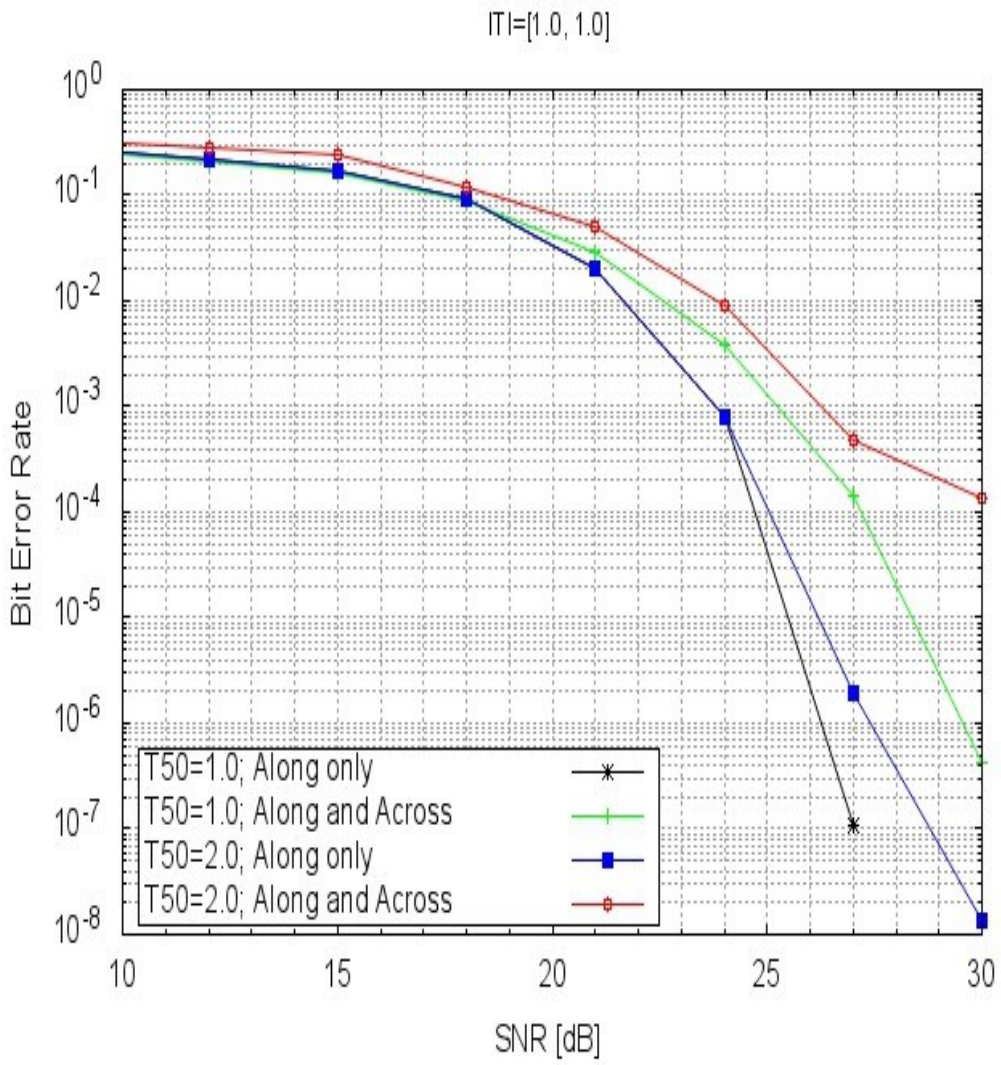


Figure 6.15: Comparison of joint detector decoder parity schemes at ITI [1.0 1.0].

Similar trend is also observed in Figure 6.15 as the ITI level is increased to 100% ITI of the side track (ITI [1.0 1.0]). The joint detector decoder with parity bits applied along track only performed better than the joint detector decoder scheme using parity bits along track and across tracks. The gain achieved by the detector decoder with parities along and across track over

along track only is higher, when ISI is high ($T_{50} = 2.0$) compared to low ISI ($T_{50} = 1.0$) regime as depicted by the figure. It was also observed that at high ITI and high ISI condition, the BER performance of the joint detector decoder floored at high SNR values.

A comparison of the performance of two coded based 2D joint detector decoder and uncoded 2D detector is shown, for various data densities, at full ITI (100% ITI of side track), in Figures 6.16, 6.17 and 6.18.

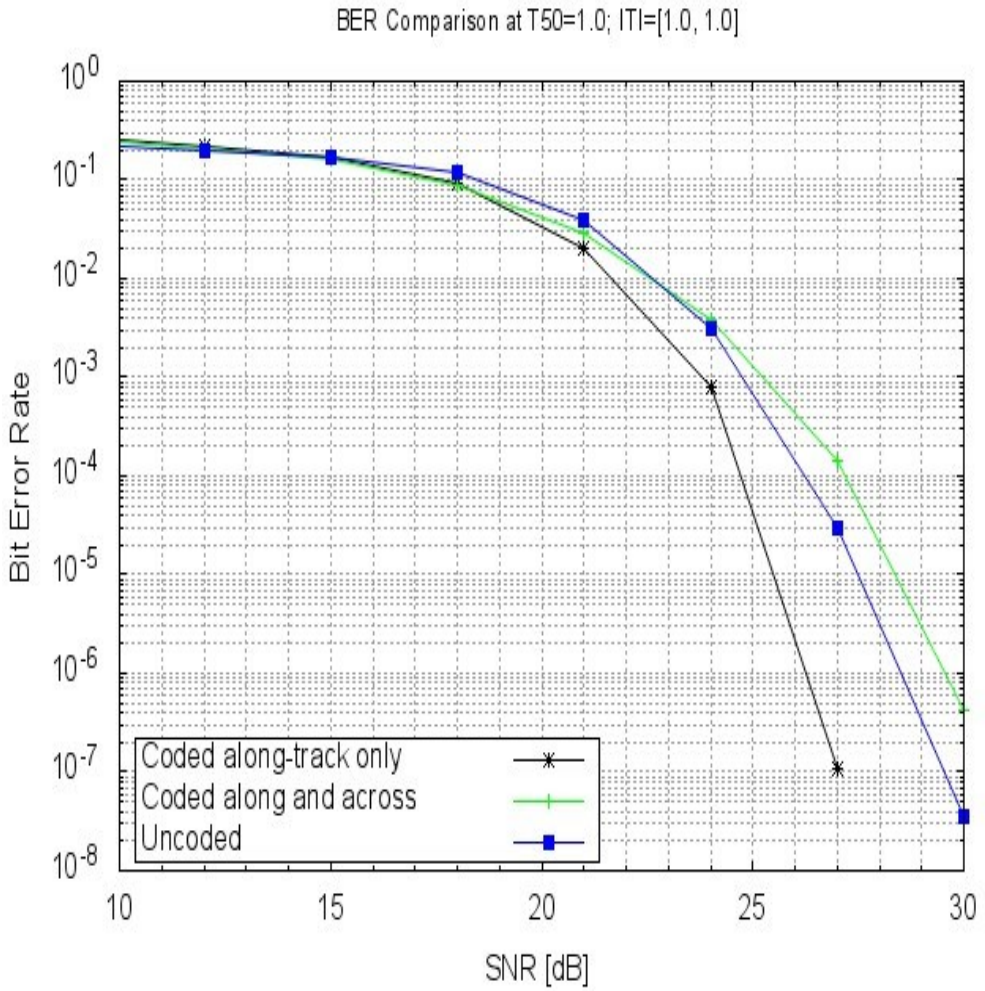


Figure 6.16: Comparison of the coded and un-coded system at $T_{50} = 1.0$, ITI [1.0 1.0].

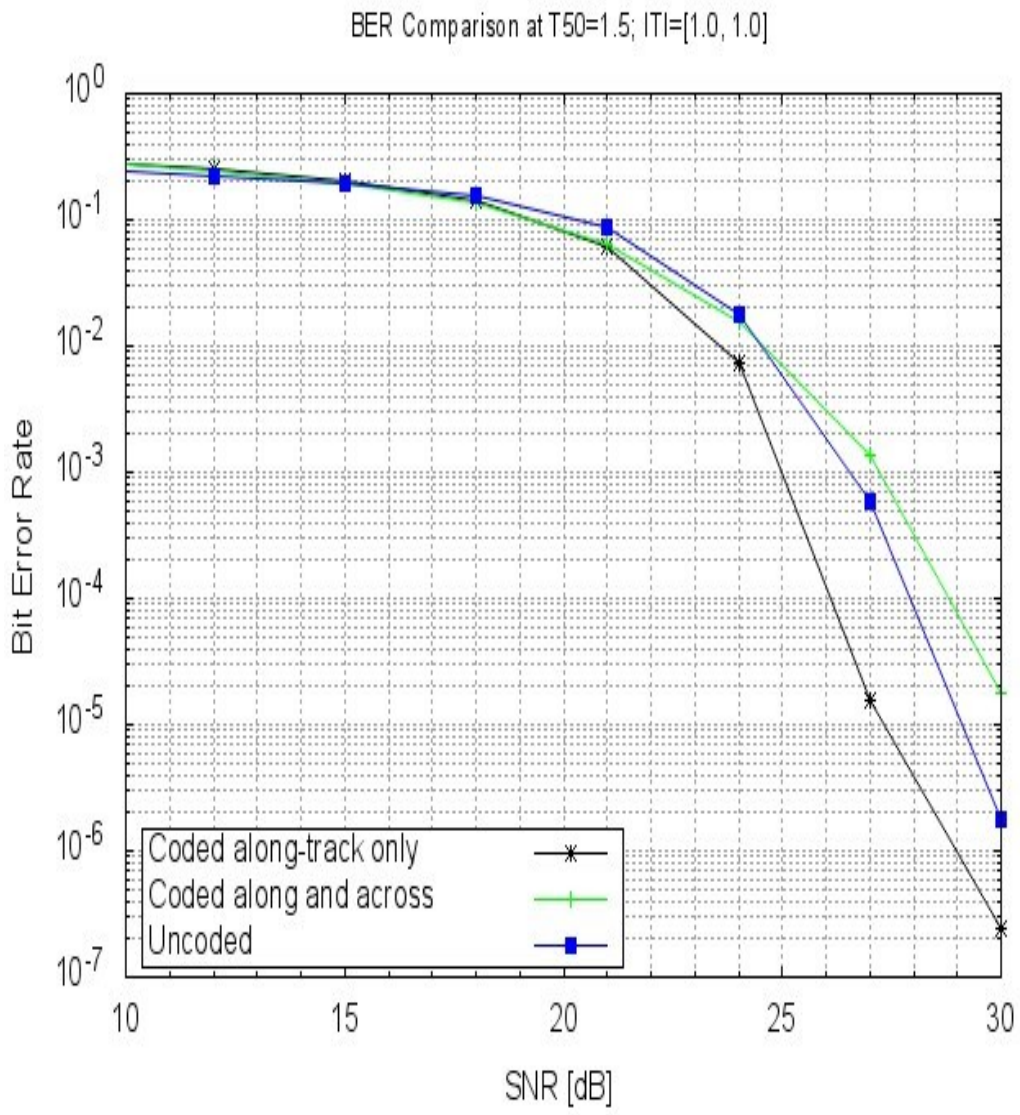


Figure 6.17: Comparison of the coded and un-coded system at $T_{50} = 1.5$, ITI [1.0 1.0].

It is seen that coded joint detector decoder with both parities along track only has the best performance. This can be attributed to the following factors. One, coding with parity check code generally improve the performance of the detector by preventing and correcting any form of error that occur in the system. This is obvious when we compare the performance of the coded system with the uncoded system.

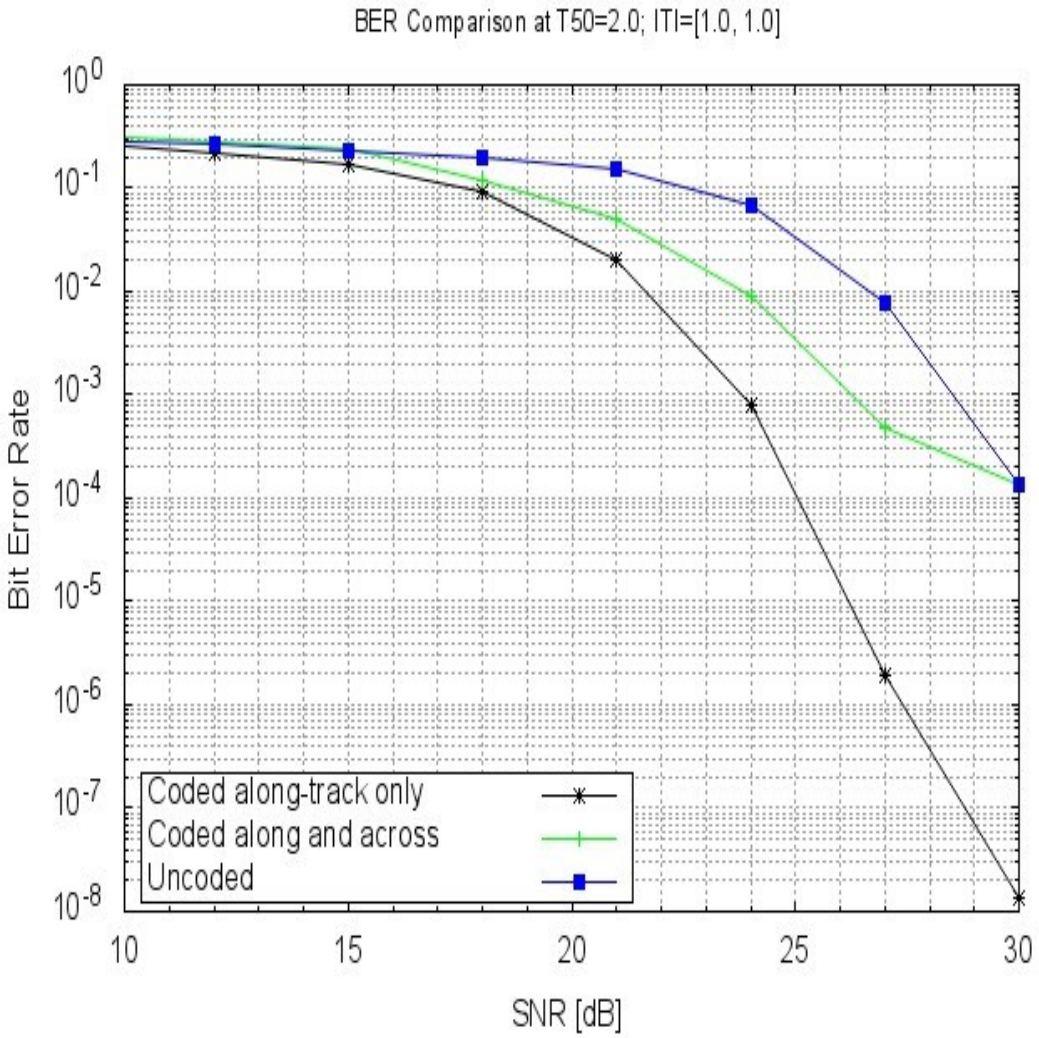


Figure 6.18: Comparison of the coded and un-coded system at $T_{50} = 2.0$, ITI [1.0 1.0].

The second factor is that for joint detector decoder with parities along track, the DRP interleaver placed in between the two parity bits provides adequate parity bit separation within the data at high data density. This randomised the noise and prevents localisation of burst errors, thereby improving the minimum distance between data and codeword. Whereas joint detector decoder with parities along track and across track, as implemented here, there is no interleaver separating the parity bits are placed in both directions.

The third factor is the fact that the 2D multi-track joint MAP detector decoder is implemented along track in both cases to start with ISI cancelation before applying the ITI detector across

track. This gives an added advantage of better performance when all the parity bits are placed along track.

The gain as seen from the Figures 6.16, 6.17 and 6.18 is between 2 dB to 3 dB in favour of the joint detector decoder with parities along track separated by DRP interleaver over that with parities in both along track and across tracks. However, this gain is achieved at the expense of an additional complexity and extra latency in the system. This comes from the interleaving and de-interleaving processes of the DRP interleaver applied between the parity bits along track.

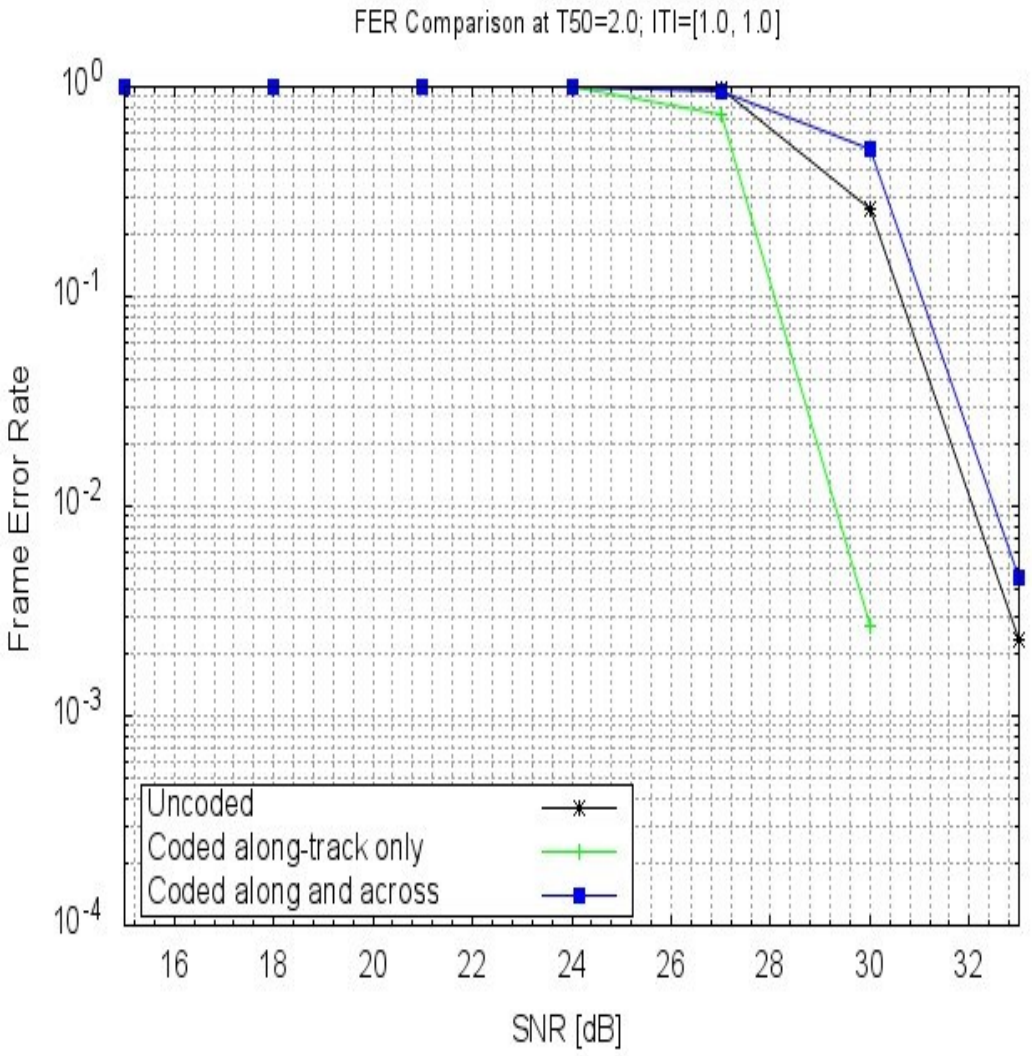


Figure 6.19: FER comparison of parity coding schemes at $T_{50} = 2.0$, ITI [1.0 1.0].

Further comparison of the joint detector decoder coding schemes is made by comparing the FER performances of the two coding schemes under various data density. Figures 6.18, 6.19 and 6.20 show the FER the scheme coded with parities along track only with DRP interleaver compared to scheme coded with parities both along and across tracks and the uncoded system. It is seen that the scheme coded with parities along track only with DRP has better performance compared to scheme coded with parities along and across tracks with reasonable margin. These results also concurred to what was presented earlier based on the BER comparison of the schemes.

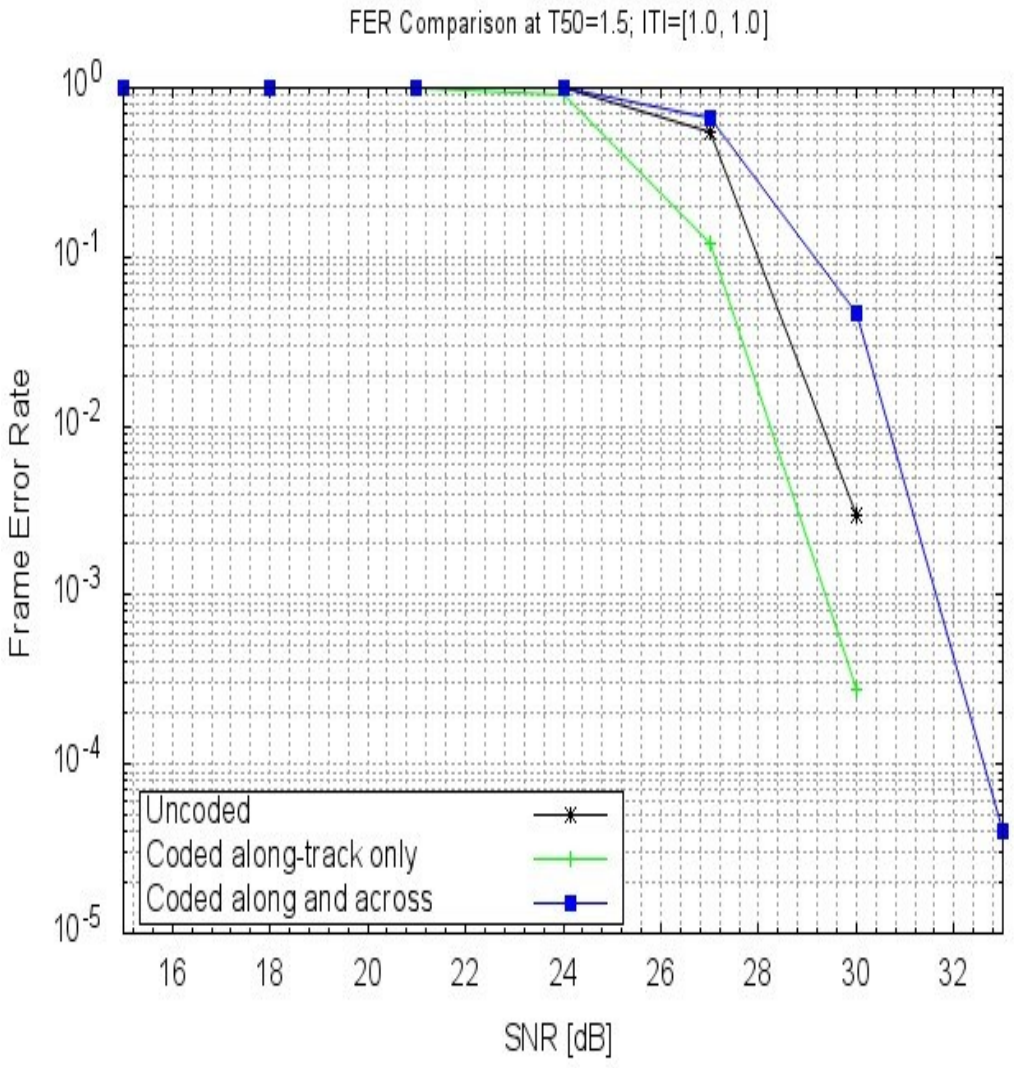


Figure 6.20: FER comparison of parity coding schemes at $T_{50} = 1.5$, ITI [1.0 1.0].

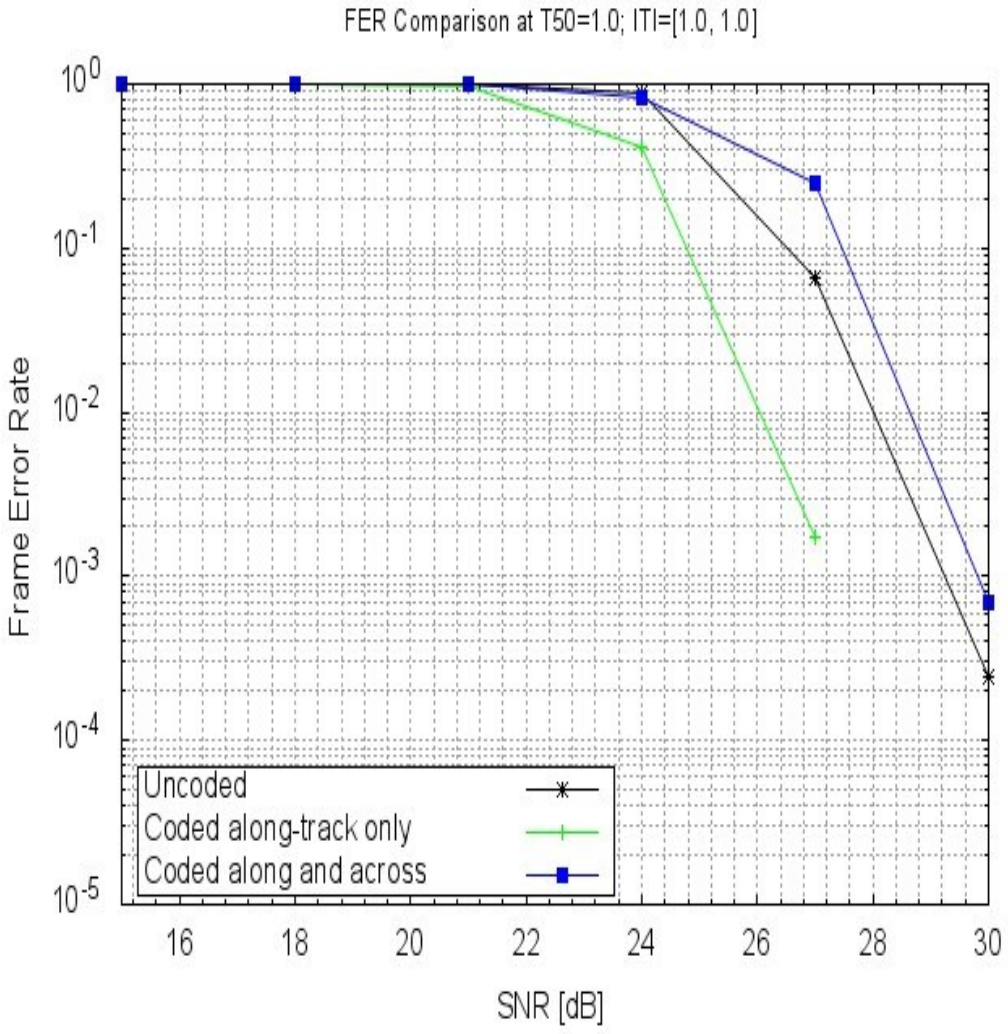


Figure 6.21: FER comparison of parity coding schemes at $T_{50} = 1.0$, ITI [1.0 1.0].

Table: 6.1 Summary of single parity coding schemes performance comparison.

	Along Track only		Along and across Tracks	
	Data density (T_{50})	Track density (ITI)	Data density (T_{50})	Track density (ITI)
LOW	Best	Worst	Best	Best
MEDIUM	Good	Good	Good	fair
HIGH	Worst	Best	Worst	worst

The summary of the comparison of the performances of the encoding schemes is given by Table 6.1. It can be therefore concluded that in general, coding with parity across and along track produce the best results in situation where there is low track density (ITI). This means that the across and along track scheme does not exploit the ITI gains. However, for channel having high track density (ITI), coding with parity bits along track only gives the best performance. The performance of the coding schemes generally decreases with increase in data density along track (T_{50}).

6.9 Summary

- The two single parity encoders used for the FEC system in this work have been developed. They are used to add two single parity check bit code to the data. The first encoder used two concatenated single parity-check codes along track separated by DRP interleaver. While the second encoder used the single parity-check code along track and across tracks direction without DRP interleaver.

- 2D multi-track MAP joint detector decoder for simultaneous signal detection and decoding of data along track has been developed and implemented. The 2D MAP detector was constrained along track to detect and decode the last parity bits. Implementation example of the 2D multi-track MAP joint detector decoder with the modified trellis diagram has been given.

- Single parity bit 2D MAP decoder and 1D MAP for decoding of first parity bits along track have been described in this chapter.

- Simulation performances of the 2D multi-track MAP joint detector decoder using the two single parity FEC encoders have been presented. The performances were investigated under various channel conditions.

- BER and FER performance comparisons have been presented for the system with FEC and without FEC. The comparison of the two coded FEC encoder schemes have also been given.

- It has been shown that by applying the single parity FEC system and using the 2D multi-track BCJR joint detector decoder, the performances of the TDMR channel can be improved with less detection and decoding complexity. A gain of about 5 dB is achieved using the proposed FEC system with 2D multi-track MAP joint detector decoder, over the uncoded 2D multi-track MAP detector system in TDMR channel with SMR media.

- For the two single parity FEC system encoders, the encoder using two concatenated single parity bit codes along track separated by DRP interleaver has a gain of about 3 dB compared to the FEC encoder system using single parity bit code along and across tracks without DRP interleaver.

Chapter 7

Summary, Conclusion and Recommendations for Future Work

7.1 Summary of Work done

The ever-increasing demand for high capacity data storage devices has approach the areal density limit of the current conventional magnetic media imposed by the superparamagnetic limit. In order to satisfy this demand and pushed the areal density growth of magnetic recording media beyond the current conventional limit, new technologies for future magnetic recording systems have been proposed. Among them are, EAMR, BPMR, SMR and TDMR.

SMR and TDMR are attractive propositions for achieving intermediate areal density growth expansion because they do not require any change from conventional media. They can easily be implemented on current magnetic media with modifications on write process and Read head. TDMR uses combination of SMR and 2D readback signal processing techniques to achieve an areal density of 10 Tb/in^2 (Wood et al., 2009). Using the shingled write process, data bits are written in overlapping shingles, by eliminating guard bands between tracks to squeeze data, such that part of the previously written bits are overwritten by the neighbouring bits written after them. This brings the data bits closer together and the interaction between them results in

severe interferences in both directions of across-tracks and along-track. The 2D interference nature of the TDMR/SMR system necessitates the need for advanced 2D signal processing techniques for coding, equalisation, detection and decoding in order to advance it large scale future deployment. Therefore, that is why this research is focused on the study, investigation and development of low complexity coding, equalisation, detection and decoding algorithms for the TDMR channel.

So far, the work undertaken includes the modelling of a PMR channel using the jitter noise model to mimic the recording medium. The PMR channel model incorporates 1D interference, jitter noise due to timing jitter and AWGN representing electronic noise, head noise and other noises. The channel model is implemented in software using C-programming codes.

PRML read system was investigated and implemented on the 1D PMR channel model as a mechanism for recovering the recorded data from the medium. This involves the design and implementation of PR equaliser used to shape the readback channel signal to a desired target response for detection. This helps to reduce the complexity of the detector needed to detect the data. GPR targets were selected for this task, since they do not filter out the low frequency component which is the useful signal in PMR channel.

1D PRML detectors are implemented using Viterbi algorithm and BCJR algorithm to detect the equalised data from the PMR channel. Their performances were verified through simulations carried out in C-programming environment and compared in terms of BER Vs SNR plot. Simulation results showed that the BCJR detector has a better performance in terms of BER compared to the VA detector which conforms to what has already been established in literatures.

In a bid to improve the performance of the PRML read system of the PMR media channel, single parity encoders and interleavers were developed and implemented. The encoders add two single parity bit systems to the user data by imposing a parity-check constraint on them. The first single parity bit code is based on even parity-check constraint while the second single parity bit code satisfied the odd parity-check constraint. The single parity-check code serves as an error correction code and RLL (0, 6) code. The two single parity code systems are separated by DRP or Matrix/Square interleaver. Interleavers are used here to provide adequate random spreading of neighbouring bits far from each other after the first parity bits detection in order to randomise the noise before detecting the second parity bits. This prevent the occurrence of error clusters and improves the minimum separation distance between bits. Also, the performance of the coded system with different interleaver configuration was investigated when data decoding was performed using MLSD or MAP decoding. A coding system with concatenated Matrix/Square-DRP interleaver was also developed to further improve the performance of the system. Three single parity bit systems were involved, with the first and second parity bits separated by Matrix/square interleaver, and the second and third parity bits are separated using DRP interleaver. The used of the constrained single parity-check bit simplifies the detection process by reducing the number of branches of the detector involve in the detection process. Concatenating more parity bits improves the performance of the system, although with some addition decoding overhead.

1D constrained MAP joint detector decoder was developed and implemented. The joint detector decoder was used to simultaneously detect data and decode parity bit with the two concatenated single parity bit systems separated by an interleaver. It does so by selecting the branch transition whose branch symbols satisfied the parity-check equation at the point where the parity bit enters the equalised signal. The resulting data from the joint detector decoder output was de-interleaved, the decoded last parity bits removed and then MAP or MLSD

decoder is used to decode inner (first) parity bits to get final data output. The novel MAP joint detector decoder reduced the detection complexity by perform both detection and decoding of data on the same trellis and eliminates the need for a postprocessor stage.

A TDMR channel with SMR media based on jitter noise channel model was also modelled and implemented in software using C-programming codes. The channel considered ITI of two-track (interference from a side track) with equaliser target length of 4 (2 by 4). Jitter noise and AWGN were included in the channel model.

2D detection scheme for the TDMR channel was developed and implemented. The scheme after equalisation uses a 2D multi-level MAP detector along track to cancel ISI, and then apply regular MAP across track for ITI cancellation. The 2D multi-level MAP detector along track produces four metrics probabilities which are saved and used subsequently by the regular MAP detector across as branch metrics during ITI cancellation. Final detected data is outputted across tracks to give the saved data. Using this detection technique significantly reduce the detection complexity compared to full 2D detection.

Single parity encoders for the TDMR channel were also implemented for FEC purpose. The encoders were implemented in two versions. One of the encoders used two concatenated single parity bit codes along track separated by DRP interleaver. The other encoder used the single parity bit codes in both directions (i.e along track and across tracks) without DRP interleaver. The single parity-check code was generated by adding an extra parity-check bit to each three-length block of user data based on the parity-check constraint invoke.

To detect and decode the data with the single parity bit system, a novel 2D multi-track MAP joint detector decoder was developed and implemented for the TDMR channel. The joint detector decoder performs simultaneous detection and decoding of the last parity bits using a

single trellis structure. After equalisation, the equalised coded output data is passed to a 2D multi-track joint detector decoder along track running BCJR algorithm for joint data detection and last parity bits decoding. The decoded parity bits are removed, and the data is de-interleaved. The resulting data containing ITI from the side track is then passed to a 2D MAP decoder for first (inner) parity decoding. A regular MAP detector is then used across tracks to cancel ITI. This procedure reduces detection/decoding complexity and improve system performance.

7.2 Conclusion

In conclusion, the main aim and objectives of this research work have been achieved. The overall findings of the study conducted reveal that: FEC by concatenated single parity-check system can provide appreciable performance gain in both conventional 1D PMR channel and TDMR channel; joint detection decoding using constrained MAP detector simplifies the detection and decoding processes by performing both simultaneously on the same trellis structure; for TDMR channels with 2D interference, the complexity of full 2D joint track detection is greatly reduced by concatenating 2D MAP detector along track with regular MAP detector across tracks; in TDMR channel FEC system, interchanging the directions in which the single parity-check bits are applied can produce better performances in some situations; for low ITI situations, using single parity bits both along track and across track directions without DRP interleaver is the best option; when both ITI and ISI are high it is better to use two single parity bit system along track only separated by DPR interleaver. There is no benefit in concatenating interleavers with more than two single parity bits when ISI is low for a 1D interference channel.

7.3 Recommendations for Future Work

Even though, the overall aim and stated objectives of the study have been achieved, there are new areas of questions/directions that have emerge in the course of this work that still remain unsolved. Others are suggestions on new ideas for further investigation that can improve the performance of some of the algorithms presented in this thesis report. The following are recommendations for future work.

1. The detectors implemented in this report are based on the assumption that, the noise is uniformly distributed in all symbols of the data patterns on the average. But in high areal density TDMR channel, jitter noise is data dependant since the noise is induced only when transitions occur. Therefore, certain symbols of data pattern (0000, 1111) will have induced jitter noise in their principal boundaries, while others (1010, 0101) will have no induced jitter noise in their principal boundaries. This means in future a work, data-dependent noise-prediction (DDNP) or pattern-dependent noise prediction (PDNP) mechanism may be incorporated into the detection process for improve detection performance. This may involve the deployment of a bank DDNP filters into the detection engine to predict and whiten the future noise samples specific to each data pattern.

2. 2D constraint coding can be implemented on the TDMR channel presented in this report. Since the noise is dominated by jitter noise which is data-dependent, by imposing restrictions on the permissible 2D input data patterns on the TDMR channel, certain 2D input data patterns that induce the highest noise can be avoided locally. This will result in a detector with a reduced state trellis and improve the system performance without additional complexity in detection.

3. Iterative decoding can also be implemented on the FEC scheme presented in this thesis in order to improve the performance of the system. This can be achieved through soft information exchange between the 2D detector along track and the detector across track by passing extrinsic information across both sides. Similar setup can be used for soft information exchange between the 2D joint detector decoder and outer MAP decoder in the case of single parity code implementation. This can easily be implemented since both detector and decoders used here produce soft information output.

4. For the FEC scheme using single parity bit system both along track and across tracks without DRP interleaver, further investigation may require changing the direction in which the 2D joint detector decoder is applied from along track to across tracks direction. That is, the 2D joint detector decoder to be applied across track for ITI cancellation and inner parity decoding, then followed by MAP detector along track to cancel ISI. This may strengthen the detector across track and improve the performance by preventing error floor into the system at high SNR when both ISI and ITI are sever.

5. As additional gains in areal densities are expected to be recorded when new media technology (like the bit-patterned media recording (BPMR)) is combined with TDMR, it will be interesting to extend the application of the single parity decoders and the detectors presented in this thesis report to BPMR media as future work.

6. LDPC coding could also be investigated and implemented alongside the detection scheme presented in this report as an alternative to the single parity code system. This could provide near capacity approaching codes with improved performance and reduce decoding errors between the detector and decoder.

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Appendices

Appendix A

Published Papers

Removed due to copyright restrictions.

Appendix A1. Almustapha, M. D. Abdulrazaq, M. B. Ahmed, M. Z. Ambroze, M. A. and Davey, P. (2016). Decoding and detection for magnetic recording channel using single parity coding. In digest of Asia-Pacific Magnetic Recording Conference.
DOI: https://doi.org/10.1109/APMRC.2016.7524256.

Appendix A2. Almustapha, M. D. Ahmed, M. Z. Ambroze, M. A. and Abdulrazaq, M. B. (2017). Multi-track 2D joint signal detection and decoding for TDMR system using single parity-check coding. In proceedings of IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE).
DOI: https://doi.org/10.1109/CCECE.2017.7946623.

Appendix A3. Almustapha, M. D. Ahmed, M. Z. Ambroze, M. A. and Abdulrazaq M. B. (2017). 2D BCJR along track and across tracks detection for shingled magnetic recording media. In proceedings of 40th International Conference on Telecommunications and Signal Processing (TSP). pp. 515-519.
DOI: https://doi.org/10.1109/TSP.2017.8076040.

Appendix B

Codes

Removed.