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ABSTRACT
Orthogonal Frequency Division Multiplexing OFDM is targeted as a main modulation technique for the next generation networks due to properties of high spectral efficiency, high transmission speed and versatility. But its suffers from high power consumption due to computational complexity and complex digital signal processing. Many factors are effected power consumption and junction temperature in Field Programmable Gate Array FPGA. The important strategy is to analyses in detail the power consumption for each OFDM block and which one consumes more power. It is an important point to find a way to estimate power consumption during design cycle. In this paper exploring estimation power consumption method for each part by using special tool from Xilinx Estimation Power Analyzer XPE.

CCS Concepts
• Information systems→Storage virtualization • Software and its engineering → Virtual machines • Software and its engineering→ Software performance.

Keywords
Cyclic Prefix; IFFT/FFT bit Precision; OFDM; Xilinx power Analyze

1. INTRODUCTION
One of the most important factor for the next generation networks is the energy consumption [1]. Due to increasing network capacity to support bandwidth-hungry application such as mobile networks, cloud computing and high resolution video. Therefore, our world is dominated by network, and the important step toward the green networks communication is reduced power consumption of the electronic network devices such as in data center. OFDM modulation techniques is targeted as a next generation networks promising techniques, because high capacity and flexibility, but it is suffering from high consumption power [2]. This occurs due to complex digital signal processing so it's the negative point which effect OFDM. The most power consumption is derived by Inverse/Fast Fourier transform IFFT/FFT block because mathematical operation of digital signal processing DSP inside this part [3].

This paper explores a method to estimate OFDM power consumption for each part during design cycle. In addition, present the effect of Cyclic Prefix (CP) length and bit precision on power consumption design model.

2. ESTIMATION POWER CONSUMPTION METHOD
The main goals of next generation networks are reduced power consumption and increased network capacity. One of the most modulation schemes for that purpose is OFDM modulation. This technique includes IFFT/FFT as a central mathematical base operation and it consumes a lot of power when compared with other parts such as Modulation/De modulation, serial to parallel and Digital to Analogue/Analogue to Digital Convertor DAC/ADC due to a large number of mathematical operations and complex digital signal processing [4]. The procedure of estimation power consumption of the OFDM transceiver FPGA design model using special tools supported by Xilinx to estimate power and cooling specification of FPGA during any stage of the design cycle. This tools providing analyses detail about power and thermal information. Xilinx is offer a spreadsheet name Xilinx Power Estimation [XPE] [5]. OFDM model is implemented in Xilinx KC705 high speed analogue evaluation board design by Avnet [6]. In the design stage Xilinx provide a Simulink tool joint with Matlab 2012b and using Xilinx ISE14.7 name is system generator. The block diagram of the OFDM design model as in Figure (1) including DAC/ADC. The modulation type using Quadrature Phase Shift Keying (QPSK) and IFFT/FFT length 256 point. The first step to estimate power during design cycle as in Figure (2) show the system generator block. Firstly, define the board type for this design through the Xilinx system generator block using Kintex-7 xc7-325t-2 ffg900. Secondly, generate power report of the design model.

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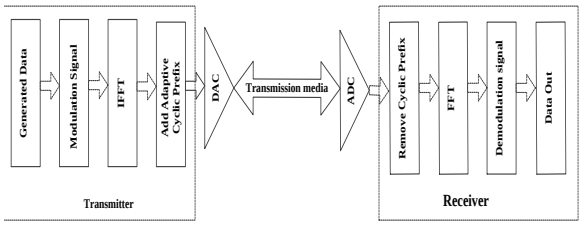

Figure 1. OFDM block diagram

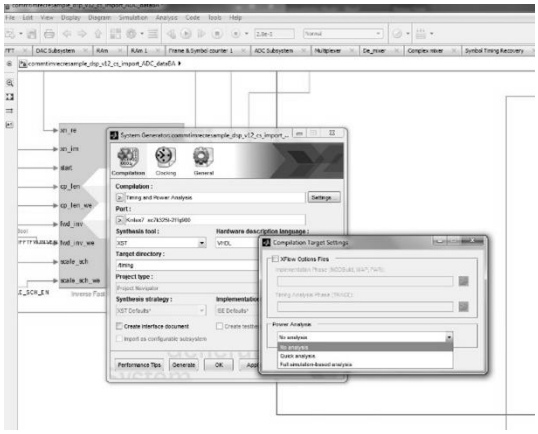

Figure 2. System generator board define

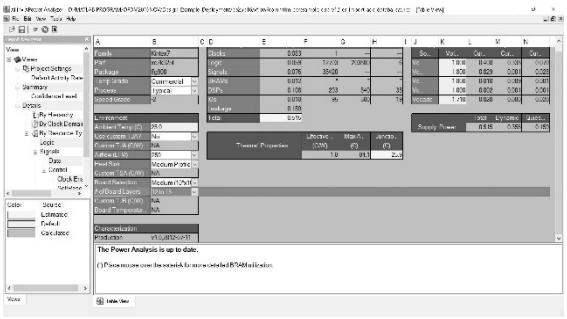

Figure 3. Xilinx power consumption report.

The output generated report includes total power, thermal power and hierarchy power. This means a power estimation for each part of the design including signal power as in Figure (3). XPower analyzer included the power of functional logic, supply voltage, static and dynamic. In addition, On-Chip thermal temperature.

The Xilinx Power Estimation XPE file is generated from the report above by select file menu and generate XPE file. It is used an Excel spreadsheet to analyze power consumption and supported by Xilinx to analyze power estimation as in Figure (4). The generated advance power report is used in next section for analyzation and represented the power estimation as a graph for functional components as shown in Figure 5.

In the following section compare the power consumption by two parameters effect on the design and IFFT/FFT. In addition, explore a method for analyses power estimation and junction thermal temperature and representation as a graph.

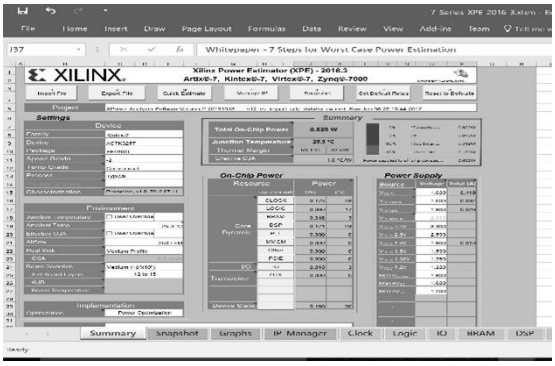

Figure 4. Excel spreadsheet to estimate power.

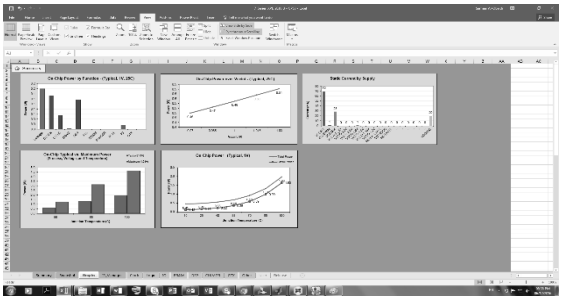

Figure 5. Power graph with junction temperature.

3. BIT PRECISION AND POWER.

The most important part of the OFDM modulation is IFFT/FFT and it is high power consumption part due to mathematical operation occurs inside it. There are many factors effect power consumptions on IFFT/FFT such as number of bits for calculation, input IFFT length, cyclic prefix, IFFT types [7]. One of these factor is increasing number of bit for calculation precision [8]. In this section explore and analyses power consumption due to increasing number of bits-precision calculation. An experiment is implemented by comparing 8-bit precision and 16-bit precision, the result output shows increasing in total power consumption. The modulation is used QPSK modulation with 256 point IFFT/FFT length.

The IFFT power consumption result for IFFT in OFDM with Cyclic Prefix length 25 and precision 8 bit is shown in Figure (6) and called Xilinx XPower Analyzer. The power consumption by IFFT/FFT is higher than the other Xilinx block in the design it consumes 23.55mw/22.63mw. Therefore, generate XPE file from XPower analyzer to uses in the Excel spreadsheet for estimate power consumption as in Figure 7. The total power on chip for all OFDM design is 0.504W with junction temperature 25.9 ℃.

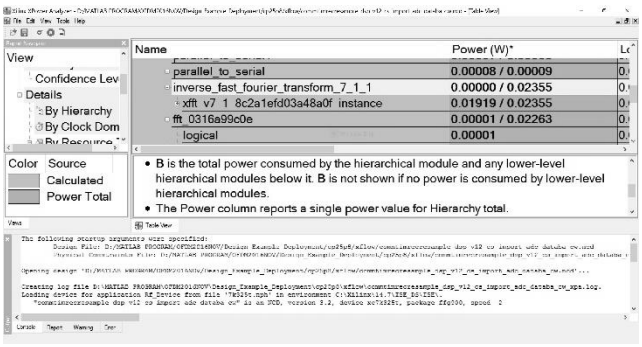

Figure 6. Power Consumption for CP25 Precision8.

Figure 7. Xilinx Power Estimation XPE

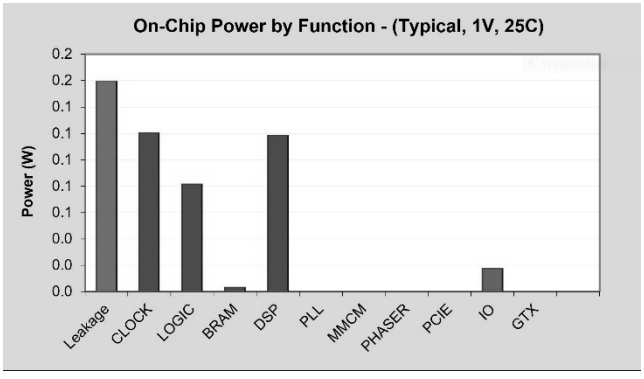

Figure 8. Power of each component type.

In the spread sheet import Xilinx estimation file generated from XPower Analyzer. The .XPE file is included all information about the design such as power and On-Chip junction tempreture.

From the Figure (7) it is applicable to represent the power with. functional components such as (logic gate, Clock, Leakage, IO) as in Figure 8.

The power consumption with junction temperature can be represented as a graph in Figure 9. The result shows the power going up with increasing junction temperature at 25℃ the power is 0.5W and forward relation between power and tempreture.

The second experiment increases the number of precision bits to a double by using 16 bits' precision. The power consumption is increased for IFFT/FFT (29.64/28.48)mw due to increse the number of bit in culculation as in Figure.10

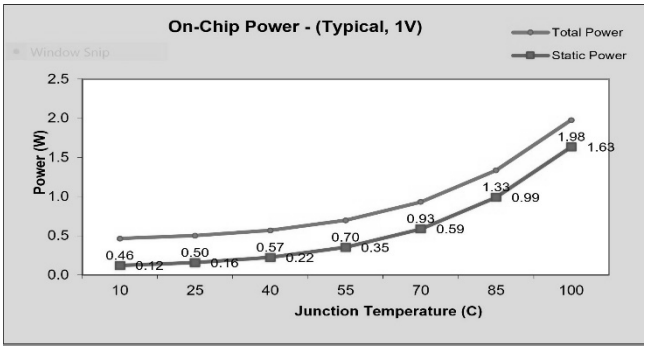

Figure 9. Power and junction temperature.

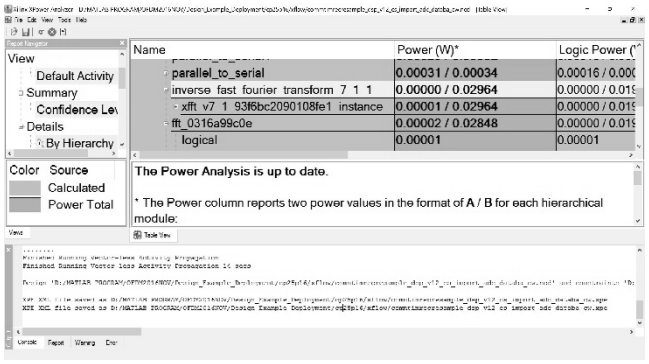

Figure 10. Power consumption with 16bit precision.

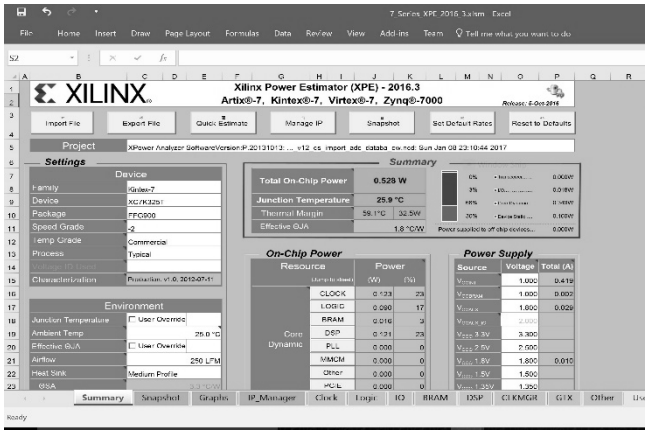

Figure 11. Spreadsheet power for 16bit precision.

Total power 0.528W for all block design is represented in spreadsheet as in Figure 11. The power is increased for logic, DSP and clock processing. The graph of power as in Figure 12. On-Chip power for Junction temperature is shown in Figure 13. However; power is going up for the same junction temperature 25 ℃ to 0.52W for all OFDM design system. The result shows that the forward relation between power and junction Temperature with number of bit for precision calculation increased.

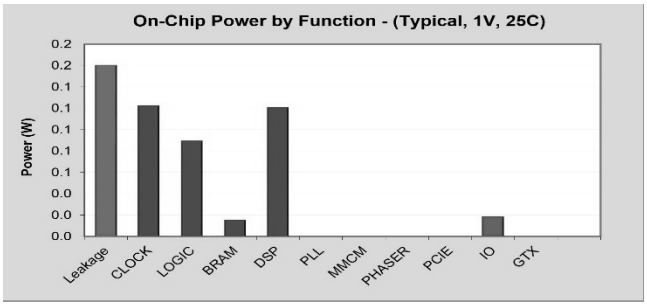

Figure 12. Component power for 16-bit precision.

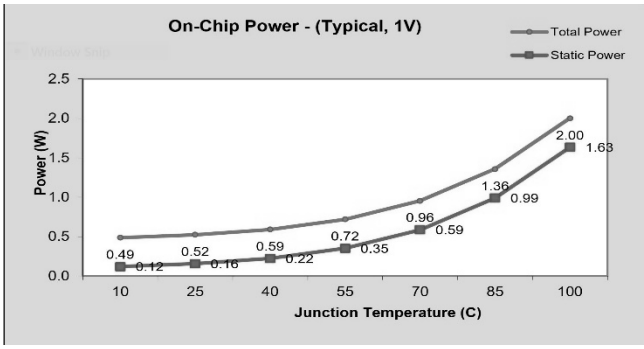

Figure 13. Power vs Junction temperature of 16-bit precision.

4. CYCLIC PREFIX AND POWER CONSUMPTION

Next generation high speed multicarrier modulation is used OFDM as a base modulation technique due to flexibility of variant parameters [9]. This modulation is suffered from inter-symbol-interference(ISI) or overlapping of the symbols because short distance between subsequent symbol. Therefore, the signal distortion and noise are increased due to overlapping. This effect is diminished by adding cyclic prefix between symbol. The CP is added by a copy of the last fraction of each symbol in the time domain and put in the front of the corresponding symbol [10] as in Figure 14. A cyclic prefix mechanism can be implemented by putting a gap between symbols and filling the gap using CP in the transmitter side. The first experiment is implemented using 25 samples cyclic prefix and 50 samples. Xilinx system generator provide IFFT Simulink blocks includes option to add CP. Our experiment is focus on Fast Fourier Transform FFT v.7.1 from Xilinx with length 256 point. The result shows increasing in total power consumption when increasing CP length due to more processing in the time domain to make a copy of the end of each symbol frame and added in the front of it. The result in Figure (15) show the power decrease of IFFT/FFT (22.46/21.93) mw compared with CP=25 in previous experiment in Figure (6). The decreasing occurs due to the IFFT/FFT processing is turn OFF for period during CP copy. The result in spreadsheet Figure 16. Shows increasing in logic, clock and BRAM power but small change for DSP power. This approve the IFFT/FFT is turn OFF during copy of CP that explain why the power is decrease when increasing length of CP.

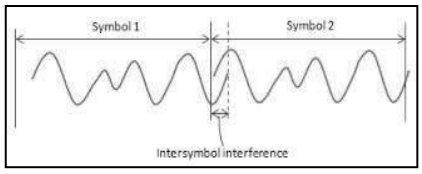

Figure 14. Mechanism of Cyclic prefix.

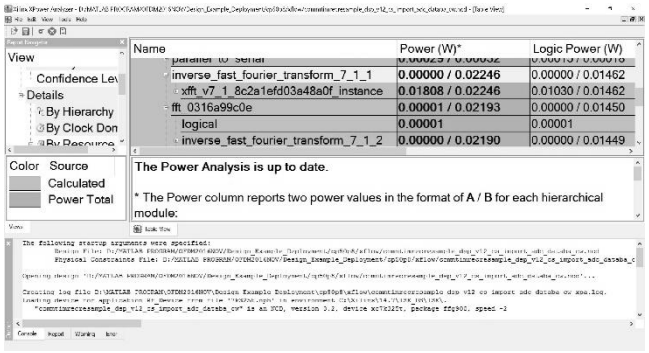

Figure 15. XPE power with CP 50.

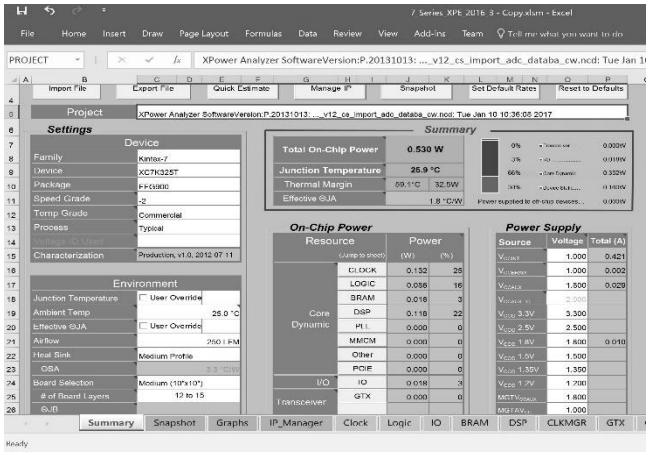

Figure 16. Cyclic prefix 50 symbol.

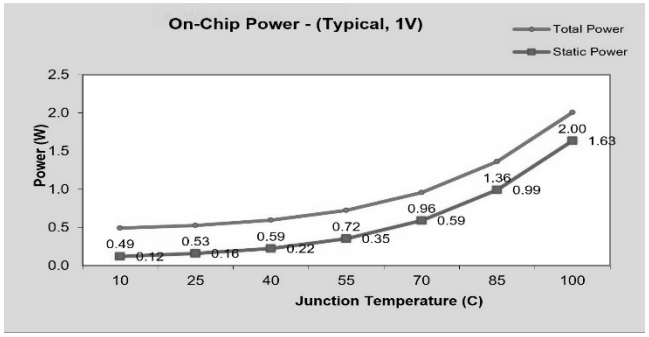

Figure 17. Junction temperature CP 50.

The power of junction temperature result in 25 ℃. the total power increased to 0.53W with cyclic prefix 50 instead of 0.5 W with cyclic prefix 25 as in Figure 17. Finally, the power is decreased in Xilinx FFT when CP is increased to double.

5. CONCLUSION

Next generation networks will be targeted to reducing power consumption in OFDM modulation for greener world. The procedure to measure power consumption described in previous section through this paper like a novel for study. Special case when using tools from Xilinx for analyses. During the study is found that forward relation between cyclic prefix and total power consumption but the power consumption of IFFT/FFT decreased. In addition, the power increased when increasing number of bits for precision calculation.

6. ACKNOWLEDGMENT

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