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Effective chemical treatment for high efficiency graphene/Si Schottky junction solar cells with a graphene back-contact structure

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Abstract

We demonstrate a high-efficiency graphene/Si Schottky junction solar cell with an easy to fabricate graphene back-contact structure and effective chemical treatments. This device effectively overcame the current challenges associated with reported graphene/Si Schottky solar cell structures. The short-circuit current density for such a device is increased by around 20% due to the increase of the active area of this device, compared to previous graphene/Si Schottky junction solar cell devices. The undesirable s-shaped kink in *J-V* curves, as found in previous works, have been eliminated by using Formamide treatment for 30 min prior to an annealing process in the forming gas. The fill factor of this device is improved by 40% after this treatment, due to the effective removal of the unwanted PMMA residue. Moreover, volatile oxidant vapour and anti-reflection coating are applied within the fabrication process for this device to further improve solar cell performance. An efficiency of 9.5% has successfully been achieved for the fabricated device using the fabrication techniques developed in this work. Our device presents a viable and achievable approach to preparing low-cost and high-performance graphene/Si Schottky junction solar cells. Copyright © 2017 VBRI Press.

Keywords: Graphene/Si Schottky junction solar cell; s-shaped kink; formamide treatment; anti-reflection coatings.

Introduction

The attractive properties of graphene, such as near zero band-gap, high electrical conductivity; high mobility, flexibility, and high transparency have stimulated a lot of research interest [1]. One of the promising applications for graphene is in solar cells. There are two basic structures reported so far for graphene/silicon Schottky junction solar cells. The first structure is with a top-window while the second structure is without a top-window [2]. Although a graphene/silicon Schottky junction solar cell with the first structure has a higher efficiency, it suffers from some serious disadvantages such as, a distinctive s-shaped kink (a non-ideal) in the measured *J-V* curves, high cost and complex fabrication process. Graphene/Si Schottky solar cells without a top window structure have recently been reported as low cost and simple graphene/Si Schottky solar cells [2, 3]. However, the fabricated devices with this structure still suffer from a distinctive s-shaped kink in the measured *J-V* curves. In fact, several graphene/Si junction solar cells reported suffer from a distinctive s-shaped kink in the measured *J-V* curves near open circuit voltages [4-12].

This kink affects solar cell performance by reducing the fill factor. Actually, there are many reasons for the s-shaped kink effect. An and his co-workers referred that it is due to the limitation of accessible states for the holes in graphene [8, 12]. Yang and his co-workers explain that this effect is due to carrier recombination at the graphene/Si interface, and this issue is reduced by using GO as a passivation layer for the silicon surface [13]. Song and his co-workers suggested that the native oxide thickness would affect this shape when the native oxide thickness is about 1.5 nm [14]. In several cases, this issue can also be reduced using chemical doping or electrostatic gating [6-8, 12].

Herein, we report a high-efficiency graphene/Si Schottky solar cell with a graphene back contact structure to overcome the disadvantages of graphene/Si Schottky solar cell structures. A new technique using Formamide treatment in combination with an annealing process in forming gas has been developed to suppress the behavior of distinctive s-shaped kinks. To additional increase the solar cell efficiency, chemically doped graphene is applied. Unlike reported devices, a sputtering technique is used to form anti-reflection coating (ARC) on the front of

Si substrates to reduce the reflected light and further improve the solar cell performance.

Experimental

Preparation of graphene

The monolayer graphene (Gr) was synthesized on copper foil through reported chemical vapor deposition (CVD) method [15]. Wet transfer process was used to transfer the graphene on the desired substrates (see Fig. S1 in supporting information). Firstly, PMMA was dissolved in the chlorobenzene with a 10 mg/ml concentration and spin-coated onto one side of the graphene film at a spin speed of 4000 rpm for 30 s. Then, the sample was baked at 180 °C for 1 min. To etch Cu substrate, 3:1 DIW: HNO₃ was employed for 3 min followed by etching in 0.1 M ammonium persulfate for approximately 3 h, with the endpoint determined when Cu was no longer visible. Afterwards, the sample was etched for an additional 7 h in a separate fresh ammonium persulfate bath to ensure that the Cu was completely removed. The resulting PMMA/graphene membrane was transferred to a rinse bath of DI-water for 20 min.

Fabrication of graphene/n-Si Schottky junction solar cells

To prepare this device, an N-type (100) single c-Si wafer with a resistivity of 2-3 Ωcm⁻¹ was used as the substrate to fabricate the Gr/Si Schottky junction solar cells. Silicon substrates were firstly cleaned with RCA procedure to avoid the metal ion contaminations. Then, Silicon substrates were immersed in a diluted 2% HF solution for 30 s to remove the oxide layer. At that time, the Cr/Ag layer was formed at 6 x 10⁻⁷ Torr using sputtering technique on the backside (unpolished side) of Si substrates. Afterwards, monolayer graphene was directly transferred onto the central area of Si substrates as shown in Fig.2a. The acetone treatment was used to remove the PMMA layer. After that, samples were immersed in Formamide (ACS reagent grade, ≥ 99.5%, Sigma-Aldrich) for 30 min followed by blow-drying with nitrogen. After drying process, samples were then annealed at 200 °C for 2 h in a hydrogen/argon environment. For a Cr/Au electrode, a Cr layer was thermally evaporated onto the surface of graphene as an adhesion layer. Subsequently, an Au layer was sputtered on the top of Cr layer. Then, SiO₂ and SiO₂/TiO₂ layers were sputtered at 10⁻⁷ Torr and room temperature on the front of Si substrates. Finally, graphene was p-doped by 65% HNO₃ for 30 s.

Optical and electrical characterization

The reflectance spectra of Si substrates with and without anti-reflection coating (ARC) were recorded using a UV/Vis/NIR spectrophotometer. The quality of graphene was characterized by Optical microscopy and Raman spectroscopy with 532 nm laser. To study the electrical characteristics of the transferred graphene, four-probe electrical measurements were carried out. The photovoltaic characteristics of the device, which were

calibrated by a standard Si solar cell, were measured using a key-sight B1500A semiconductor Analyzer and a solar simulator under AM1.5 and conditions at an illumination intensity of 100 mW/cm².

Results and discussion

After transferring graphene onto desired substrates, the PMMA layer is removed by a standard acetone treatment process. However, there is a residue of PMMA as acetone treatment cannot remove this layer completely. This residue has a negative effect on the graphene properties, such as reducing the mean free path and mobility of carriers [16]. Moreover, it alters the electronic band structure of graphene when it is adsorbed at the edge or defect sites [17-19]. In addition, removing this residue will improve the contact between the graphene and electrodes [2]. Actually, removing the residue of PMMA is a challenging issue for obtaining a graphene sheet with its intrinsic electronic properties, although there are many techniques for this purpose [20]. For example, a modified Radio Corporation of America (RCA) cleaning process has been used to reduce this issue. However, this technique requires complicated wet chemistry and is limited to cleaning only a local area [21-23]. Formamide liquid (CH₃NO) has also been used to minimize the PMMA issue [24], but this method requires long time (overnight) to deal with PMMA issue. Other teams have tried to reduce residue by using annealing process in the forming gas at different temperatures. However, a systematic study of PMMA decomposition on graphene has proved that this technique cannot entirely remove the residue [25, 26].

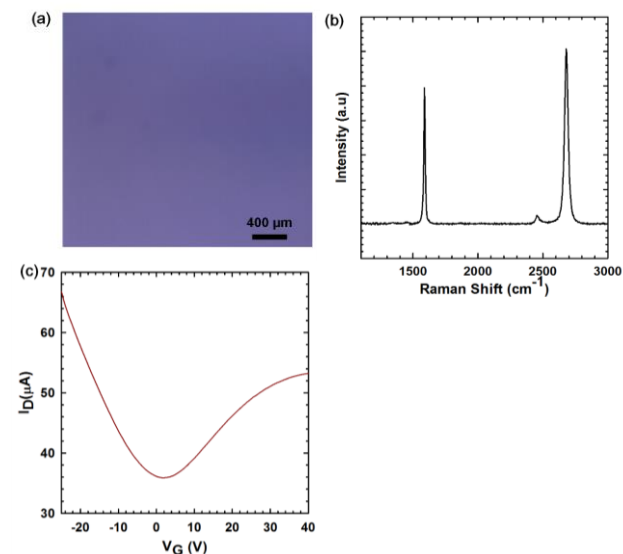


Fig. 1. (a) Optical image of transferred graphene onto SiO₂/Si substrate. (b) Raman spectrum of transferred graphene onto SiO₂/Si substrate. (c) Current-voltage (I_D - V_G) curve for the GFET measured in air.

To effectively reduce the effect of unwanted PMMA residue, Formamide treatment for 30 min was firstly used to donate electron charge at the interface with graphene

[24]. Then, the annealing process in a hydrogen/argon environment for 2 h was applied to effectively restore the intrinsic electrical properties of transferred graphene. The quality and monolayer nature of transferred graphene were verified by optical microscope. **Fig. 1a** displays a typical optical image of transferred graphene film using Formamide treatment onto SiO₂/Si substrate. It can be seen that transferred graphene film was almost uniform and continuous. The monolayer nature of transferred graphene was also evaluated by Raman spectroscopy as shown in **Fig. 1b**.

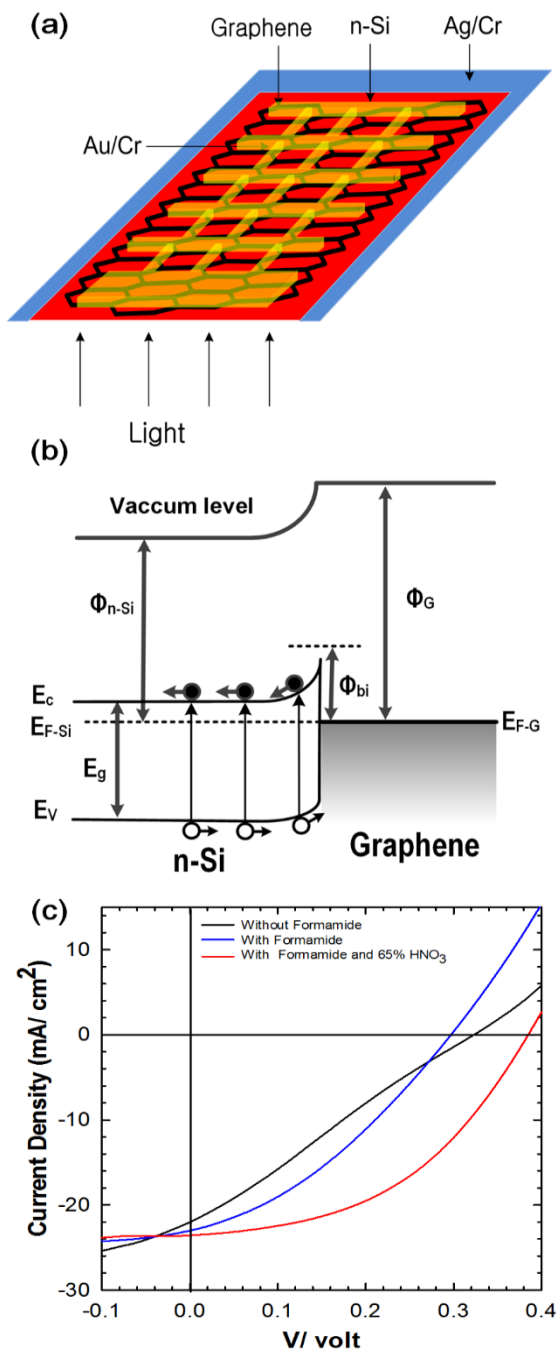


Fig. 2. (a) Schematic structure of graphene/Si Schottky junction solar cell. (b) Schematic energy diagram of graphene/Si Schottky junction and photo-excited electron transfer. (c) *J-V* characteristics for the graphene/Si Schottky solar cells that are annealed in forming gas for 2h.

It can be observed from this figure that the spectrum is for monolayer graphene, and there is no D band in this spectrum. The intensity ratio of the 2D to G bands for transferred graphene was around two. These characteristics indicated that the transferred graphene film using the improved technique was a high-quality monolayer [27-29]. Four-probe electrical measurements were carried out on the graphene field effect transistor (GFET) in air to study the electrical characteristics of the transferred graphene on the SiO₂/Si substrate. The Gate voltage (V_G) was applied through the backside of the Si substrate, and the source-drain bias was constant at 10 mV. The channel width (W) and length (L) were 80 and 90 μm , respectively. **Fig. 1c** shows a typical I_D - V_G curve of the GFET. It can be noted that the Dirac point is at about 2.6 ± 1 V, and this confirms that using Formamide treatment before annealing process was effectively minimized the PMMA residue. The sheet resistance of the transferred graphene is in the range of $450 \pm 50 \Omega^{-1}$. The new graphene/Si Schottky junction solar cell structure with a back-contact graphene is illustrated in **Fig. 2a**. This structure has a number of advantages. In particular, it is fabricated to avoid the formation and etching steps of the SiO₂ layer in the fabrication process of reported devices with a top window structure. Moreover, the active area for this structure is larger than the area of the previous structure. This means that the number of electron-hole pairs generated is higher and leads to an increase in the solar cell efficiency. In addition, this structure enables the antireflection coatings formed by sputtering technique to be involved in the fabrication process in order to reduce the reflected light from front Si substrates and improve the solar cell efficiency. The Schottky junction in this structure is formed at the interface between the graphene and silicon as shown in **Fig. 2b**. A leakage current density of this device is in the order of $\mu\text{A}/\text{cm}^2$ at reverse bias, and this value is comparable with that value for reported graphene/Si Schottky junction solar cells [6, 13]. **Fig. 2c** shows the current-voltage characteristics of graphene/n-Si Schottky junction solar cells. It can clearly be observed the *J-V* curve (black) for an untreated device with Formamide is non-ideal, as the forming gas technique cannot effectively remove the PMMA residue.

The short circuit current (J_{SC}), open circuit voltage (V_{OC}), fill factor (FF) and power conversion efficiency (PCE) of this device were 24.2 mA/cm², 0.32 V, 25%, 1.96% respectively. In contrast, the *J-V* curve (blue) in the same figure for a Formamide treated device is ideal. For this device, J_{SC} , V_{OC} , FF and PCE were 25.3 mA/cm², 0.30 V, 35% and 2.6% respectively. This indicates that minimizing the PMMA residue could successfully increase FF of this device by 40%, hence improving the PCE by 30% in comparison with those parameters for a previous device. **Table 1** shows the comparison of our device with other reported devices [3, 13]. It is clear that our device displays the highest photovoltaic achievement as shown in this table; in particular, the FF and PCE were enhanced by about 50% and 60% respectively in comparison with those parameters for fabricated device with the top window structure. These enhancements are

because of using the back-contact structure and Formamide treatment within the fabrication process.

Table 1. Open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (FF), and power conversion efficiency (PCE) of fabricated devices with different structures.

Structure	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	η (%)
Top window	310	21.4	24	1.57
Without top window	310	7	18	0.39
Back-contact	300	25.3	35	2.6

The effect of chemical doping process on graphene was examined to further improve the solar cell performance. **Fig. 2c** also shows the J - V curve (red) of this device after treating graphene with the vapor of 65% HNO_3 for 30 s, showing a higher PCE of 4.6% with V_{oc} of 0.38 V, J_{sc} of 26 mA/cm² and FF of 45%. This enhancement can be attributed to improve the graphene's electrical conductivity [35] and contact between the graphene and metal contact when the PMMA residue has been minimized [2]. To significantly minimize the reflectance of Si substrates, SiO_2 and SiO_2/TiO_2 coatings were sputtered on Si substrates at room temperature.

Schematic designs of these coatings on Si substrates are shown in **Figs. 3a** and **b**. The thickness of the SiO_2 layer should equal one quarter the wavelength of the incoming wave (i.e. $d_{SiO_2} = \lambda_o/4n_{SiO_2}$, where λ_o the mid-range wavelength of 500 nm, n_{SiO_2} and d_{SiO_2} represent the refractive index and thickness of SiO_2 layer, respectively [40]. To achieve a zero reflectance using DLAR coating, the thickness of SiO_2 and SiO_2/TiO_2 layers should satisfy following **Eqs. 1** and **2**:

$$\frac{n_2 d_2}{\lambda_0} = \frac{1}{2\pi} \tan^{-1} \left\{ \pm \left[\frac{(n_s - n_0)(n_0 n_s - n_1^2) n_2^2}{(n_1^2 n_s - n_0 n_2^2)(n_2^2 - n_0 n_s)} \right]^{1/2} \right\} \quad (1)$$

$$\frac{n_1 d_1}{\lambda_0} = \frac{1}{2\pi} \tan^{-1} \left\{ \pm \left[\frac{(n_s - n_0)(n_0 n_s - n_2^2) n_1^2}{(n_1^2 n_s - n_0 n_2^2)(n_1^2 - n_0 n_s)} \right]^{1/2} \right\} \quad (2)$$

where, d_1 and d_2 represent the thickness of the TiO_2 and SiO_2 layers, respectively. Moreover, n_0 , n_1 , n_2 and n_s refer to the refractive index of air, TiO_2 , SiO_2 and Si substrate, respectively [41]. The effect of the ARC on the Reflectance of Si substrates was investigated using a spectrophotometer with an integrating sphere, and a Si substrate was used as a reference. As shown in **Fig. 3c**, the diffused reflectance (R) of Si substrates with and without SiO_2 and SiO_2/TiO_2 coatings is as a function of the wavelength within the range of 400-1000 nm. It can be observed in this figure that average R of the reference wafer is around 35% within this range, while the average R was reduced to 17.5% and 4.3% within the same range by forming SLAR (SiO_2) and DLAR (SiO_2/TiO_2) coatings on Si substrates, respectively. The J - V characteristics of fabricated devices using Si substrates with SLAR and DLAR coatings are shown in **Fig. 4**. As shown in this

figure, the J - V curve (black) for a fabricated Si/graphene device with a SiO_2 layer exhibited a significant improvement in photovoltaic performance in comparison with a fabricated device without SiO_2 layer, showing a higher J_{sc} of 33.5 mA/cm² with FF of 47.4% and PCE of 7% as displayed in **Table 2**. This improvement is due to increasing the J_{sc} from 26 to 33.5 mA/cm² and V_{oc} from 0.38 to 0.442 V after reducing the reflected light by the SiO_2 layer.

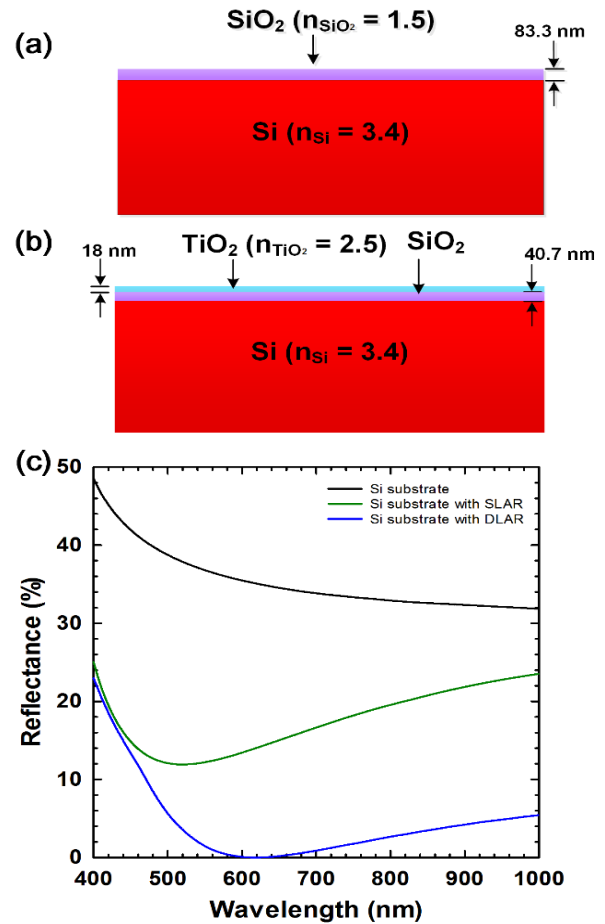


Fig. 3. Schematic structures of Si substrates with (a) SLAR and (b) DLAR coatings. (c) Reflectance spectra of Si substrates with and without antireflective coatings.

It can also be observed in **Fig. 4** (red curve) and **Table 2** that the fabricated device using a Si/graphene device with DLAR coating displays superior photovoltaic achievement, in particular, a J_{sc} of around 44 mA/cm² that increases by 10.5 mA/cm² in comparison with J_{sc} for the previous device as the reflected light is further minimized. This results in an increase the FF from 47.4 to 50% and PCE from 7 to 9.5%. Whereas, V_{oc} for a fabricated Si/graphene device with DLAR coating was slightly improved from 0.422 to 0.458 V as listed in **Table 2**. It is also clear from this table that the maximum efficiency is 9.5 % for final fabricated device, and to the best of our understanding, this value is a new record for graphene/Si solar cell efficiency reported to date in comparison with fabricated devices without a top window structure.

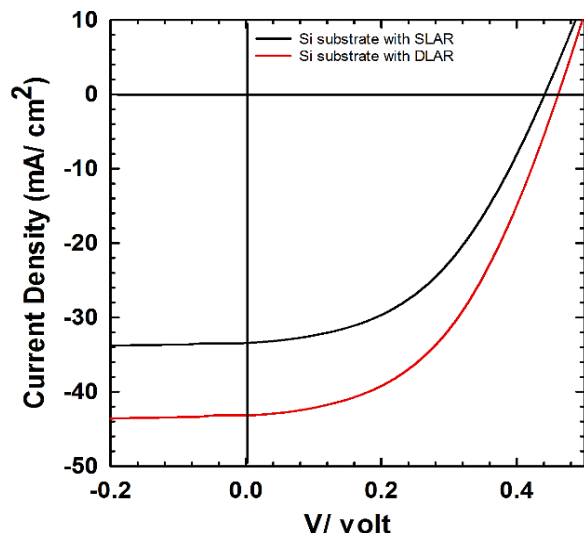


Fig.4. *J-V* characteristics for the fabricated devices using Si substrates with antireflective coatings after Formamide treatment, annealing in forming gas for 2h and doping treatment.

Table 2. Open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (FF), and power conversion efficiency (PCE) of fabricated devices using Si substrates with and without antireflective coatings after Formamide treatment, annealing in forming gas for 2h and doping process.

Devices (mV)	V_{oc}	J_{sc} (mA/cm ²)	FF (%)	η (%)
Si	380	26	45	4.6
SLAR	422	33.5	47.4	7
DLAR	458	44	50	9.5

Conclusion

We presented the significant of a back-contact structure on the graphene/Si Schottky junction solar cell performance. It was also discovered that the distinctive s-shaped kink in measured *J-V* curves of graphene/Si Schottky junction solar cells could be attributed to PMMA residue. The presence of this residue on transferred graphene remains a key challenge in the fabrication of graphene devices. To manage this issue, Formamide treatment was applied prior the annealing process to effectively minimizes the effect of PMMA residue and consequently improves solar cell performance. Applying chemical doping and anti-reflection coating techniques could be further improved the efficiency of this device. This novel device offers a feasible way to fabricate a high performance and affordable graphene/Si Schottky junction solar cell.

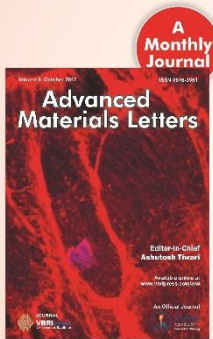
Acknowledgements

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Supporting information

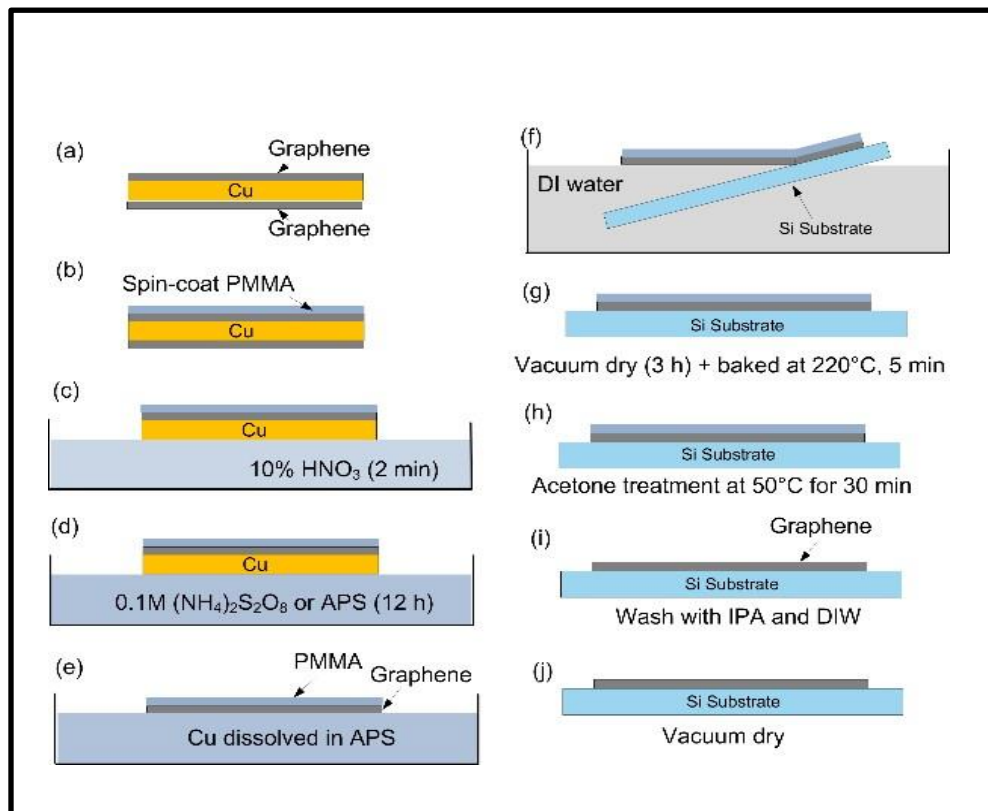


Fig. S1. Schematic illustration of the wet-transfer process on Si substrates. (a) Monolayer graphene is on both sides of 25 μm Cu foil. (b) Depositing a supported layer of PMMA on graphene. (c, d and e) Graphene at the bottom and Cu layers were etched by HNO₃ and Ammonium per-sulphate, respectively. (f) After transferring the resulting graphene/PMMA to DI-water bath, both were transferred to the Si substrate. (g) Drying and baking processes of the graphene/Si. (h and i) Cleaning process to remove the PMMA layer from the graphene surface. (j) Drying process of the graphene/Si sample.